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Elucidation of Various PWM Techniques for a Modified Multilevel Inverter

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Abstract

This paper focuses on hybrid H-bridge cascaded MLI using two equal dc sources in order to produce a five-level output. The proposed topology reduces the number of dc sources and switching elements. This paper emphasis on various inverted sine carrier PWM (ISCPWM) techniques with equal amplitude and unequal amplitude carriers. The inverted sine carrier pulse width modulation (ISCPWM) technique enhances the fundamental output voltage particularly at lower modulation index ranges with reduction in total harmonic distortion (THD) and switching losses. Simulation is performed using MATLAB-Simulink. From the simulation it is observed that variable amplitude inverted sine carrier variable frequency (VAISCVF) strategy provides output with relatively low distortion for all strategies. It is also seen that variable amplitude inverted sine carrier phase disposition (VAISCPD) is found to perform better for all strategies since it provides relatively higher fundamental RMS output voltage.

Keywords*: THD, CMLI, PWM, CF, FF, ISC*

1. Introduction

Multi-level inverters have become an effective and practical solution for increasing power and reducing harmonics of AC waveforms. By synthesizing the AC output voltage from several levels of DC voltages, staircase output waveform can be produced. Rodriguez et al [1] have introduced a survey of multilevel inverters topologies, controls, and applications. A novel PWM scheme to eliminate common mode voltages in cascaded multi-level inverters presented by wang et al [2]. Aghdam et al [3] made a analysis on various multi-carrier PWM methods for asymmetric multi-level inverter. Song et al [4] deals with cascaded multilevel inverter employing three-phase transformers and single dc input. A sinusoidal PWM method with voltage balancing capability for diode-clamped five-level converters presented by Pan et al [5]. Zhao et al [6] proposed a novel PWM control method for hybrid-clamped multilevel inverters. Dixon et al [7] proposed a asymmetrical multilevel inverter for traction drives using only one dc supply. A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications introduced by Ebrahimi et al [8]. Abdalla et al [9] developed a multilevel DC-link inverter. Distributed control of a fault-tolerant modular multilevel inverter for direct-drive wind turbine grid interfacing introduced by parker et al [10]. Younghoon Cho et al [11] developed a carrier-based neutral voltage modulation strategy for multilevel cascaded inverters under unbalanced dc sources. Murali et al [12] made a design and analysis of voltage source inverter for renewable energy applications. Jamaludin et al [13] proposed a multilevel voltage source inverter with optimized usage of bidirectional switches. Gabriel et al [14] introduced a five-level multiple-pole pwm ac – ac converters with reduced components count. Lim et al [15] suggested a modular-cell inverter employing reduced flying capacitors with hybrid phase-shifted. Rasilo et al [16] proposed an effect on multilevel inverter supply on core losses in magnetic materials and electrical machine. Reddy et al [17] developed an embedded control for a n -Level DC – DC – AC Inverter. The main purpose of this work is to reduce the components in hybrid H-bridge multilevel inverters which have been developed to increase number of output voltage levels using less number of semiconductor switches. Simulation results are presented to validity the proposed strategies.

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2. Toplogy and Operation

Figure 1 illustrates cascaded Hybrid H-bridge multilevel inverter. As shown in Figure 1, the multilevel inverter consists of six DC voltage sources and fifteen switches. The configuration and the principle of operation of the proposed inverter have been presented. One switching element and four diodes added in the conventional full-bridge inverter are connected to the center-tap of dc power supply.

3. The Proposed Multilevel Inverter

In multilevel inverters, the desired output voltage is achieved by suitable combination of multiple low dc voltage sources used at the input side. The most important part in multilevel inverters is switches which define the reliability, circuit size, cost, installation area and control complexity. To provide a large number of output levels without increasing the number of bridges, a new modified cascaded hybrid H-bridge symmetrical multilevel converter is proposed in this paper. Table 1 displays the various possible switching states of the proposed inverter. Table 2 shows the comparison between cascaded MLI and proposed topology.

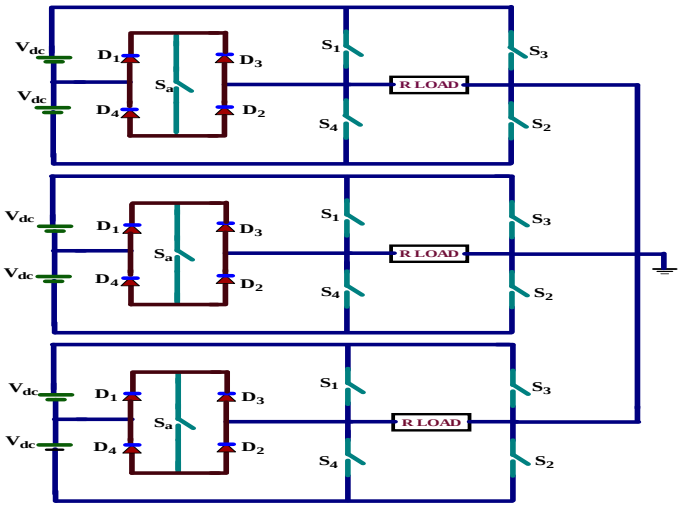

Figure 1. Schematic of chosen three phase, five level modified cascaded hybrid H-bridge inverter

Table 1. Voltage ouput and switching states

Vphase a	S_a	S_1	S_2	S_3	S_4
$2V_{dc}$	0	1	1	0	0
V_{dc}	1	0	0	0	0
0	0	0	0	0	1
$-V_{dc}$	1	0	1	0	0
$-2V_{dc}$	0	0	0	1	1

Table 2. Comparison between existing system and proposed system

Type	Conventional CMLI	Chosen hybrid H-bridge cascaded inverter
No. of switches	24	15
No. of clamping diodes	24	15
No. of DC sources	6	6

4. Modulation Schemes

There are many control techniques employed for multilevel inverters. For controlling the output voltage, one of the methods is Sinusoidal PWM method. In this method, a fixed DC input voltage is applied to the inverter and get a controlled AC output voltage by adjusting the ON and

OFF periods of the inverter power semiconductor devices. The sinusoidal pulse width modulation is applied in the proposed inverter since it has various advantages over other techniques. This technique eliminates low order harmonics in order to reduce the distortion in the output voltage. In this paper an inverted sine wave (ISCPWM) of high switching frequency is taken as a carrier wave and is compared with that of the reference sine wave. The pulses are generated whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave. The number of carriers required to produce the m level output is m-1. The inverted sine PWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM. The inverted sine carrier PWM (ISCPWM) method uses the sine wave as reference signal while the carrier signal is an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index.

This work uses six different modulation strategies that all well known carriers based multilevel PWM strategies as descried below:

A. Inverted Sine Carrier Phase Disposition (ISCPD)

To produce a five-level output, this PWM strategy uses only four carriers, all these carriers have the same amplitude, frequency and phase. Since all carriers are selected with the same phase. The PD PWM signal generation for modulation index m_a = 0.8 is shown in Figure 2.

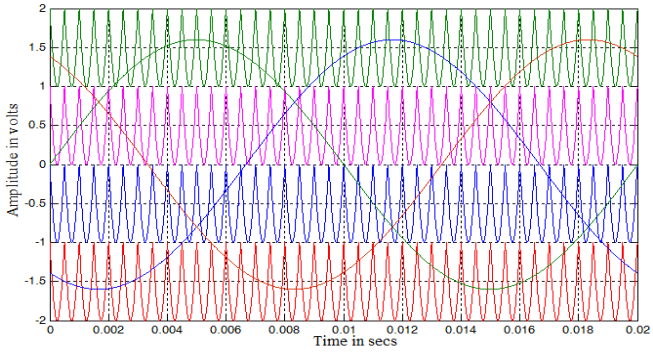

Figure 2. Modulating and carrier waveforms for ISCPDPWM strategy (m_a = 0.8 and m_f = 40)

B. Inverted Sine Carrier Alternate Phase Opposition Disposition (ISCAPOD)

The APODPWM signal generation for m_a = 0.8 is shown in Figure 3. Here we present four inverted sine carriers with one sine reference for a five level inverter. In this method carriers are seem to be inverting their phase in turns from previous one and the same procedure is repeated below the zero average levels. All these carriers have the same amplitude, frequency, and phase.

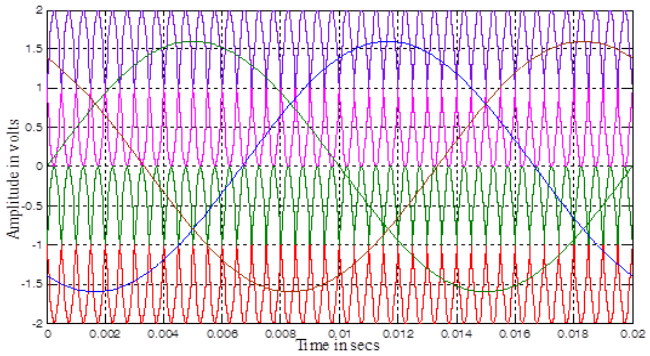

Figure 3. Modulating and carrier waveforms for ISCAPODPWM strategy (m_a = 0.8 and m_f = 40)

C. Inverted Sine Carrier Variable Frequency (ISCVF)

The number of switchings for upper and lower devices of chosen MLI is much more than that of intermediate switches. This method is having constant amplitude constant frequency. It is named as variable frequency PWM. The VFPWM signal generation for m_a = 0.8 is shown in Figure 4.

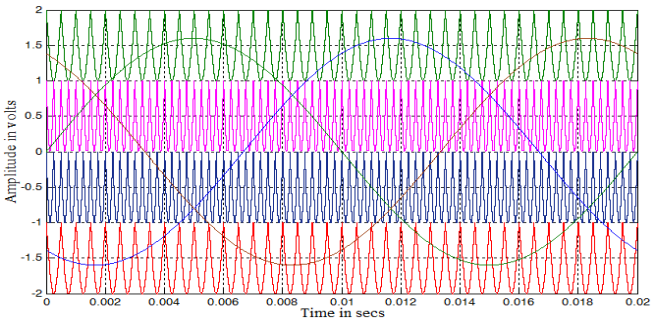

Figure 4. Modulating and carrier waveforms for ISCVFPWM strategy
(m_a = 0.8 and m_f = 40 for lower and upper switches and m_a = 0.8 and m_f = 80 for intermediate switches)

D. Variable Amplitude ISCPD (VAISCPD)

In this method is same as PD but varying amplitude, so it is named as Variable Amplitude. It provides lower total harmonic distortion and relatively higher fundamental RMS voltage, while comparing to PDPWM technique. The carrier arrangement for this strategy is shown in Figure 5.

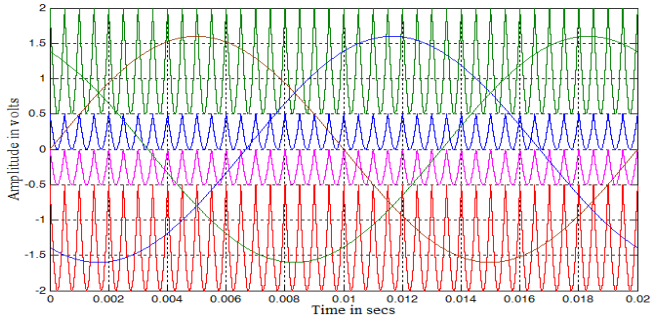

Figure 5. Modulating and carrier waveforms for VAISCPDPWM strategy (m_a = 0.8 and m_f = 40)

E. Variable Amplitude ISCAPOD (VAISCAPOD)

Carrier arrangement for VAAPODPWM strategy is shown in Figure 6. It seems that four carriers generated for a five level inverter, is divided into two groups according to the positive and negative average levels. This scheme is similar to the VAPDPWM strategy but the two groups are phase shifted by 180 degree from its adjacent one.

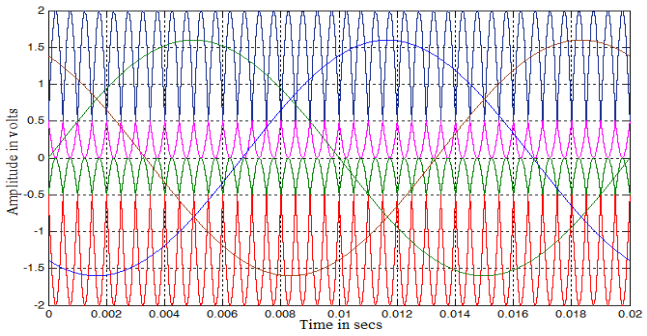

Figure 6. Modulating and carrier waveforms for VAISCAPODPWM strategy (m_a = 0.8 and m_f = 40)

F. Variable Amplitude ISCVF (VAISCVF)

In this strategy is same as VF, but amplitude somewhat different. All carriers are selected in same phase. It generate five level output. The VAVFPWM signal generation for m_a = 0.8 is shown in Figure 7.

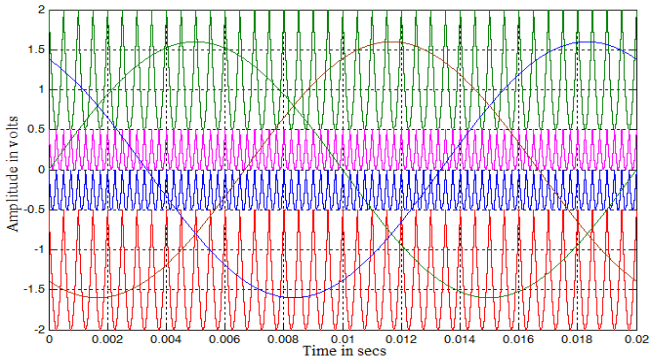

Figure 7. Modulating and carrier waveforms for VAISCVFPWM strategy (m_a = 0.8 and m_f = 40)

5. Simulation Results

Simulation studies are performed by using MATLAB-SIMULINK to verify the proposed PWM strategies for chosen three phase Hybrid H- bridge type cascade five level inverter for various values of m_a ranging from 0.6 – 1 and corresponding %THD values of output voltage are measured using FFT block and they are shown in Table 3. Table 4 shows the V_{RMS} of fundamental of inverter output for the same modulation indices. Tables 5, 6 and 7 show the Form Factor (FF), Crest Factor (CF) and Distortion Factor (DF). Figures 8-19 show the simulated output voltage of chosen hybrid cascaded inverter and the corresponding FFT plots with different strategies but only for one sample value of m_a=0.8 and m_f=40. Figure 8 shows the five level output voltage generated by PDPWM strategy and its FFT plot is shown in Figure 9. From Figure 9, it is observed that the PDPWM strategy produces significant 9th, 30th, 31st and 40th harmonic energy. Figure 10 shows the five level output voltage generated by APODPWM strategy and its FFT plot is shown in Figure 11. From Figure 11, it is observed that the APODPWM strategy produces significant 3rd, 5th, 35th, 37th and 39th harmonic energy. Figure 12 shows the five level output voltage generated by VFPWM strategy and its FFT plot is shown in Figure 13. From Figure 13, it is observed that the VFPWM strategy produces significant 38th and 40th harmonic energy. Figure 14 shows the five level output voltage generated by VAPDPWM strategy and its FFT plot is shown in Figure 15. From Figure 15, it is observed that the strategy produces significant 3rd, 5th and 40th harmonic energy. Figure16 shows the five level output voltage generated by VAAPODPWM strategy and its FFT plot is shown in Figure 17. From

Figure 17, it is observed that the VAAPODPWM strategy produces significant 3rd, 5th, 7th, 35th and 39th harmonic energy. Figure 18 shows the five level output voltage generated by VAVFPWM strategy and its FFT plot is shown in Figure 19. From Figure 19, it is observed that the VAVFPWM strategy produces significant 3rd, 5th, 38th and 40th harmonic energy.

A. Simulation of ISCPDPWM Technique

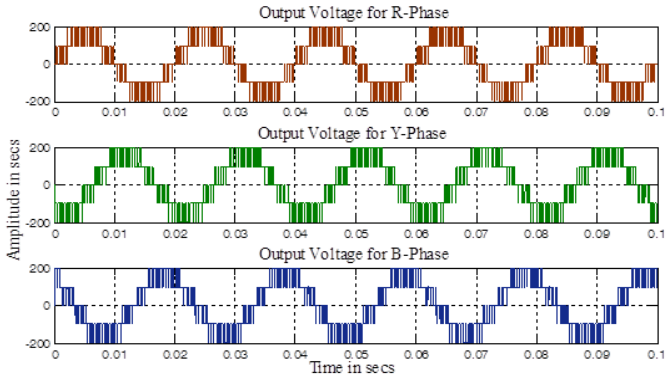

Figure 8. Simulated output voltage generated by ISCPDPWM technique for R-load

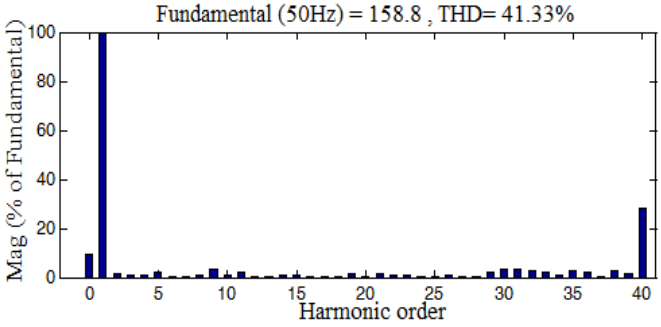

Figure 9. FFT spectrum for ISCPDPWM technique

B. Simulation of ISCAPODPWM Technique

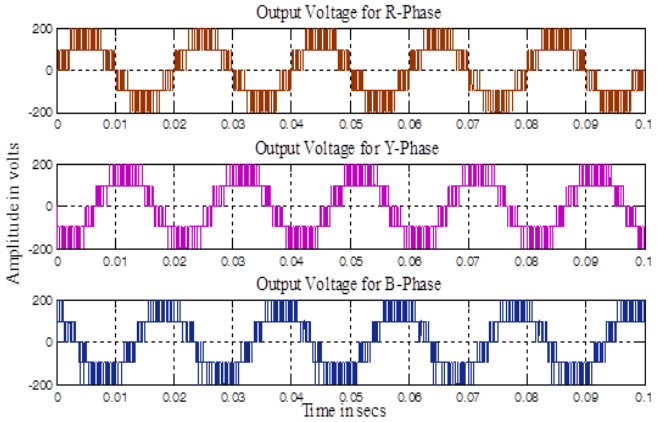

Figure 10. Simulated output voltage generated by ISCAPODPWM technique for R-load

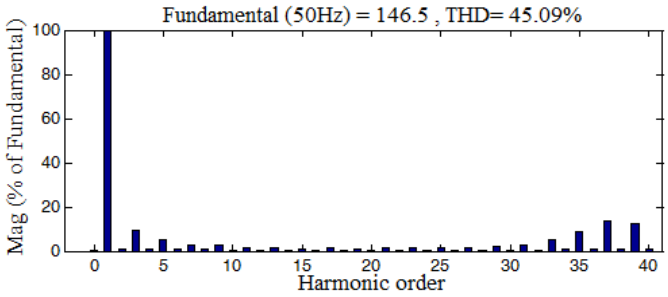

Figure 11. FFT spectrum for ISCAPODPWM technique

C. Simulation of ISCVFPWM Technique

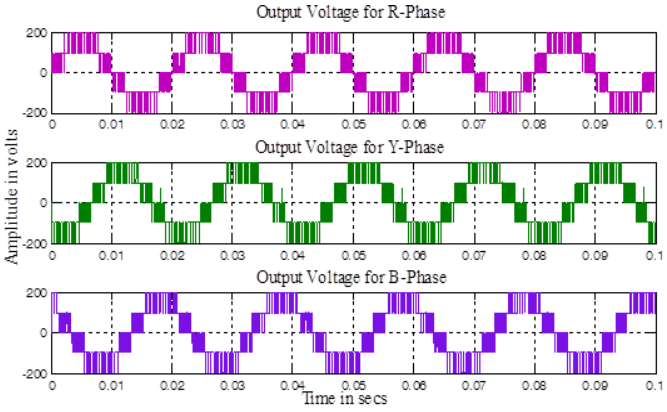

Figure 12. Simulated output voltage generated by ISCVFPWM technique for R-load

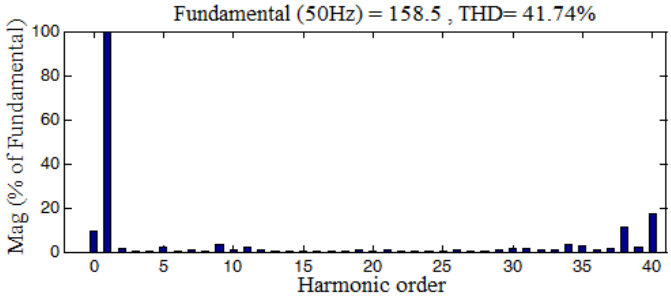

Figure 13. FFT spectrum for ISCVFPWM technique

D. Simulation of VAISCPDPWM Technique

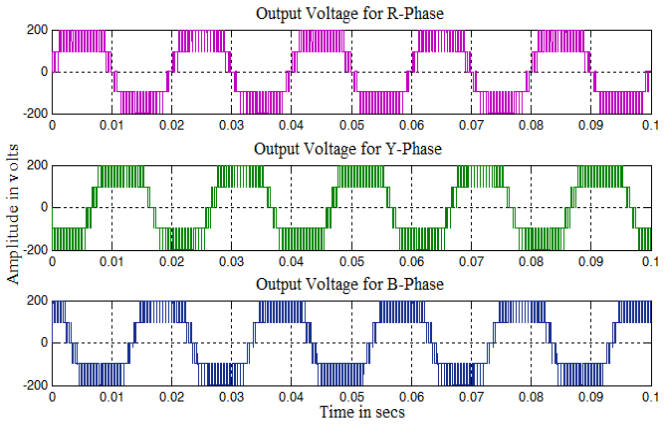

Figure 14. Simulated output voltage generated by VAISCPDPWM technique for R-load

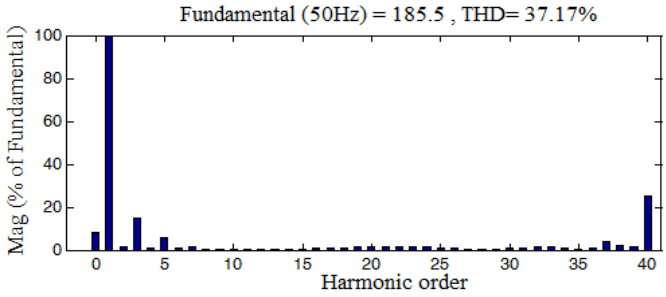

Figure 15. FFT spectrum for VAISCPDPWM technique

E. Simulation of VAISCAPODPWM technique

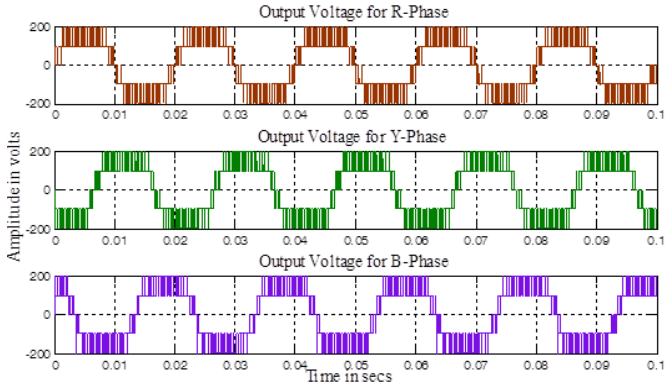

Figure 16. Simulated output voltage generated by VAISCAPODPWM technique for R-load

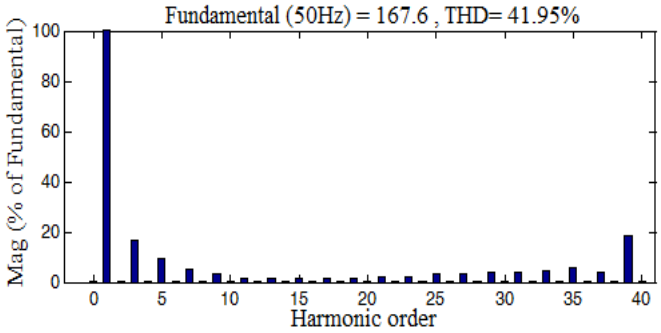

Figure 17. FFT spectrum for VAISCAPODPWM technique

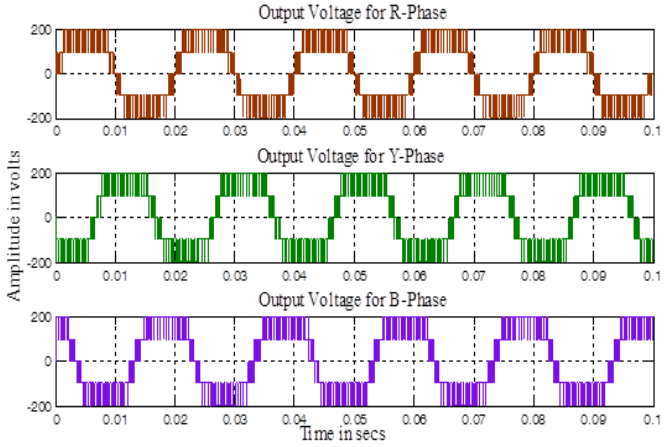

Figure 18. Simulated output voltage generated by VAISCVFPWM technique for R-load

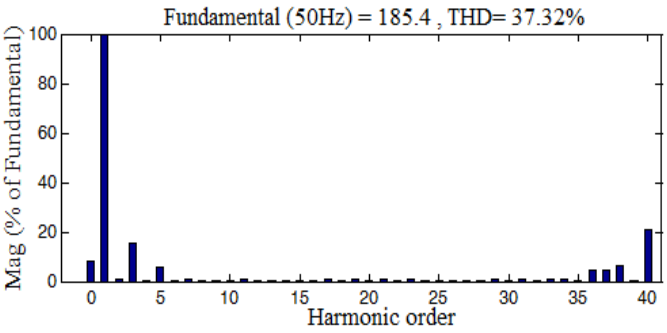

Figure 19. FFT spectrum for VAISCVFPWM technique

Table 3. % THD of output voltage (R-phase) of choosen hybrid H-bridge MLI for various values of m_a with sine reference

%THD	m_a				
	1.0	0.9	0.8	0.7	0.6
ISCPD	33.62	42.57	41.33	42.83	51.18
VAISCPD	30.95	35.25	37.17	38.84	40.41
ISCAPOD	40.18	47.70	45.09	43.59	49.43
VAISCAPOD	35.17	42.79	41.95	45.38	48.24
ISCVF	36.33	42.40	41.74	42.53	51.10
VAISCVF	30.69	35.05	37.33	38.90	39.81

Table 4. V_{RMS} (fundamental) of output voltage (R-phase) of choosen hybrid H-bridge MLI for various values of m_a with sine reference

V_{RMS}	m_a				
	1.0	0.9	0.8	0.7	0.6
ISCPD	137.7	124.0	112.3	99.33	85.2
VAISCPD	148.8	139.3	131.2	123.3	115.3
ISCAPOD	130.0	114.7	103.6	93.71	84.24
VAISCAPOD	139.8	127.6	118.5	111.8	104.10
ISCVF	137.4	124.2	112.0	99.38	85.23
VAISCVF	148.6	138.9	131.1	123.6	115.7

Table 5. FF of output voltage (R-phase) of choosen hybrid H-bridge MLI for various values of m_a with sine reference

FF	m_a				
	1.0	0.9	0.8	0.7	0.6
ISCPD	20.737	13.762	11.808	9.92	7.738
VAISCPD	25.52	19.347	16.607	14.437	13.102
ISCAPOD	265.30	157.12	280.0	3123.6	240.68
VAISCAPOD	998.57	425.33	INF	399.28	281.35
ISCVF	19.76	14.210	11.839	10.140	7.76
VAISCVF	26.488	19.26	16.265	14.74	13.22

Table 6. CF (fundamental) of output voltage (R-phase) of choosen hybrid H-bridge MLI for various values of m_a with sine reference

CF	m_a				
	1.0	0.9	0.8	0.7	0.6
ISCPD	1.4139	1.4137	1.4140	1.4144	1.4143
VAISCPD	1.4139	1.4134	1.4138	1.4144	1.4145
ISCAPOD	1.4138	1.4141	1.4140	1.4139	1.4138
VAISCAPOD	1.4141	1.4145	1.4143	1.4141	1.4140
ISCVF	1.4148	1.4138	1.4151	1.4147	1.4138
VAISCVF	1.4138	1.4139	1.4141	1.4134	1.4148

Table 7. DF of output voltage (R-phase) of choosen hybrid H-bridge MLI for various values of m_a with sine reference

DF	m_a				
	1.0	0.9	0.8	0.7	0.6
ISCPD	0.5586	0.17	0.3654	0.2782	0.6866
VAISCPD	1.5764	1.7236	1.7305	1.6713	1.633
ISCAPOD	0.4727	0.7454	1.0762	1.109	1.2722
VAISCAPOD	1.2565	1.6692	1.8779	2.0131	2.1278
ISCVF	0.6234	0.2139	0.4059	0.2876	0.6143
VAISCVF	1.5663	1.688	1.7167	1.6622	1.6375

6. Conclusion

From the simulation results, several features of the proposed modulation strategy from the aspect of phase voltage have been identified. The line voltage yields better spectral performance for ISCPWM compared to the conventional PWM. This method results harmonics decreases as the number of levels increase, less number of switches and cost of the converter. Among the different carrier-based methods the measures %THD, V_{RMS}, CF, FF and DF have been studied from converter performances. By employing this new technique it has been proved that the fundamental voltage is improved. In addition to this, switching losses and THD are also lower compared to the conventional PWM technique. By increasing the number of steps, waveform approaches the desired sinusoidal shape and THD is reduced. The conventional

PWM strategies are ISCPD, ISCAPOD, ISCVF and the variable amplitude PWM strategies are are VAISCPD, VAISCAPOD, VAISCVF. By comparing with conventional PWM strategies, it is observed that the chosen modified hybrid H-bridge multilevel inverter produces the less total harmonic distortion and recognized that VAISCVF strategy provides output with relatively low distortion for all strategies. It is also seen that VAISCPD is found to perform better for all strategies since it provides relatively higher fundamental RMS output voltage. Table 3 and 4 shows the total harmonic distortion and RMS for all chosen modulating indices. Table 5 displays form factor for all modulating indices. Tables 6 and 7 display the crest and distortion factor for all chosen modulating indices.

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