Indonesian Journal of Electrical Engineering and Computer Science
Vol. 26, No. 1, April 2022, pp. 253~260
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v26.i1.pp253-260

Datasets design of gate diffusion input based pipeline architecture for numerically controlled oscillator

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Article Info

Article history:

Received Sep 6, 2021
Revised Feb 1, 2022
Accepted Feb 10, 2022

Keywords:

32-bit counter
Coherent control
Gate diffusion input
Index compute
Look up table
Numerically controlled oscillator
Phase separation

ABSTRACT

Gate diffusion input (GDI) is a technique, which enables reducing power consumption, area and delay in the digital circuits significantly, at the same time maintains low complexity of the logical design. This paper focuses on the analysis and interpretation of the design and implementation of GDI-based pipeline architecture for numerically controlled oscillator (NCO) using look up table (LUT). Based on the input signal and the alternate signal, this phase separation will separate the phase difference signal. The NCO generates a frequency and phase harmonized output signal with an antecedence fixed frequency clock. The 32-bit counter then compares the current count to the value stored in the compare register. Here the Coherent control comes into picture. It controls the carrier synchronizer by employing data from the 32-bit counter and the obtained data will be saved. It is updated and advanced using the third peer group of frequency synthesis technology. The test outcomes are accompanied with the theoretical concept and reproduced the results. The main objective of GDI-based pipeline architecture for NCO using LUT is to reduce the usage of metal oxide semiconductor field effect transistors (MOSFET's). NCO is an indispensable component in many digital communication systems linked to modems, software-defined radios, and digital radio, digital down/upconverters for cellular and personal communications service base stations.

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1. INTRODUCTION

Numerically controlled oscillator (NCO) is a digitally functioned signal generator, which is directed as an immediately advanced synthesizer. As compared with the conventional strategies, NCO offers numerous advantages, including a massive output relative transmission capacity, fine recurrence goal, and rapid tuning capability. In addition to this, NCO has two deficiencies such as large yield prod and tight yield transmission capacity [1]. Earlier, as a significant part of the computerized correspondence frameworks, NCO was being generally utilized and investigated. There are two concerns to be fathomed, together with the

time frame and area. The resources of FPGA are restricted i.e. the entire setup in the NCO is the accuracy mode whose sizes have an incredible connection with false presentation. The advantages of NCO over other types of oscillators reflect in terms of quickness, authenticity, stability, and accuracy. To diminish the deceptive signs of NCO, the pieces of the stage aggregator and the width of the accuracy table should be considered under the circumstances. Concurring the sine wave signal and out phase cosine wave evenness, quarter-wave balance can be abused to bring about more asset proficient execution [2].

The waveform stage is exceptionally significant in fast remote applications like radar, media transmission frameworks, instrumentation, and numerous different fields.The principal waveform generators utilized the direct analog synthesizers (DAS). The synthesizer is obtained by adding frequencies from non-linear oscillations and sounds. The most widely usedbasic waveform synthesizers utilize the stage identifier, a numerically controlled oscillator, a simple phase-locked loop (PLL) [3], [4]. These simple waveform synthesizers had average exchanging time with weak recurrence goal, less adaptability, and less flexibility. In present days field programmable gate arrays (FPGAs) are quite well known for accomplishmentof advanced circuits because of an ideal opportunity to advertise, simple for programming at the customer level contrasted with application-specific integrated circuit (ASIC). So, the usage of the oscillators on FPGA makes the gadget exceptionally productive. In addition, the principal center was around the age of the sine wave just yet various waveform ages will expand the district of use. Very high-speed hardware description language (VHDL), hardware description language is commonly utilized. Numerically controlled oscillator was constructed for utilizing read-only memory (ROM) with tests a sine wave spared in it sine look up table (LUT) [5]. Coordinate rotation digital computer (CORDIC) algorithm is an improved, very powerful and efficient algorithm, that produces one extra bit of accuracy for each iteration [6]. Direct digital synthesis (DDS) in light of numerically controlled oscillators is the most predicted strategy for generating semi periodic sinusoidal signals whenever a high recurrence goal, quick changes in recurrence, and stage with high otherworldly virtue of the output signals are required [7]. The representation of NCO in sign quality and stability when contrasted with different strategies, e.g: voltage-controlled oscillators (VCO) by significant equipment multifaceted nature and a recurrence limit by Nyquist hypothesis.

Figure 1 represents the basic block diagram of NCO having four blocks for signal generation. The NCO proceeds with signals at a specific recurrence control word, which decides the stage of operation [8]. When it is set, then it determines the sign of recurrence to be delivered. Stage gatherer yield consistently has appropriate parallel words speaking to the moment stage to look into table capacity.

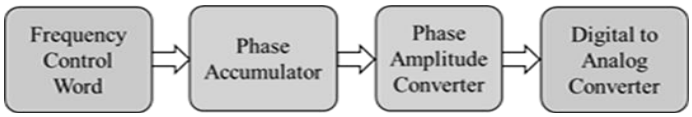

Figure 1. Basic bock diagram of a NCO for signal geneatation with frequency control word text box

The NCO will comprise of stage gatherer and stage to abundance converter [9]. This stage converter is actually LUT, which converts phase to amplitude. Using the complementary metal oxide of semiconductors, all the digital and analog designs can be fabricated. Apart from this, it organizes a ring oscillator associated with a circle from the remainder of that yield stage and is given to the first stage's contribution. The ring oscillators have been intended for various stages. Because of different preferences, complementary metal oxide semiconductor (CMOS) innovation is broadly utilized in business applications [10]. Dependability is another remarkable boundary parameter that is likewise required for planning of low force circuit. The incremental functions are performed with a straightforward CORDIC extension [11]. In this vast, majority of the computerized and electronic frameworks show oscillatory conduct. Oscillators have now gotten the most significant of every advanced segment, the optical gadgets of a correspondence framework [12]. Size of the electronic gadgets is diminished enormously after the presentation of the incorporated circuit of the innovation.

While structuring any collaborative innovation and incorporated chip, planners need to deal with specific boundaries. They are power utilization, speed, silicon territory, and the ring oscillator's delay is a shunt circle. The circuit must fulfill the Barkhausen criterion, which measures to give the oscillation and support the circuits to increase the voltage [13]. It must have the move around a stage of 2π. The DC reversal gives π stage move; the move of residual stage π is separated similarly among the phases in the ring oscillator. So, each postponement provides stage deferral of π/N, where N is referred as the number of several stages in an oscillator.

2. STATE OF THE ART

Ireneusz Janiszewski, Bernhard Hoppe, and Hermann Meuth proposed a crossbreed work for the generation of sine wave with high-accuracy NCOs, which joins conventional LUTs iterative methods of the CORDIC calculation. This paper results with SNR of 92 dB with a word length of 16-bits. Gopal D. Ghiwala, Pinakin P. Thaker, Gireeja D. Amin proposed the reenactment and combination of signal generation with numerical control. The design and realization of numeric control basic oscillator incorporate phase accumulator and a look-up table. In this paper proposed framework is a plan for yield recurrence of 2.5 MHz with 24 bits word length. Snehal Gaikwad, Kunal Dekate suggested direct digital synthesizer is done at clock recurrence, which is determined as a standardizing esteem comparative with clock rate given. A double oscillator subsequently upholds the variable width, phase tweak and client characterized recurrence goal with 5 MHz yield recurrence. Matt Bergeron and Alan N. Willson proposed engineering technique that utilized a point pivot calculation. This calculation was being used for the stage to quantify the change. The design used a stage collector of 32 cycles, and the clock frequency is 1 GHz, which gives a yield recurrence of 400 MHz on Xilinx Virtex rendition 7 FPGA.

The size of electronic gadgets has been extraordinarily diminished after the presentation of the incorporated circuit innovation. While structuring any coordinated chip, architects need to deal with specific some boundaries such as power utilization, speed, and silicon regions. The invention of corresponding metal oxide semiconductors is broadly utilized to develop the coordinated circuits, as CMOS circuits give very low power utilization and littler area. To actualize any advanced circuit like CMOS, metal oxide semiconductor field effect transistor (MOSFET), and N-type and P-Type transistors are utilized. As a result of the different favorable circumstances, CMOS innovation is broadly used in various business applications. Unwavering quality is another significant boundary that is likewise required for structuring a low power circuit.

In this generation, the vast majority of the advanced electronic frameworks show oscillatory conduct. Oscillators have now become the most significant gadgets of all advanced, correspondence frameworks of entire sight. The CMOS will control the recurrence of yield [14]. A numerically controlled oscillator is a shut circle circuit comprising phases of various odd inverters indistinguishable, a circuit of shaping criticism [14]. The last phase of yield from the criticism is equivalent to the information motions which are wanted. To begin the activities, it needs just flexibility of vitality, and then after that, it works all alone. Furthermore, the swaying of recurrence can be changed either by providing the voltage to the phases of number. The scaling recurrence is another significant factor in oscillators of low vitality PCs of versatility. The numerically controlled oscillator is concocted by utilizing the plans of chip systems as they possess the territory of fewer chips [15]-[17].

It can produce the two sources of information and the yields of unmistakable quadrature. In any case, the exhibition of the particular clamor of the ring is inadequate because of the nature of the low factor. The oscillating signals are seen in electrical systems of different types. An oscillating signal can be used as a clock signal to synchronize the digital electronic system of an operation. The signals are used in the communication systems of radio and data transmission. Electronic oscillators are designed to create these signals to process data in communication and real-time systems linear/harmonic and non-linear/relaxation models are basic types of oscillators used in communication [18]-[20].

A relaxation oscillator is a type of numerically controlled oscillator that contains several odd inverters creating alternating between low & high voltage of the non-sinusoidal signal [21]. The last inverter's output is connected to the first inverter, there comes the name "ring" oscillator from this detail. Numerically controllable oscillators are attractive for many reasons, including their simple low operating voltage [22]. The last reason is quite essential i.e., by lowering the clock signal's power consumption, the whole digital energy consumption system can be reduced. Changing the voltage supply can vary the power of a numerically controllable oscillator, although this will change the circuit frequency. The designs of very-large-scale integration are widely used because of their high performance and need to manufacture even smaller designs [23]. Hence, the optimizing scale designs of nanometers for the trade-off between the solution's performances in the integrated circuits. The initial voltage should be low and maintain the propagation at a low power supply to the NCO module to generate a sine wave at any desired frequency [24], [25].

3. NUMERICALLY CONTROLLED OSCILLATOR CONCEPTUAL STRUCTURE

To understand the operation of numerically controllable oscillator, first all should understand the delay of the gate, which is shown in Figure 2. In the device, no gate can switch at once on the physical design. CMOS is a device that consists of several transistors. For example, before the current flow will be between the drain and source, the gate must be charged with the capacitance. After the input has changed, the inverter of every output in the numerically controllable oscillator will change the amount of finite time. It is seen that more inverters increase the gate of total delay, and it reduces the oscillation frequency [7]-[9]. The time delay of the numerically controlled oscillator is an oscillator member. The amplifier input, output with the delay element, the

inverting amplifier consists of a time-delay oscillator. At the intended oscillation frequency, the amplifier must gain greater than 1. We should consider the initial phase, where the amplifier's voltage is momentarily balanced at a stable point by the input and output. Figure 2 shows the conceptual structure of a numerically controlled oscillator. A wide range of frequencies with periodic output nature signals will be generated with NCOs at very low power. Phase lag signal was considered herein and expressed in (1).

$$Y\,[n]\; =\; cos\,(\varphi[n]) \tag{1}$$

$$\varphi[n]\; =\; 2\pi f0n\; +\; \theta 0 \tag{2}$$

$$y[n]\; =\; cos\,(2\pi f0n\; +\; \theta 0) \tag{3}$$

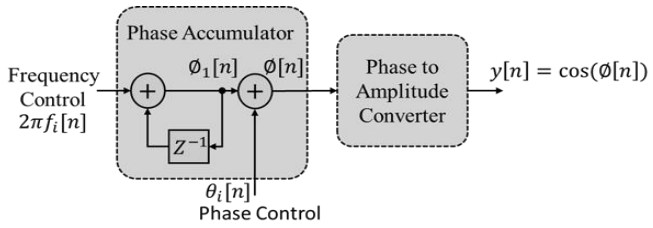

Figure 2. Numerically controlled conceptual oscillator structure

However, suppose the frequency of the signal and its phase are changing with n. In that case, the instantaneous frequency fi[n] provides the increment for φ[n] to overcome the change, which must be accumulated over time. For the nth sample, the instantaneous phase offset θi[n] provides an offset value to the limit range:

$$\varphi 1[n]\; =\; \varphi 1[n\; -\; 1]\; +\; 2\pi fi[n] \tag{4}$$

$$\varphi[n]\; =\; \varphi 1[n]\; +\; \theta i[n] \tag{5}$$

the amplifier raises the noise in a small amount. The lower output voltage signal change will be dispensed to the input amplifier after passing through the delay elements of this time. The negative gain should be greater than 1 of the amplifiers, and the output will be in the opposite direction to the input voltage. The more considerable amount of the input value will change, and it is greater than 1. The amplified and the reversed signal should widely spread from the time delay through the output. It will be input back and then amplified, and inverted are again. In the sequential loop, the wave signal is a square, and the amplifier output result with each square wave of the equal half period with the bounded time delay. It will grow until the amplifier of voltage output reaches its specified limits, and then stabilize the square wave. The wave grows from exact analysis noise; it will show that the initial and the square may not succeed. As the amplifier reaches its output limits, it will become square. Another version of the oscillator delay is the numerically controlled oscillator. The numerically controllable oscillator uses the number of odd inverters, the single amplifier effect of an inverting greater is than one. Hence the name numerically controlled oscillator is having a delay rather than the single element.

It contributes to the inverter of each signal of the ring of inverters of the delay cells. Adding the numerically controllable oscillator pair increases the inverters of delay cells total, the frequency decreases the oscillator. The changes in each inverter delay's supply voltage will reduce the typical higher voltage and increase the delay oscillator frequency. The Bratislava of frequency stability has described some methods that improves the consumption of power. The included numerically controllable oscillator has the quantity of postponing stages, with the last step and the yield is taken care of going into the main info. This voltage-controlled oscillator of current starved by utilizing a numerically controllable oscillator is planned, and all the activities are happening like that. To the structure, there are numerous topologies of the voltage-controlled oscillator. A portion of the LC-based oscillator of the voltage-controlled oscillator. The VCO is dependent upon the numerically controlled oscillator, the relaxation oscillator is dependent upon the voltage-controlled oscillator. The power supply is a measure of the impact of various voltage variations on circuits' reactions.

According to the change, the percentage is defined by the oscillation frequency to the voltage supply. The sensitivity of supply decreases the frequency with an increase. At the higher operating frequency, the sensitivity falls below the negative to a zero value. The design of modern complementary metal-oxide

semiconductors is based on power reduction principle and the circuit design is stable. The power consumption of voltage-controlled oscillator is significantly less than the numerically controlled oscillator. The current estimation of area and the voltage-controlled oscillator are substantially less than the selected NCO.

4. GDI PIPELINE ARCHITECTURE FOR NCO USING LUT

Figure 3 shows gate diffusion input (GDI) based pipeline architecture block diagram for NCO using LUT. This phase separation will autonomous the phase difference signal based on the oscillated input signal. NCO generates a phase tunable output signal with a precision fixed-frequency clock to use in a 32-bit counter. 32-bit counter will compare the current count to the value stored in compare register. Coherent control will control the carrier synchronizer by employing data from the 32-bit counter. The index will save the obtained data after controlling.

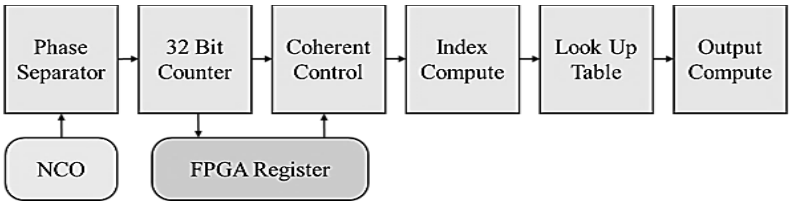

Figure 3. Block diagram of GDI-based pipeline architecture for NCO using LUT

An FPGA register is a type of memory that utilizes a progression of flip-flop to store the individual pieces of a paired word, for example, a byte (8 bits) of information. The length of the put away paired word depends on the flip-flop quantity that makes up the register. A lookup table, otherwise called LUT, is utilized in PC programming that holds esteems that would somehow to be determined. The table might be physically populated when the program is composed, or the program may populate the table with values as it figures them. Different oscillations provide the same range of frequency signal which is used in the inverter addition stages. In the process, the addition of more inverting steps leads to propagation delay rise. The oscillation frequency is added by the propagation delay through a number of process steps in GDI based pipelined architecture. The delay of propagation not acceptable to generate the particular signal, after adding few inverting stages. The power factor measurement is essential and needed to be estimated in the design of VLSI. The dissipation factor will increase in power in the circuits by adding more inverting stages.

Less frequency and a more stable signal can be produced based on complementary metal-oxide semiconductors by adding a number of delay cells. The dissipation factor is reduced, thereby using less energy. In many communication areas, the frequency is varied from gigahertz to megahertz by varying the VCO. Small frequency ranges of oscillation signals are applied explicitly. It is achieved by using voltage-controlled oscillators. Complexities in manufacturing, Dynamic mode power consumption, and noise phrases are overcome by using the system. Design of voltage controlled oscillator having ideal characteristics, provides low power consumption, high gain, and a significant improvement in frequency linearity.

Converting an input voltage into a particular frequency component for radio wireless communication systems is a main considerable element. This conversion and process can be made through a frequency selective NCO. The typical voltage-controlled frequency can be generated through two types. One is a waveform oscillator, and another one is a resonant oscillator. The voltage-controlled oscillator has control to hold the range of values. The circuitry clock output required for the design is afforded by the numerically controlled oscillator. Varying component ranges will adjust the PLL frequency filter. With the aid of an inverter, reverse osmosis is regulated by a current with similar oscillations. The proposed system is used for designing phase separation blocks. Wafers that act like line structures of tests using reverse osmosis–wafer testing manufacturing process in measuring effects during manufacturing.

5. RESULTS AND DISCUSSION

Table 1 shows a comparative analysis and the synthesis report of LUT-based NCO and CORDIC-based NCO. As compared to both it is obtained that the LUT-based NCO gives more effective results. From the below table it is certainly observed that the LUT based NCO require a smaller number of LUTs than the CORDIC based NCO, simultaneously the gate count is also less in case of LUT based NCO. The PIE Utilization of 4 inputs LUT, Slices and Gates in LUT based NCO and CORIC based NCO is shown in Figure 4.

Table 1. Synthesis report of LUT-based NCO and CORDIC based NCO

S. No	Name of the parameter	LUT based NCO	CORDIC based NCO
1	4-input LUT	300	411
2	Slices	161	239
3	Gate count	3224	4113

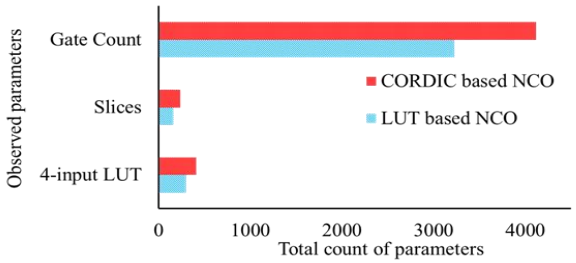

Figure 4. PIE utilization of 4 input LUT, slices, and gates in LUT based NCO and CORIC based NCO

Table 2 shows the summarized analysis of LUT-based NCO and CORDIC-based NCO. In this locking time, phase angle and tracking range values are compared with each other. But, LUT-based NCO offers a more productive output. Figure 5 shows the pictorial representation of the above table for the parameters locking time, phase angle, and tracking range of LUT-based NCO and CORDIC-based NCO, which gives a logical understanding.

Table 2. Synthesis report of LUT-based NCO and CORDIC based NCO

S. No	Name of the parameter	LUT based NCO	CORDIC based NCO
1	Locking time	11.735 us	16.975 us
2	Phase angle	53 deg.	21 deg.
3	Tracking range	~75 MHz	~64 MHz

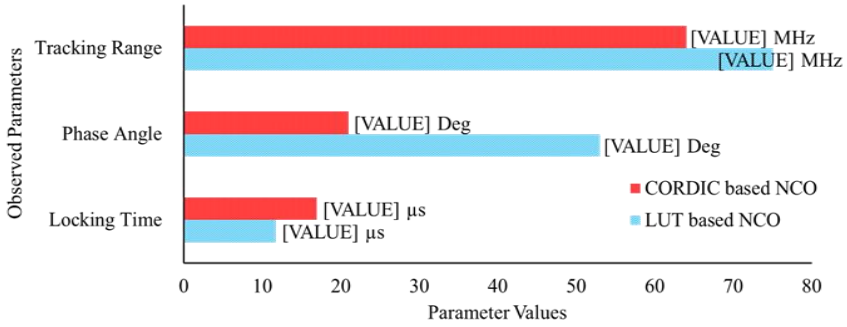

Figure 5. Locking time, phase angle, and tracking range of LUT-based NCO and CORDIC-based NCO

Table 3 shows the comparison of chip level configuration for LUT based NCO and CORDIC based NCO. Table 4 shows the Synthesis report of LUT-based NCO and CORDIC Based NCO. The parameters of voltage, mean square errors and Noise Spectrum for LUT based NCO and CORDIC based NCO are explained in Table 4.

Table 3. Synthesis report of LUT-based NCO and CORDIC based NCO

S. No	Name of the parameter	LUT based NCO	CORDIC based NCO
1	Chip area	1.7 x 1.7 mm^2	6.2 x 6.2 mm^2
2	Transistor Count	3,900	7,600
3	Power supply	+5 v	+5 v
4	Package	40-pin ceramic DIP	20-pin ceramic DIP
5	Power consumption	850 mW @700 MHz	920 mW @800 MHz
6	Maximum clock rate	700 MHz	900 MHz

Table 4. Synthesis report of LUT-based NCO and CORDIC based NCO

S. No	Name of the parameter	LUT based NCO	CORDIC based NCO
1	Voltage	1.2 V	1.45 V
2	Mean square errors	Errors are very less	More errors are obtained
3	Noise spectrum	Less noise is obtained	High noise is obtained

6. CONCLUSION

The article investigates both LUT based NCO and CORDIC based NCO in terms of their productivity and parameters. Various parameters are examined, and it is experimentally obtained that effective response can be realized through LUT-based NCO. Relevant parameters are studied, which are shown in the results. The numeric input clock range used in 700 MHz, is the maximum reported by the GDI NCO chip. NCO is digital and results at high resolution, tunable to various ranges of frequencies along with open-loop control linearization results. Digital methods are suitable along with an analog approach. Locking angle, phase angle, power consumption, and tracking range parameters are less in LUT-based NCO models. Advanced techniques with good circuit design can conjunction with GDI technology, and an NCO model device with clock rates of more than 1 GHz is indeed possible for high-end applications. All these investigations and analysis verified the productivity and constructive capability of the LUT based NCO over the CORDIC based NCO. In future LUT based NCO can be extended by using 19nm GDI technology and fin field-effect transistor (FINFET) technology.

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