Indonesian Journal of Electrical Engineering and Computer Science
Vol. 26, No. 2, May 2022, pp. 667~674
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v26.i2.pp667-674

Multi-level inverter with novel carrier pulse width modulation technique for high voltage applications

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Article Info

Article history:

Received Sep 15, 2021
Revised Feb 12, 2022
Accepted Mar 13, 2022

Keywords:

Cascaded full-bridge inverter
Current
PO-LSPWM techniques
Total harmonic distortion
Voltage

ABSTRACT

The present work deals with multilevel inverters (MLI) with modified carrier pulse width modulation technique and its application, especially in solar-based applications due to its modularity in structure and suitability for medium or high-power applications. Several multilevel inverters are introduced for various applications. One of the drawbacks of these inverters is high total harmonic distortion (THD) value in the output which impacts the power quality. The main objective of this work is to improve the power quality, thereby increasing the life and performance of the overall system at the consumer side. The most popular and compact cascaded multilevel DC-link inverter (CMDCLI) is considered for study and employed for 11-level operation. In general, sinusoidal pulse width modulation (SPWM) technique is used for control of inverter. However, the present work proposes a modified carrier-based hybrid pulse width modulation (HPWM) technique and has been tested with CMLDCLI. This novel technique compares the THD performance results with normal carrier wave considering R-L load. The results are analyzed in MATLAB environment and are validated with experimental results.

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1. INTRODUCTION

In the recent decade, the power quality plays a vital role in determining the performance of various industrial and domestic applications. In this regard, integration of renewable energy sources with power electronic converters poses a major challenge in terms of reduced fundamental component and total harmonic distortion of the output voltage and current. The multilevel inverter converts dc voltage to variable ac voltage with multilevel output. A study of solar photovoltaic inverter system with different improved switching strategies are introduced in [1] at 10 kHz switching frequency. The improved inverter switching performance by muti reference and dual-carrier pulse width modulation (PWM) technique which results in lower fundamental component at the output when compared with multi-reference phase opposition-level shifted sinusoidal pulse width modulation (PO-LSPWM) technique [2]. The effect of modified carrier sinusoidal pulse width modulation (SPWM) techniques is reported in [3] consisting more number of carrier waves and need of expensive magnetic coupled transformer. A study of the selective harmonic method is reported in [4] consisting of asymmetrical voltage sources with high modulation index in order to obtain improved fundamental output component. Numerous PWM techniques and topologies are introduced in [5]–[12].

Observations on different shapes of carrier waves for PO-SPWM are introduced in reference [13] for a five-level cascaded inverter. Analysis of modified design and different over modulated SPWM and trapezoidal pulse width modulation (TPWM) techniques are reported for high voltage and lower total harmonic distortions (THD) in [14] for seven level operation. The effect of mitigation of harmonics using SPWM and SHE techniques for R-load in [15], to improve the inverter performance for 11-level inverter at 10 kHz and 50 Hz. A vast area of research has been reported in references [16]–[29] for MLI. Implementation of a hybrid PWM technique having a combination of normal PD-SPWM and fuzzy controller for level and polarity generation respectively in [16], [17] for 11-level cascaded multilevel DC-link (CMLDCL) inverter and obtained better output performance. However, the drawback is the lower fundamental component of output voltage and THD is poor. In order to overcome this limitation, the proposed work employs novel triangular carrier wave in PD-SPWM to obtain improved performance than that of references [17], [18] given in Table 3. Section 1 discusses design and switching sequence of single phase 11-level MLDCL inverter, sections 3 and 4 discusses the novel carrier PWM technique and its simulation results for 11-level multilevel DC-Link inverter (MLDCLI) at modulation index of 0.888, at 10 kHz switching frequency with R=100 Ω and L=30mH load.

2. PWM TECHNIQUE

2.1. Single phase 11 MLDCLI topology

The modified 11-level CMDCLI is shown in Figure 1, which consists of supply voltages are V_1, V_2 V_3, V_4, V_5 with the same voltage (V). It consists of nine Metal oxide semiconductor field effect transistor (MOSFET) switches, five diodes with RL load at mi= 0.888, carrier frequency 10 kHz. The topology is better in terms of reduced switch count, but requires more number of input dc sources compared to conventional cascaded 11-MLI. The switching action is performed by the novel carrier shape 1 PD-LSPWM technique for level generation and fuzzy logic control technique for polarity generation as shown in Figure 2. The switching sequence is given in Table 1, consting of level generation and polarity generation.

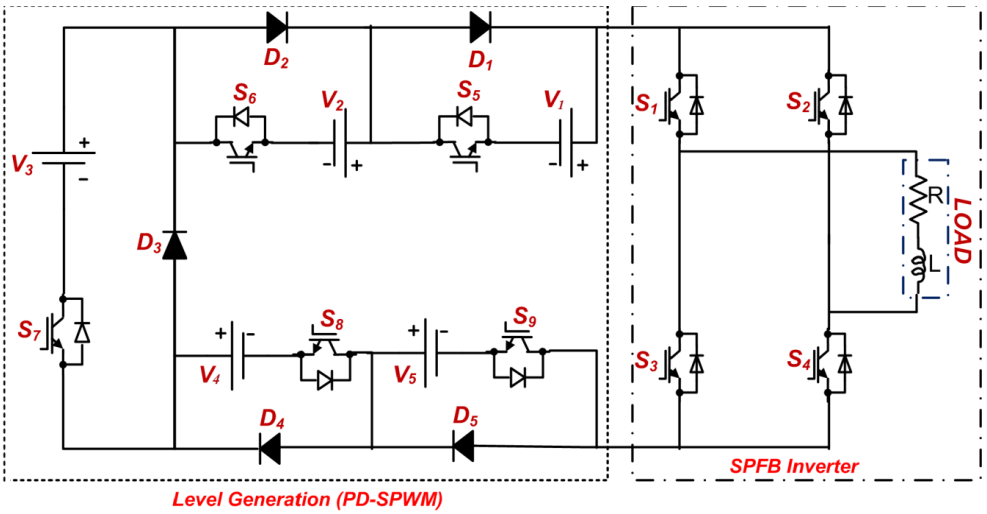


Figure 1. Modified 11-level CMLDCL inverter

The paper mainly focusses on improvement of the conversion efficiency of modified 11-level CMDCL inverter by using a novel triangular carrier shape in the PD-LSPWM technique. For level generation, switches S5, S6, S7, S8 and S9 are operated whereas for polarity SFBI is giving output shown in Figure 1. The control of SPFBI has switching action of (S1, S2, S3, and S4). The work presents novel triangular carrier shape in PD-SPWM along with fuzzy logic control technique to reduce the harmonic distortion at output voltage and to increase the magnitude of the output voltage at a modulation index of 0.888, and switching frequency 10 kHz.

Table 1. Switching table for 11-levels MLI

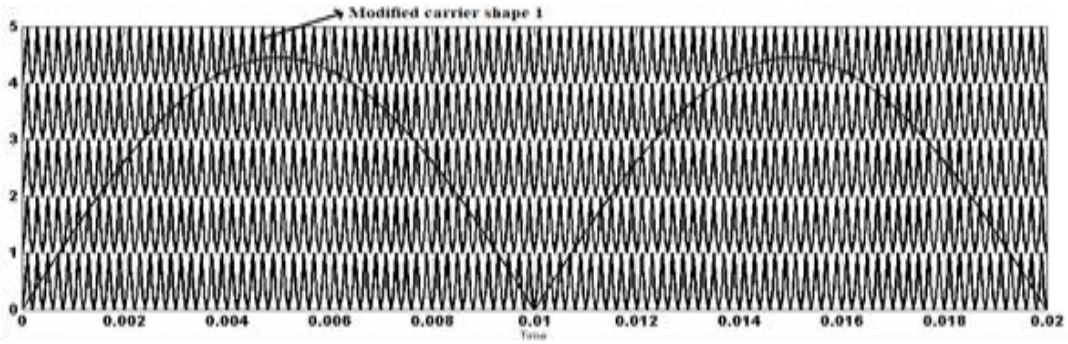
for level generation						for polarity generation				
Voltage level	S5	S6	S7	S8	S9	Voltage level	S1	S2	S3	S4
0	0	0	0	0	0	Vdc	1	1	0	0
V1	1	0	0	0	0	0	0	0	0	0
V1+V2	1	1	0	0	0	-Vdc	0	0	1	1
V1+V2+V3	1	1	1	0	0					
V1+V2+V3+V4	1	1	1	1	0					
V1+V2+V3+V4+V5	1	1	1	1	1					

3. PROPOSED NOVEL HPWM TECHNIQUE

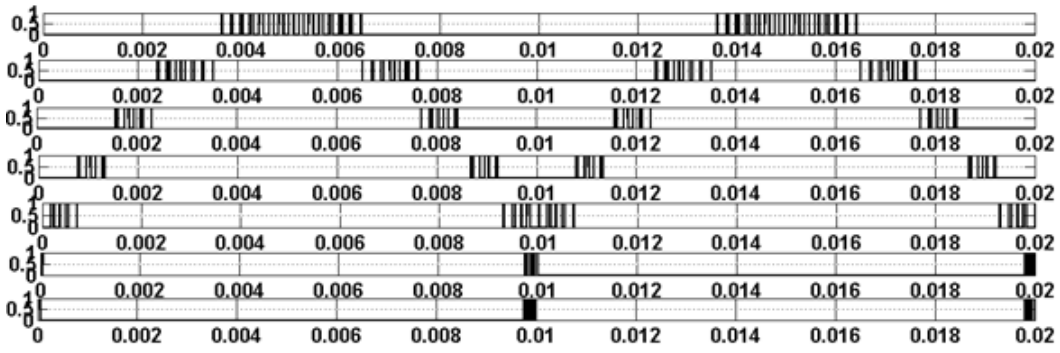
The proposed novel hybrid pulse width modulation (HPWM) is a combination of PD-SPWM and fuzzy logic control techniques. Where PD-SPWM technique is for level generation. Its working is similar to that of normal SPWM technique with improved performance of output voltage. The only difference is novel triangular carrier wave generation and its performance. The second stage fuzzy controller is applied at polarity generation to reduce the harmonics in the obtained output voltage of the novel carrier PD-SPWM technique.

3.1. Triangular carrier shape 1

This paper presents the novel carrier wave generation by the PD-SPWM technique. The carrier wave generation is explained by Figure 2. Modified carrier shape 1 PD-SPWM technique with five carrier waves, one reference wave in Figures 2(a) and 2(b) pulses generation are shown. Figure 3(a) depicts the zoomed version of fifth carrier shape 1, Figure 3(b): (i), (ii), (iii), and (iv) gives the description of carrier waves at different values of d, D distances. In Figure 3(b): (i) d=0.5, D=0.5 (conventional), (ii) d=0.75, D=0.25 (proposed), (iii) d=0.885, D=0.115, and (iv) d=1, D=0 respectly. The analysis is carried in such a way that the pulse widths are generated such that the simulation of Figure 3(b), (ii) at d=0.75, D=0.25 is able to achieve better output voltage and output current than the conventional one. Where d is the distance between d_(1) and d_(2), D is the distance between d_(2) and d_(3). The simulation and the FFT Spectrum results are depicted in Figure 4.



(a)



(b)

Figure 2. SPWM technique for modified 11-level CMLDCL inverter for (a) modified carrier shape 1 PD-SPWM technique with six carriers, one reference and (b) pulses generation

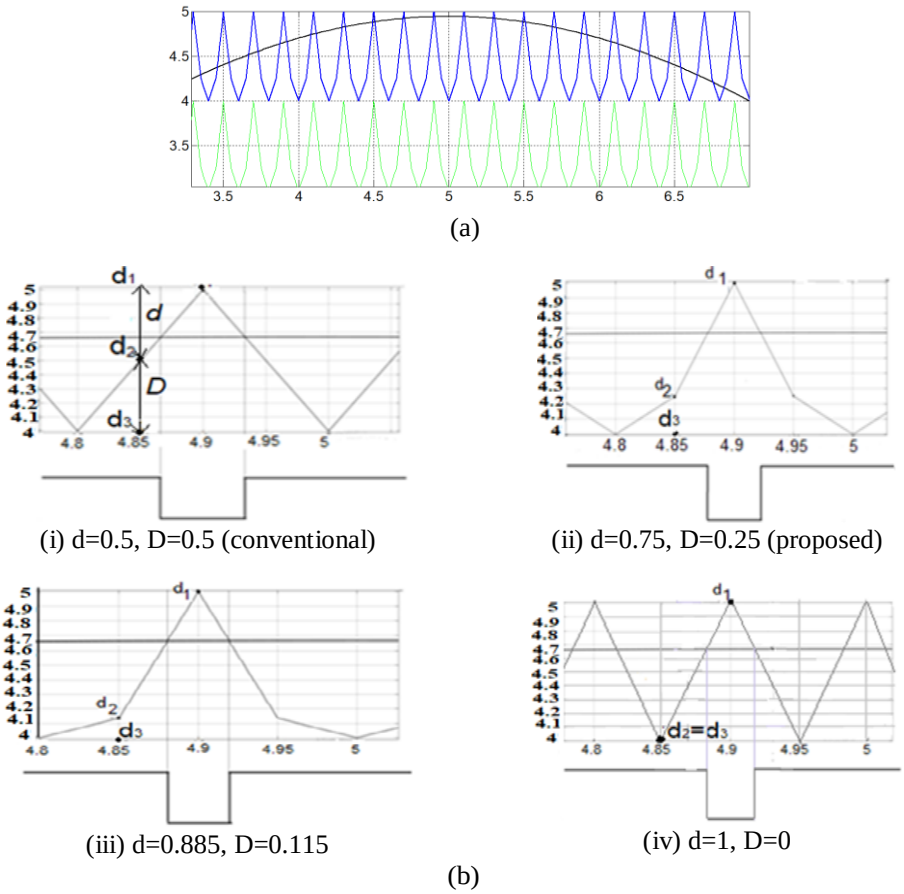


Figure 3. Modified 11-level CMLDCL inverter using novel PWM technique: (a) view the zoom of fifth carrier shape 1 and (b) explanation of carrier wave at different d, D distances shown in (i), (ii), (iii), and (iv)

3.2. Fuzzy logic

Fuzzy logic refers to the process of converting an input space into an output space through the use of conditional or rule-based logic for polarity generation of the sine wave. It can be achieved by using the fuzzy logic controller which maintains the modulation index of the PWM based multilevel inverter on the input side signals, the voltage error, and its rate of change. The signals which are given as input are fuzzified, that is they are characterized by a set of linguistic labels by their membership functions.

3.2.1. Working of FLC

In the fuzzy logic system, the fuzzy logic controller is responsible for determining the fuzzy rules that govern its operation. The fuzzy logic controller (FLC) system takes as inputs error (E) and error change (dE), as depicted in the following figure. The fuzzy logic controller's output is determined solely by the rules set by the designer, and the controller does the rest. By doing this we can obtain the desired output. Fuzzy logic system rules are as follows in Table 2 [17].

Table 2. Fuzzy rules for this hybrid controller

	NVB	NVM	NVS	ZVE	PVS	PVM	PVB
NVB	NVB	NVB	NVB	NVB	NVM	NVS	ZVE
NVM	NVB	NVB	NVB	NVM	NVS	ZVE	PVS
NVS	NVB	NVB	NVM	NVS	ZVE	PVS	PVM
ZVE	NVB	NVM	NVS	ZVE	PVS	PVM	PVB
PVS	NVM	NVS	ZVE	PVS	PVM	PVB	PVB
PVM	ZVS	ZVE	PVS	PVM	PVB	PVB	PVB
PVB	ZVE	PVS	PVM	PVB	PVB	PVB	PVB

4. RESULTS AND DISCUSSION

Simulation results for 11 multilevel inverter DC links are shown in Figure 4 for modified 11-level CMLDCL inverter using modified carrier shape 1 PD-SPWM technique: (a) output-voltage FFT before filter, (b) output-voltage and FFT after filter for single phase, and (c) output current and FFT for before filter. The simulation results are improved when compared with the references [17], [18]. Table 3 gives the comparison of the results for carrier waves of 11 level CMLDCL inverter. Modulation Index at 0.8888 is giving better results for both existing and novel hybrid PWM techniques with carrier shape 1 is giving better fundamental FFT analysis of output voltage and current waveforms i.e., for novel carrier shape 1 obtain better waveforms of output voltage and current, as well as FFT analysis i.e., before filter output voltage as 494.5 V, 10.37% THD, current as 4.25 A, 1.86%. After filter output voltage as 490.4 V, 3.27%, current 4.922A, 1.75% and is improved than the conventional PD SPWM technique in reference paper [17], i.e., before filter output voltage as 444.6 V, 14.17% THD, current as 4.425 A, 1.86%. After filter output voltage as 440.8 V, 3.27%. It can be noticed for carrier input 1, its giving better fundamental component voltage and current values than other carrier waveforms. The comparison results at the index at 0.88 carrier shape 1 gives better performance with respect to fundamental output value than conventional one. Table 3 gives the comparison of results for RL load with the proposed method for modified cascaded 11 level DC link inverter before filter and after the filter. The inverter control has been performed by normal carrier hybrid pulse width modulation (combination of Phase disposition SPWM technique at level generation and fuzzy controller at polarity generation) for 11-levels as discussed in in reference paper [17]. The drawback is the lower output voltage and high THDs. To overcome this, the present work improves the fundamental component quantity (output value) and quality (%THD) are by using modified carrier hybrid pulse width modulation. The results are analyzed in MATLAB/Simulink environment.

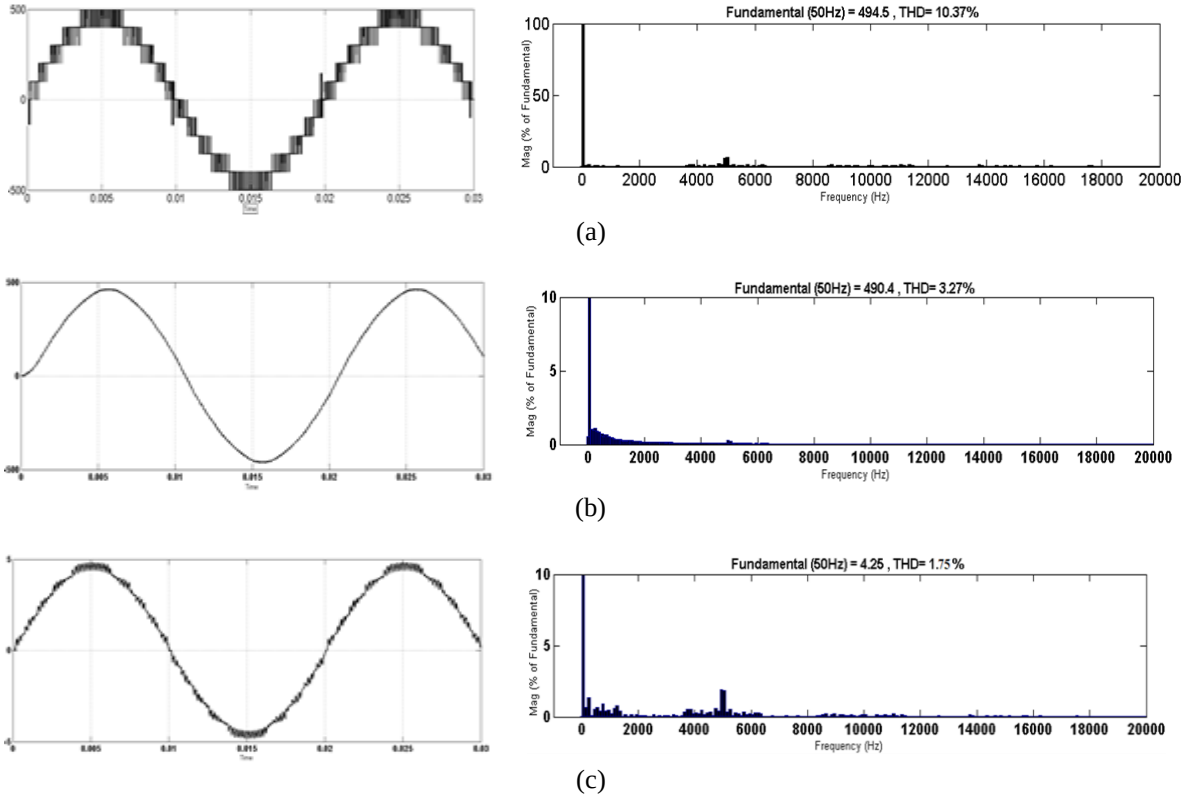


Figure 4. Simulation of modified 11-level CMLDCL inverterusing modified carrier shape 1 PD-SPWM technique: (a) output-voltage FFT before filter, (b) output-voltage and FFTafter filter for single phase, and (c) output current and FFT for before filter

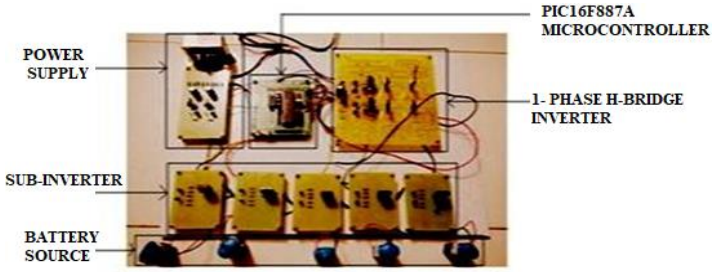
From Table 3 the observations concluded that the modified carrier shape 1 of hybrid pulse width modulation gives better output voltage and THD when compared to the conventional carrier hybrid PWM technique. The hardware and simulation results comparison before filter for 11-level MLI are mentioned in Table 4.

Table 3. Comparative simulation results for 11 level inverter by PD-LSPWM

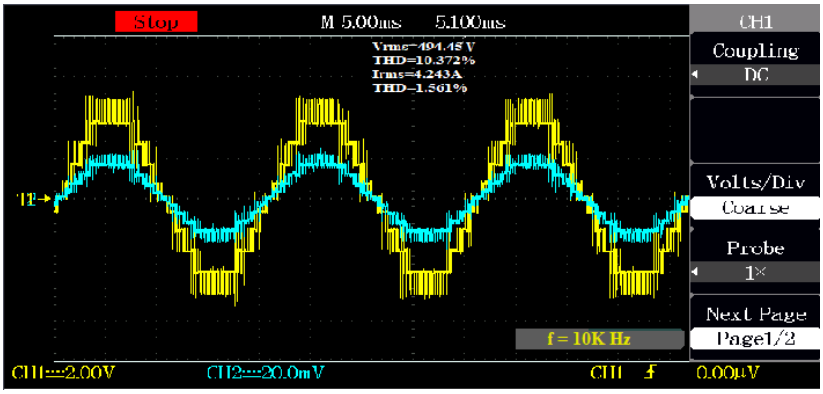
Parameter	Voltage (RMS value)				Current (RMS value)	
	Before filter		After filter		Before filter	
	Fundamental (HZ)	%THD	Fundamental (HZ)	%THD	Fundamental (HZ)	%THD
Conventional carrier shape [17]	444.6	14.17	440.8	3.27	4.425	1.86
Capacitor switched-PWM MLI [18]	420.3	11.41	-	-	-	-
Proposed carrier shape 1	494.5	10.37	490.4	3.27	4.922	1.75

4.1. Hard-ware description

Figure 5(a) depicts the proof-of-the concept laboratory prototype of the 11-level CMLDCL inverter with the proposed carrier HPWM. It is constructed using MOSFETs and diodes and tested with modified carrier shape 1 PD-SPWM technique. Regulated 100 V DC supply is used as the power supply for all the sources. A PIC16F887 microcontroller is used for the generation of control pulses. Sub-inverter on another side linked to a single-phase full-bridge (SPFB) inverter is operated at 0.88 modulation index, 10 kHz switching frequency and tested with R=100 ohms, L= 30 mH load. The output voltage and output current of the 11-level CMLDCL inverter are measured using digital signal oscilloscope (DSO) as shown in Figure 5(b). The fundamental voltage and THD of 494.5 V, 10.372% are obtained respectively. As a result, the voltage and current THD of the 11-level CMLDCL inverter is shown for almost two cycles. Table 4 is the comparison of experimental and simulation results with the proposed novel carrier shape 1-HPWM technique before the filter. The experimental fundamental output voltage, current; THDs are 494.45 V, 4.243 A; 10.372%, 1.861% respectively, and is in good agreement with the simulation results. From the results, it can be noticed that the proposed technique significantly improves the fundamental components of output voltage than the conventional PWM technique.



(a)



(b)

Figure 5. Modified 11-level CMLDCL inverter using modified carrier shape 1 PD-SPWM technique for (a) hard-ware representation of proposed model and (b) CRO output voltage

Table 4. Comparison of proposed simulation and experimental results

Novel carrier shape 1 for HPWM techniqueat d=0.75, D=0.25, (Proposed)				
	Before filter			
Comparison	Simulation results		Experimental results	
Parameter	Funda-mental (HZ)	THD (%)	Funda-mental (HZ)	THD (%)
Phase voltage (RMS)	494.5	10.37	494.45	10.372
Load current (RMS)	4.25	1.86	4.243	1.861

5. CONCLUSION

The performance of the novel carrier based HPWM technique is investigated on 11-level CMLDCLI and compared with the conventional SPWM control technique. It is observed that the proposed control technique improves the fundamental component of output voltage and lower THD. The performance of the control technique is tested in simulation and also validated through experimental investigation. The simulation and experimental results are in close agreement with each other.

ACKNOWLEDGEMENTS

We thank the applied renewable energy research (ARER) lab of sree vidyanikethan engineering college, Tirupati. A.P State, India for providing a research Lab to carry out the research on multilevel Inverters.

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