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Analysis of a New Reduced Switch Nine Level Inverter

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Abstract

The multi level inverter system is mostly used in ac drives, when both reduced harmonic contents and high power are required. In this paper a new topology of multilevel inverter is introduced. This type has many steps with less power electronic switches. Due to the less number of switches the cost of the inverter is very less and also less installation area is required. Firstly, we describe briefly the structural parts of the inverter then switching strategy and operational principles of the proposed inverter are explained and operational topologies are given. Simulation is performed using MATLAB SIMULINK. Various PWM techniques are applied to the circuit such as PDPWM, PODPWM, APODPWM, VFPWM and COPWM. By comparing among the PWM techniques, PODPWM provide the less THD value and COPWM provide a higher fundamental RMS output voltage.

Keywords*: PDPWM, PODPWM, APODPWM, VFPWM, COPWM, THD*

1. Introduction

The multilevel inverter [MLI] is used for high voltage and high power applications. This inverter produce staircase (stepped) waveform from several different levels of DC voltage. It have lower voltage rating of devices, low harmonics distortion, high power quality waveforms, lower switching frequency and losses, higher efficiency, reduction of dv/dt stresses. Because of the above characteristics, it have a possibility of working with low speed semiconductors if its compared with the two-level inverters. Many number of MLI topology are available but most popular MLI topology is diode clamped, flying capacitor and cascaded multilevel Inverter. Radan [1] et al developed an evaluation of carrier-based pwm methods for multi-level inverters. Samir and Lezana [2] introduced a multicarrier pwm with dc-link ripple feed forward compensation for multilevel inverters. Palanivel and Dash [3] made multicarrier pulse width modulation methods based three phase cascaded multilevel inverter including over modulation and low modulation indices. Andler [4] et al deal with a switching loss analysis of modulation methods used in neutral point clamped converters. Sujanarko [5] et al proposed advanced carrier based pulse width modulation in asymmetric cascaded multilevel inverter. Mukherjee and Poddar [6] suggested a series connected three level inverter topology for medium voltage squirrel cage motor drive applications. Kavousi and Vahidi [7] presented an application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters. Cougo et al [8] deal with PD modulation scheme for three phase parallel multilevel inverters. Yousefpoor et al [9] introduced a THD Minimization Applied Directly on the Line to Line Voltage of Multilevel Inverters. Distributed control of a fault-tolerant modular multilevel inverter for direct-drive wind turbine grid interfacing introduced by parker et al [10]. Younghoon Cho et al [11] developed a carrier-based neutral voltage modulation strategy for multilevel cascaded inverters under unbalanced dc sources. Murali et al [12] made A design and analysis of voltage source inverter for renewable energy applications. Jamaludin et al [13] proposed a multilevel voltage source inverter with optimized usage of bidirectional switches. Gabriel et al [14] introduced a five-level multiple-pole pwm ac – ac converters with reduced components count. Lim et al [15] suggested a modular-cell inverter employing reduced flying capacitors with hybrid phase-shifted. Rasilo et al [16] proposed a effect on multilevel inverter supply on core losses in magnetic materials and electrical machine. Reddy et al [17] developed a embedded control for a n -Level DC – DC – AC Inverter. Ranjitha and Ravivarman [18] made a review on voltage balancing solutions in multilevel inverter. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

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2. Multilevel Inverter

The operation of a multilevel inverter is concerned with comparison of carrier and reference wave.

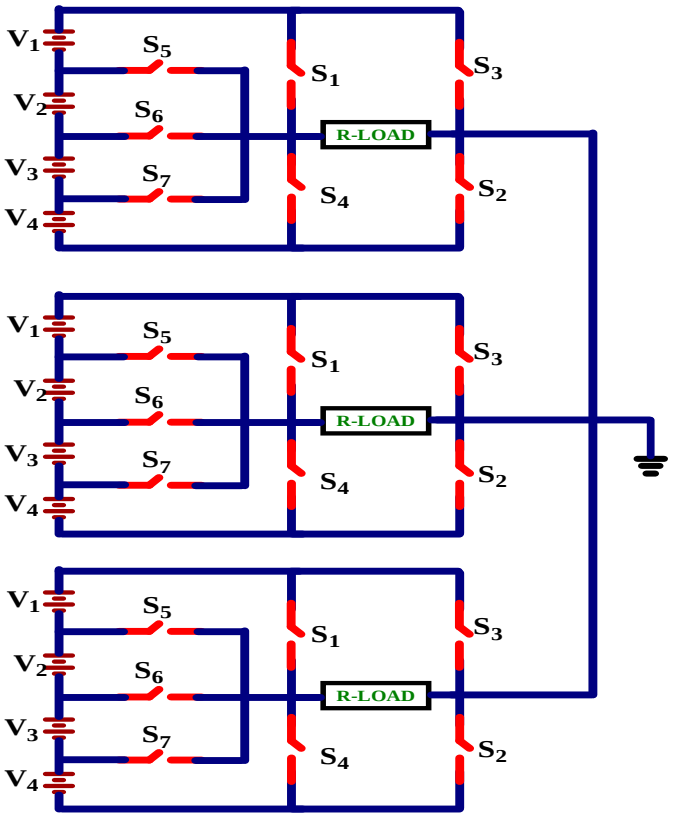

Figure 1. Power Circuit for Three Phase Nine Level Inverter

The basic operation can be described as an optional stacking of a number of DC voltage source stages which depends on certain time of operation that one stage is stacked (forward or reverse) or bypassed. MLIs also have some issues such as requiring a big number of semiconductor switches which increases as the number of steps/levels increases. If the levels of the steps increase the design will be complex for synchronous gate drivers for different levels. The order of numbering of the switches is S_1, S_2, S_3, S_4, S_5, S_6 and S_7. This circuit does not have a capacitor and diode. So cost of the circuit is low compared to the conventional circuit. The voltage levels of the outputs are $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$. In proposed circuit semiconductor switches are less when compared to the conventional circuit. So the advantages of the proposed circuit are less cost and minimum switching losses. Figure 1 shows a three phase nine level Inverter.

Table 1. Comparison table between conventional and proposed circuit

S.No	Conventional circuit DCMLI (9-level)	Conventional circuit FCMLI (9-level)	Conventional circuit CMLI (9-level)	Proposed circuit (9-level)
Switches	48	48	48	**21**
Diode	48	48	48	**0**
Clamping Diode	168	0	0	**0**
DC Bus Capacitor	24	24	12	**0**
Balancing Capacitor	0	84	0	**0**
DC Sources	1	1	12	**12**

3. Modulation Strategies

The most popular PWM methods are available to the inverter. For controlling the output voltage, one of the methods is SPWM method. In this method, a fixed DC input voltage is applied to the inverter and get a controlled AC output voltage by adjusting the ON and OFF periods of the inverter power semiconductor devices. By this technique increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonics and associated sideband harmonics further away from the fundamental frequency component. The modulating/reference wave of multilevel carrier based PWM strategies is sinusoidal. The sinusoidal reference wave is concerned to multiple Control Freedom Degree including frequency, amplitude, and phase angle of the reference wave. The principle of SPWM strategy is to use several carriers with three phase sinusoidal modulating signal. For an m level inverter, m-1 carriers are used. All carriers having same frequency f_c and same peak-to-peak amplitude A_c which are disposed such that the bands they occupy overlap each other. The amplitude of the reference wave is A_m and frequency is $f_{m,}$ which are centered in the middle of the carrier signals. The frequency ratio m_f is defined in the carrier overlapping method as follows:

$$m_f = \frac{f_c}{f_m}$$

This paper focuses on five SPWM strategies. They are: PDPWM, PODPWM, APODPWM, VFPWM and COPWM. The above five strategies are simulated in this work.

Figure 2. A sample SIMULINK model developed for chosen three phase seven level inverter for COPWM technique

Table 2. Switching table for proposed circuit

Switching Level	S_1	S_2	S_3	S_4	S_5	S_6	S_7
$4V_{dc}$	1	1	0	0	0	0	0
$3\ V_{dc}$	0	1	0	0	1	0	0
$2\ V_{dc}$	0	1	0	0	0	1	0
V_{dc}	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0
$-V_{dc}$	0	0	1	0	1	0	0
$-2\ V_{dc}$	0	0	1	0	0	1	0
$-3\ V_{dc}$	0	0	1	0	0	0	1
$-4V_{dc}$	0	0	1	1	0	0	0

A. PDPWM Strategy

This method is one of the PWM techniques. In this work, six carriers are used for 9 levels AMLI. Each carrier is having amplitude as 1V. The sinusoidal reference wave is placed at the middle of the six carriers. In PDPWM technique all carriers are arranged in a same manner. The carrier arrangement for this strategy is shown in Figure 3.

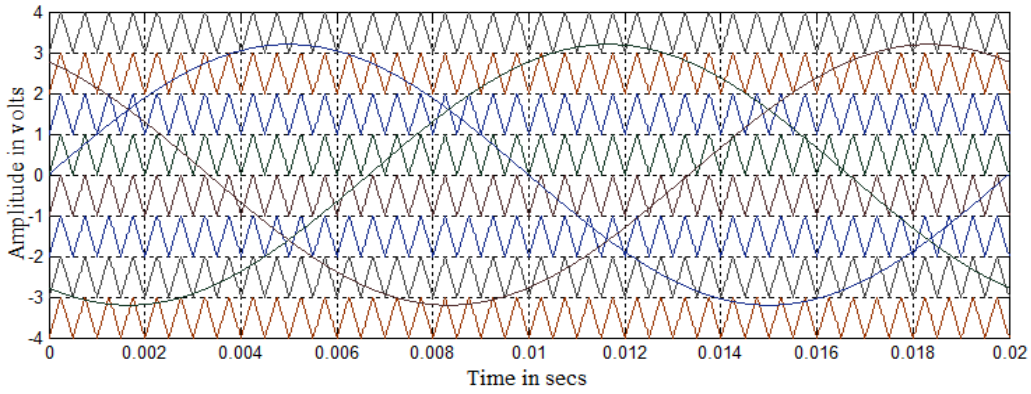

Figure 3. Modulating and carrier waveforms for PDPWM strategy (m_a=0.8 and m_f=40)

B. PODPWM Strategy

This method is same as PDPWM but carrier arrangement is some what different. The carriers are equally divided into two groups based on positive/negative average levels. In this type the two groups are opposite in phase with each other while keeping in phase within the group. The carrier arrangement for this strategy is shown in Figure 4.

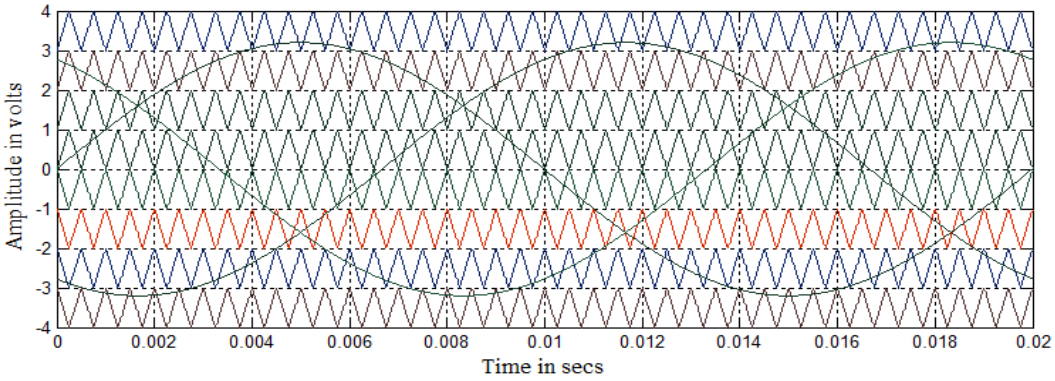

Figure 4. Modulating and carrier waveforms for PODPWM strategy (m_a=0.8 and m_f=40)

C. APODPWM Strategy

This method is also same as PDPWM technique but one of the main different in APODPWM by comparing to the PDPWM is that the alternate carriers are phase shifted by 180 degree with each other. The carrier arrangement for this strategy as shown in Figure 5.

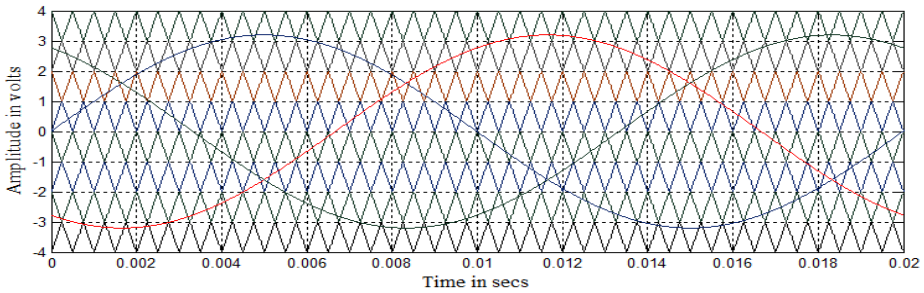

Figure 5. Modulating and carrier waveforms for APODPWM strategy (m_a=0.8and m_f=40)

D. VFPWM Strategy

This method is one of the PWM techniques and it is same as PDPWM but intermittent carrier having different frequency compare to upper and lower carrier. The carrier arrangement for this strategy is shown in Figure 6.

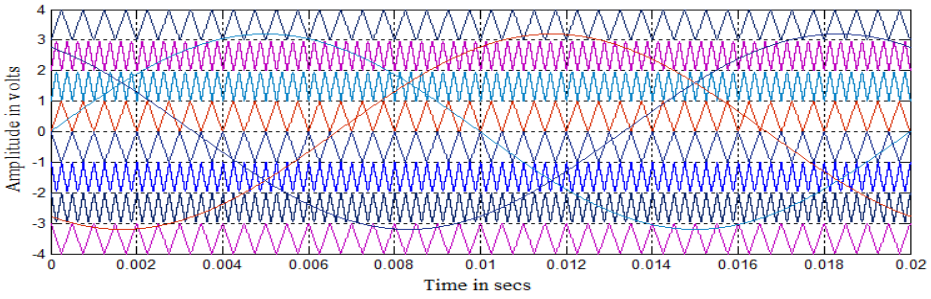

Figure 6. Modulating and carrier waveforms for VFPWM strategy (m_a=0.8, m_f=40 for upper and lower switches and m_a=0.8,m_f=80 for intermediate carrier)

E. COPWM Strategy

This method is same as PDPWM method but each carriers are overlapped each other and overlapping amplitude is 0.8V but each carrier having amplitude 1.6V and the total amplitude of this technique is 2.8. The carrier arrangement for this strategy is shown in Figure 7.

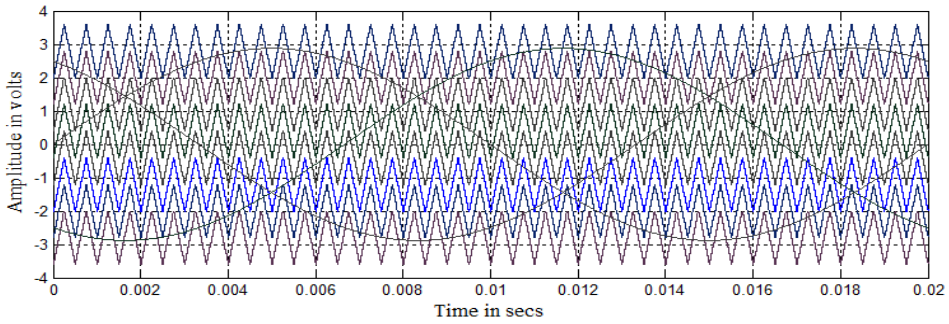

Figure 7. Modulating and carrier waveforms for COPWM strategy (m_a=0.8 and m_f=40)

4. Simulation Results

Simulation studies are performed by using MATLAB-SIMULINK to verify the proposed PWM strategies for chosen three phase proposed nine level inverter for various values of m_a ranging from 0.6 – 1 and corresponding %THD values are measured using FFT block and they are shown in Table 3. Table 4 shows the V_{RMS} of fundamental of inverter output for the same modulation indices. Table 5 shows the form factor for different modulation indices which are calculated using rms voltage and DC component from FFT plots. Table 6 shows Crest factor values which are measured using peak voltage and rms voltage from FFT plots. Table 7 shows the distortion factor for different modulation indices. This inverter produce 9 level up to m_a=0.8. Figure 8 shows the simulated output voltage of chosen MLI and the corresponding FFT plots with different strategies but only for one sample value of m_a=0.8 and m_f=40. Figure 8 shows the nine level output voltage generated by PDPWM strategy and its FFT plot is shown in Figure 13. From Figure 13 it is observed that the PDPWM strategy produces significant 2^{nd} 3^{rd}, 5^{th}, 11^{th}, 12^{th}, 15^{th}, 17^{th}, 21^{st}, 23^{rd}, 24^{th}, 30^{th}, 34^{th}, 38^{th} and 40^{th} harmonic energy. Figure 9 shows the nine level output voltage generated by PODPWM strategy and its FFT plot is shown in Figure 14.

From Figure 14 it is observed that the PODPWM strategy produces significant 3rd, 5th, 9th, 11th, 15th, 17th, 21st, 25th, 27th, 29th, 31st, 33rd, 35th, 37th and 39th harmonic energy. Figure 10 shows the nine level output voltage generated by APODPWM strategy and its FFT plot is shown in Figure 15. From Figure 15 it is observed that the APODPWM strategy produces significant 5th, 7th, 11th, 15th, 17th, 21st, 25th, 27th, 29th, 31st, 33rd, 35th and 39th harmonic energy. Figure 11 shows the nine level output voltage generated by VFPWM strategy and its FFT plot is shown in Figure 16. From Figure 16 it is observed that the VFPWM strategy produces significant 3rd, 5th, 11th, 15th, 17th, 19th, 21st, 23rd, 25th, 27th, 29th, 31st, 33rd, 35th, 37th and 39th harmonic energy. Figure 12 shows the nine level output voltage generated by COPWM strategy and its FFT plot is shown in Figure 17. From Figure 17 it is observed that the COPWM produces significant 12th, 20th, 31st and 40th harmonic energy. The following parameters are used for the simulation V_{dc}=110V, R=100Ω, f_c=2000Hz, f_m=50Hz.

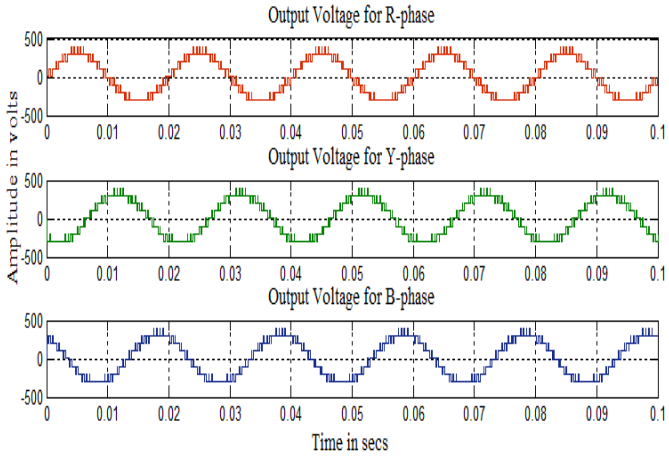

Figure 8. Simulated output voltage generated by PDPWM technique for R load

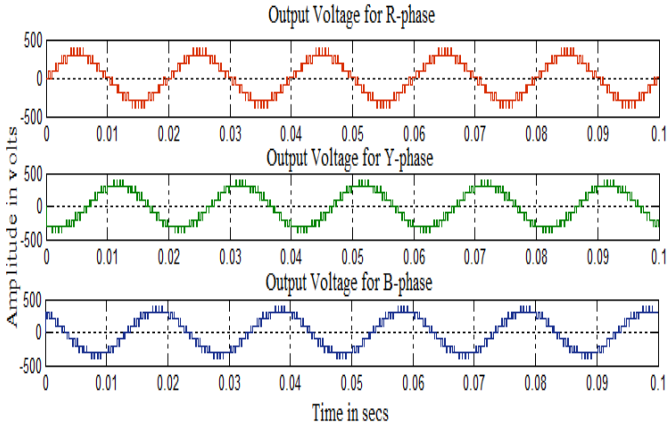

Figure 9. Simulated output voltage generated by PODPWM technique for R load

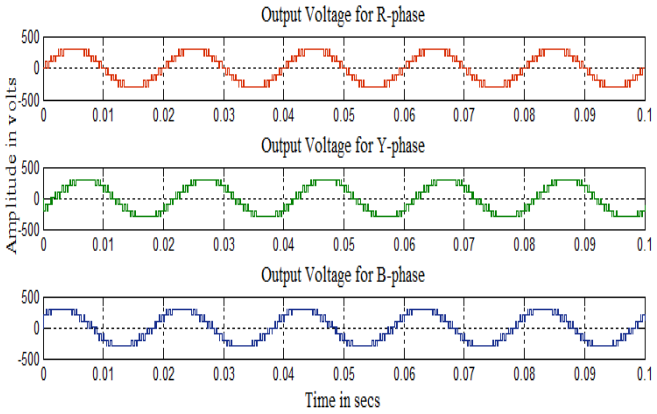

Figure 10. Simulated output voltage generated by APODPWM technique for R load

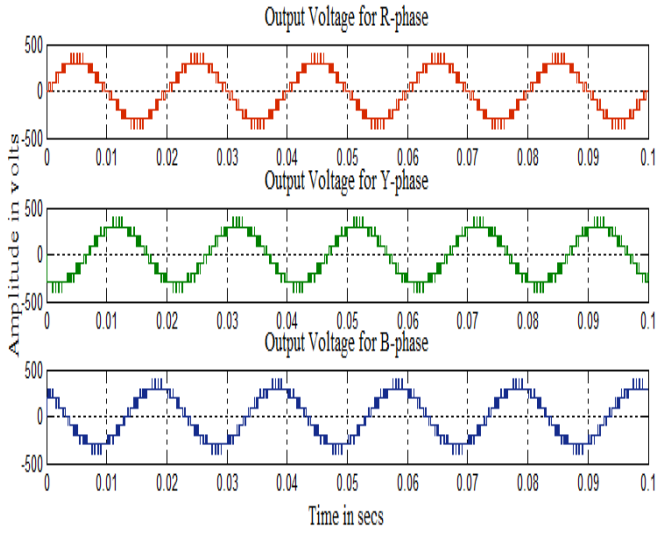

Figure 11. Simulated output voltage generated by VFPWM technique for R load

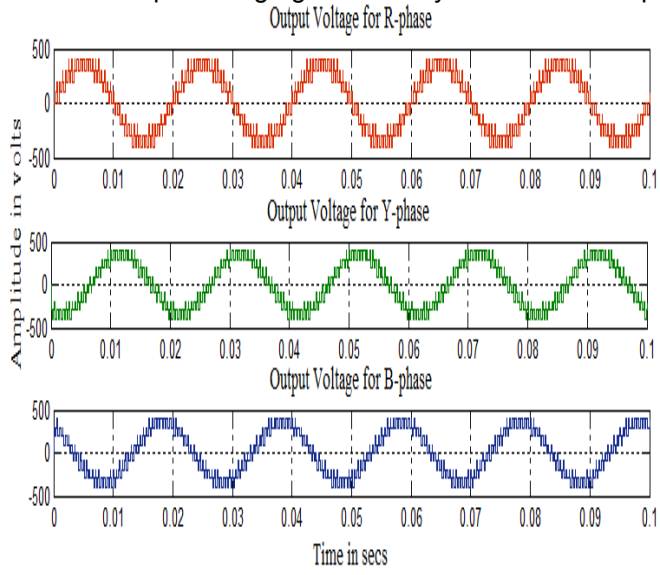

Figure 12. Simulated output voltage generated by COPWM technique for R load

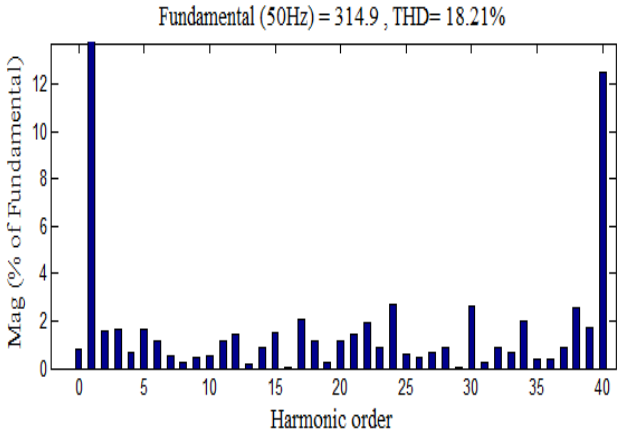

Figure 13. FFT spectrum for PDPWM technique

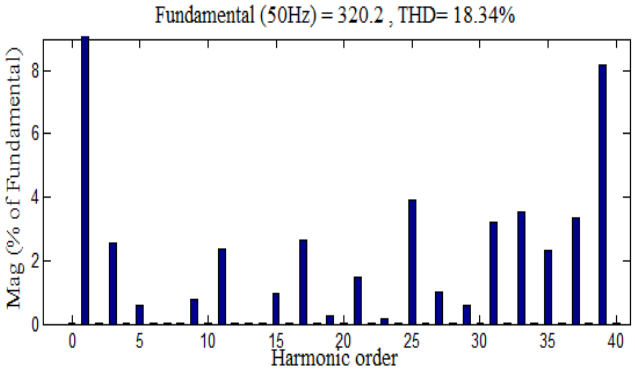

Figure 14. FFT spectrum for PODPWM technique

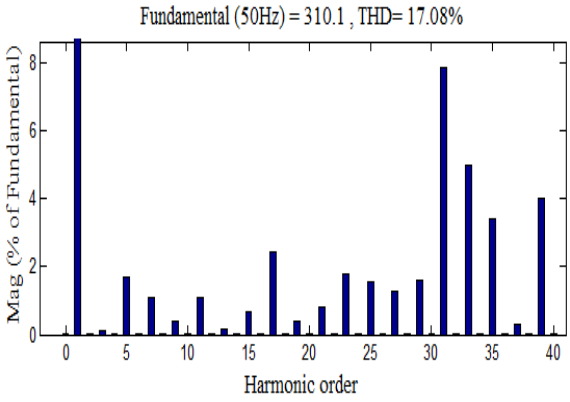

Figure 15. FFT spectrum for APODPWM technique

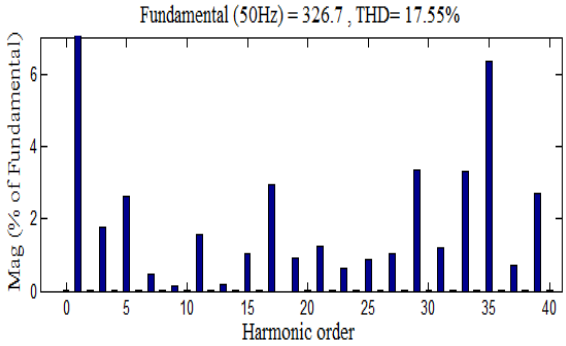

Figure 16. FFT spectrum for VFPWM technique

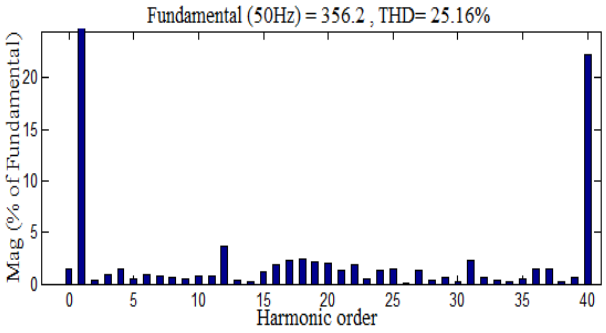

Figure 17. FFT spectrum for COPWM technique

Table 3. % THD of output voltage of chosen MLI for various values of modulating indices

%THD	m_a				
	1.0	0.9	0.8	0.7	0.6
PDPWM	13.51	17.29	18.21	21.84	24.27
PODPWM	12.67	17.04	18.34	22.09	23.02
APODPWM	13.45	17.53	17.08	22.80	24.73
VFPWM	12.88	17.04	17.55	22.26	23.99
COPWM	18.52	21.96	25.16	29.91	35.4

Table 4. % V_{RMS} of output voltage of chosen MLI for various values of modulating indices

% V_{RMS}	m_a				
	1.0	0.9	0.8	0.7	0.6
PDPWM	281.7	253.8	222.7	194.3	170.7
PODPWM	284.1	256.3	226.4	193.1	168.5
APODPWM	281.4	250.9	219.3	191.3	166.2
VFPWM	285	255.2	231	194.5	166.4
COPWM	298.3	276.8	251.9	222.5	189

Table 5. Form Factor of output voltage of chosen MLI for various values of modulating indices

% V_{RMS}	m_a				
	1.0	0.9	0.8	0.7	0.6
PDPWM	563.4	604.3	281.9	1079.4	275.3
PODPWM	INF	INF	INF	INF	INF
APODPWM	INF	INF	INF	INF	INF
VFPWM	INF	INF	INF	INF	INF
COPWM	505.6	1064.6	179.9	1390.6	67.26

Table 6. Crest Factor of output voltage of chosen MLI for various values of modulating indices

% V_{RMS}	m_a				
	1.0	**0.9**	**0.8**	**0.7**	**0.6**
PDPWM	1.4143	1.4141	1.4141	1.4143	1.4142
PODPWM	1.4139	1.4144	1.4143	1.4143	1.4142
APODPWM	1.4140	1.4145	1.4140	1.4140	1.4139
VFPWM	1.4144	1.4142	1.4143	1.4138	1.4146
COPWM	1.4143	1.4140	1.4141	1.4144	1.4143

Table 7. Distortion Factor of output voltage of chosen MLI for various values of modulating indices

% V_{RMS}	m_a				
	1.0	**0.9**	**0.8**	**0.7**	**0.6**
PDPWM	0.0995	0.3188	0.4374	0.3919	0.496
PODPWM	0.033	0.1798	0.2877	0.1413	0.5179
APODPWM	0.0897	0.2211	0.0737	0.0992	0.4838
VFPWM	0.1131	0.0411	0.2251	0.2738	0.4029
COPWM	0.507	0.394	0.1601	0.666	0.8173

6. Conclusion

In this paper various new schemes adopting the constant switching frequency multicarrier CFD concepts are developed and simulated for a chosen nine level asymmetrical inverter. Performance indices like %THD, V_{RMS} (indicating the amount of DC bus utilization), CF, FF and DF related to power quality issues have been evaluated, presented and analyzed. By comparing among the conventional PWM techniques, PODPWM techniques provide the less THD value (table 3) and COPWM provide a higher fundamental RMS output voltage (table 4). Table 5 shows FF for all modulating indices. Table 6 displays CF for all chosen modulating indices. Table 7 displays DF for all chosen modulating indices. The result indicate that appropriate PWM strategies have to be employed depending on the performance measure required in a particular application of MLI based on the criteria of output voltage quality (Peak value of the fundamental, THD and dominant harmonic components).

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