A new topology of multilevel inverter with switches count reducing at symmetrical/asymmetrical mode

Mohammed D. Albakhait, Arwa Amer Abdulkareem
Department of Electrical Power Engineering Techniques, Electrical Engineering Technical College, Middle Technical University, Baghdad, Iraq

Article Info

ABSTRACT

The multi-level inverter (MLI) has an important role in modern technologies due to its advantages. On the other hand, its circuits need a large number of switches, capacitors and direct current (DC) sources. This paper introduces a new topology for a MLI with a reduction in number of switches, no need for capacitors in exchange for an increase in number of levels in the output. The proposed model is operated in symmetric and asymmetric modes with the presence of resistive and inductive loads. Whereas, (5 and 9) output levels were obtained in symmetric and asymmetric modes, respectively. In contrast, the number of switches was halved and without need for capacitors, compared to the conventional MLI topologies not a secret that reducing the number of switches has the effect of reducing cost and complexity, in addition to the problems of balancing the voltage on capacitors. The programming environment used to build the proposed model of the MLI was MATLAB/Simulink, where the validity of the hypotheses contained in this paper were proved and the obtained results are identical to what was planned under different loads and different operation modes. In addition, the paper included a comparison study among the proposed topology and conventional topologies in terms of the number of switches, capacitors and sources.

Corresponding Author:

Mohammed D. Albakhait
Department of Electrical Power Engineering Techniques, Electrical Engineering Technical College
Middle Technical University
Baghdad, Iraq
Email: mohammedalbakhait@mtu.edu.iq

1. INTRODUCTION

In recent decades, the topologies of the multi-level inverter (MLI) have become very popular in the scientific and industrial fields. This came because of the capabilities of this type of inverters to induced an output power with high efficiency, indeed, much better than its conventional two-level inverter [1]. Actually, The multi-level inverter is a result of a great development in semiconductor switches industry technology. Where these mutations in the quality of electronics switches and its speed response, in addition with an urgent need to MLI in industrial fields, all of this led to the birth of the first multi-level inverter. Therefore, the MLI is a combination of the capabilities of electronics switches, bisa dihi sources or links, and a suitable control algorithm. This interaction is led to generate an output voltage in a staircase wave form which is closest as possible as to the sinusoidal waveform [2]–[5].

There are three main conventional topologies of the MLI that are widely used in practical and commercial applications, namely, neutral point clamped (NPC), flying capacitor (FC) and cascade h-bridge (CHB) MLI [6], [7]. As a literature review of a multi-level inverter, Nabae et al who generated three voltage levels using the NPC method first devised this type of inverter in 1981. Another modification of multilevel

inverter topology was introducing flying capacitor MLI in mid of last decade of twentieth century [8]–[12]. Recently, a modern MLI topographies have been developed, with the aim of overcoming on some of the problems found in this type of devices. One of these topographies is active clamped (ANPC) whitch presented by Bruckner *et al.* [13] which aims to overcome the imbalance in the sharing of switching losses between the outer and inner switches of MLI. An other topology named as hybridised cascaded h-bridge (HCHB) MLI which presented by Odeh and Nnadi [14] which is used more auxiliary/clamping switches for enhancement of the harmonic profile of waveforms in the output. Another classification of the MLI, named as modular multilevel converter (MMC) that presented by Lesnicar and Marquardt. The MMC has a simplified construction and redundancy and modular extension to any output level in compare with traditional CHB MLI [15].

The main problem in MLI is how to get a large number of levels in output with a minimum number of swithes, capacitors and DC sources. Nowday, researchers focus their efforts on reducing the number of DC sources, switches, and improving the process of balancing the voltage between capacitors with more output levels and less harmonics distortion [16]–[21]. This paper introduces a new method for MLI topology. Whereas, five and nine levels have gotten from the proposed circuit in case symmetric and asymmetric modes respectively. On the other side, a reduction in number of switches required to perform the function of MLI without need for capacitors, while inspect the circuit at resistive and inductive loads. The computer model for the proposed circuit was designed using MATLAB/Simulink, in order to verify the correctness of the expected results of the proposed topology. Topics in this paper are arranged as follows: second section describes the proposed topology design, and it consists of two sub-sections for the topology's operation condition, symmetric and asymmetric, respectively. Third section is a comparison between the proposed MLI and the conventional types of MLI in terms of number of switches, capacitors and DC sources requirements to produce a nine levels in the output. Fourth part will be a presentation of the computer model of the proposed MLI and its results for the two aforementioned operation modes. Finally, fifth section deals with a summary of the idea in this paper and future work.

2. DESCRIPTION OF PROPOSED MULTI-LEVEL INVETER TOPOLOGY

Figure 1 illustrates the basic components of the proposal model for a multi-level inverter. The power circuit of the inverter is consisting of a two DC voltage sources connected to the load via a group of eight unidirectional switches. Switches (S1 & S2), (S3 & S4), (S5 & S6), and (S7 & S8) are complementary switches, though, they cannot be turned on at the same time, because that will generate a short-circuit across one of DC voltage source or both of them in the same time. All the eight switches have to stand the maximum load current at ON-state and block the inverse voltage at OFF-state. Indeed, in the proposed MLI topology there are a three switches turn-on to generate each level of output voltage. So, the load current is shared among these three switches and that will reduce the rating power requirements when choosing the switches type. The multi-level inverter that uses DC sources of equal value is classified as symmetric, while the type that uses DC sources of different voltage value is asymmetric type [22]–[25]. The symmetric type has its drawbacks, such as: It requires a larger number of electronic switches and their related drive circuits for each of them, and a large number of DC-links, and this is what makes this type larger in size, cost, and very complex, especially for higher voltage levels in the output. On the other hand, the symmetric type has an advantages of being better in balancing the voltages between capacitors, and more flexibility in operating with faults conditions, because it includes more than one way (redundant states) to generate the same level of voltage. On the other hand, the asymmetric multi-level inverter type can drive a higher number of output levels for the same number of electronic switches and DC links compared to the symmetric type [26]–[28].
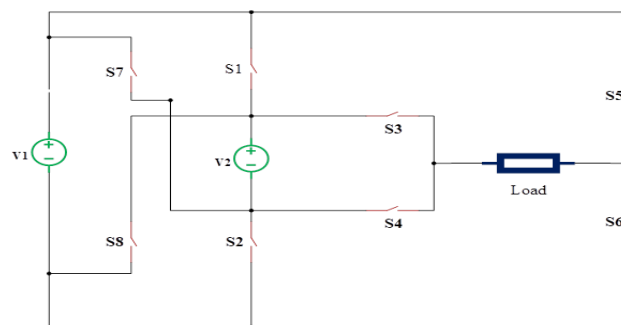

Figure 1. Proposed topology of MLI

3. RESEARCH METHOD

There are two modes to operate the proposed MLI depending on the value of the two dc voltage sources. First mode is symmetrical mode with V1=V2. Moreover, the second mode is asymmetrical mode with V1≠V2.

3.1. Symmetrical mode (2S-5L-8SW) MLI

For symmetrical mode the two DC voltage source have the same value V1=V2=V_{dc}. due to this equality in value of sources the number of levels in output is five level only. The switching state strategy applied to semiconductor switches to get these five-voltage levels illustrated in Table 1.

Table 1. Switching state of symmetrical (2S-5L-8SW) MLI

S1	S2	S3	S4	S5	S6	S7	S8	Vo (V)
0	0	1	0	0	1	1	0	+ 2 V_{dc}
0	1	1	0	0	1	0	0	+ 1 V_{dc}
0	0	0	1	0	1	1	0	two state give +1 V_{dc}
1	0	1	0	1	0	0	0	0 V_{dc}
0	1	0	1	0	1	0	0	two state give zero level
1	0	0	1	1	0	0	0	-1V_{dc}
0	0	1	0	1	0	0	1	two state give -1 V_{dc}
0	0	0	1	1	0	0	1	-2 V_{dc}

As shown clearly in Table 1, there are more than one way to get some levels in the output, and that give flexibility in case of switches faults. Figure 2 shows the path of connection among two DC sources and load via semiconductor switches. Clearly, V_o=+2 V_{dc} in connection path as Figure 2(a) shown, V_o=+1 V_{dc} in connection path as Figures 2(b) and (c) shown, V_o=0 V in connection path as Figures 2(d) and (e) shown, V_o=-1 V_{dc} in connection path as Figures 2(f) and (g) shown, and V_o=-2 V_{dc} in connection path as Figure 2(h) shown. Peak output voltage in this case is (1):

$$V_{p.o} = V_1 + V_2 = 2\,V_{dc} \tag{1}$$

Where $V_{p,o}$ is peak output voltage, V_1 and V_2 are the first and second DC source respectively and V_{dc} is the voltage value of DC source. The summation of peak inverse voltage that appear across any of semiconductor switches is called total standing voltage (TSV). However, TSV is an important factor in choosing the semiconductor switches of power circuit. The value of TSV is equal for each pair of complementary switches, as given in (1).

$$\left.\begin{array}{l} V_{PIV.S1} = V_{PIV.S2} = \ Vdc \\ V_{PIV.S3} = V_{PIV.S4} = \ Vdc \\ V_{PIV.S5} = V_{PIV.S6} = \ Vdc \\ V_{PIV.S7} = V_{PIV.S8} = \ 2\,Vdc \end{array}\right\} \tag{2}$$

Where $V_{PIV,\,Sk}$ is the peak inverse voltage, and k=1, 2…, 8. The resulting TSV is calculated as (3).

$$TSV = 2 \times (V_{PIV.S1} + V_{PIV.S3} + V_{PIV.S5} + V_{PIV.S7}) = 10V_{dc} \tag{3}$$

3.2. Asymmetrical mode (2S-9L-8SW) MLI

In this mode the two DC voltage source are unequal in its values, V1=Vdc, whenever V2=3 Vdc. As have been mentioned before in introduction, the asymmetrical mode enhance the operation of MLI by increase number of levels in compare with symmetrical mode for the same number of sources and switches. So the number of levels in output is increase to 9 level in current mode with the same circuit design before. To induced these nine level a critical conditions of Switching must be followed. The following logical strategy that shown in Table 2, illustrates the switching table for the eight switches that compose the power circuit of the proposed MLI at asymmetrical mode.

For asymmetrical mode, there is one state only can achieved by two path of conduction switches whiches 0 volt level. Figure 3, showes the path of conduction between DC sources and load through semiconductor switches. Whereas, V_o=+4 V_{dc} in connection path shown in Figure 3(a), V_o=+3 V_{dc} in connection path shown in Figure 3(b), V_o=+2 V_{dc} in connection path shown in Figure 3(c), V_o=+1 V_{dc} in connection path shown in Figure 3(d), V_o=0 V in connection path shown in Figures 3(e) and (f), V_o=-1 V_{dc} in connection path shown in Figure 3(g), V_o=-2 V_{dc} in connection path shown in Figure 3h, V_o=-3 V_{dc} in connection path shown in Figure 3(i), and V_o=-4 V_{dc} in connection path shown in Figure 3(j).
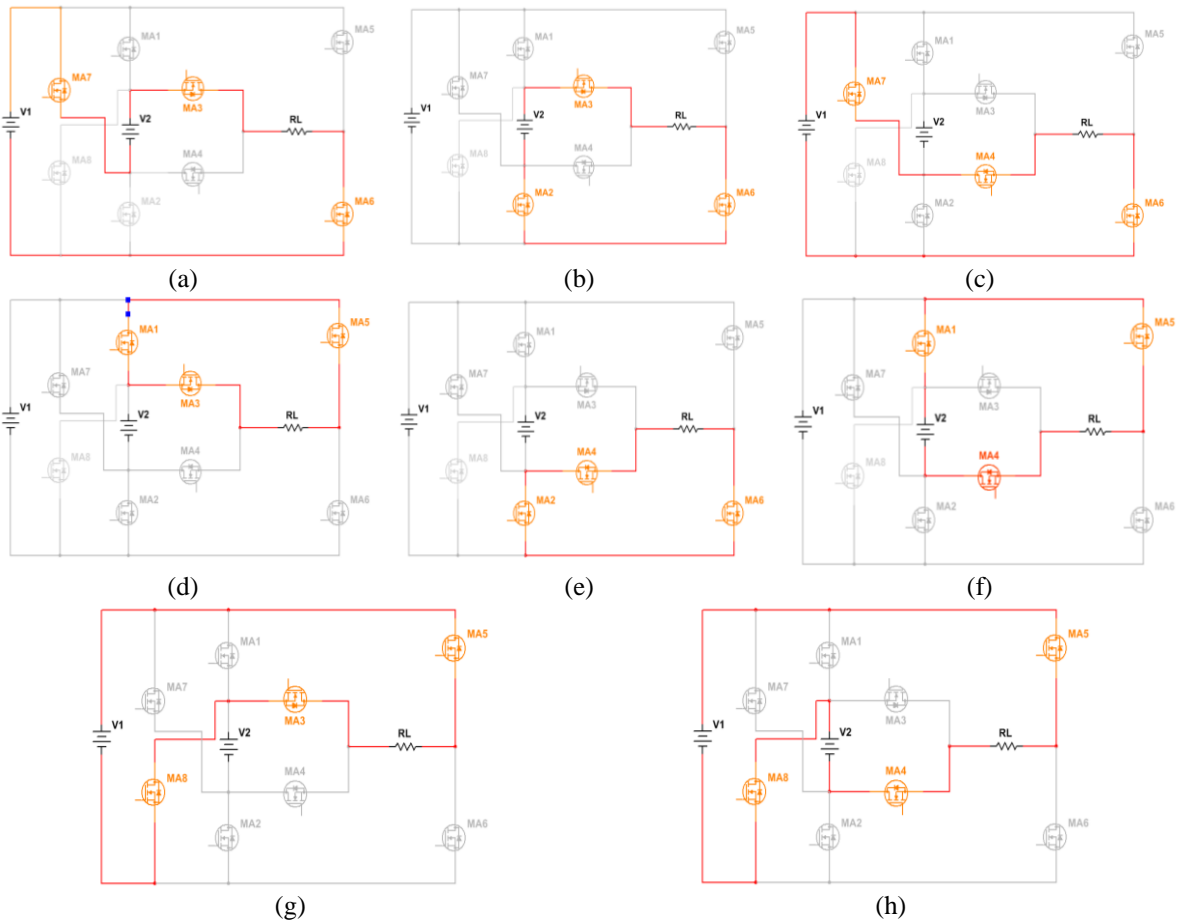
Figure 2. Path of connection in each switching states of symmetrical (2S, 5L, 8SW) MLI, (a) $V_o=+2V_{dc}$, (b) $V_o=+1V_{dc}$, (c) $V_o= +1V_{dc}$, (d) $V_o=0$, (e) $V_o=0$, (f) $V_o=-1V_{dc}$, (g) $V_o=-1V_{dc}$, and (h) $V_o=-2V_{dc}$

Table 2. Switching state of an asymmetrical (2S-9L-8SW) MLI

S1	S2	S3	S4	S5	S6	S7	S8	Vo (V)
0	0	1	0	0	1	1	0	$+ 4 V_{dc}$
0	1	1	0	0	1	0	0	$+ 3 V_{dc}$
0	1	1	0	1	0	0	0	$+2 V_{dc}$
1	0	1	0	0	1	0	0	$+1 V_{dc}$
1	0	1	0	1	0	0	0	$0 V_{dc}$
0	1	0	1	0	1	0	0	two state give zero level
0	1	0	1	1	0	0	0	$-1V_{dc}$
1	0	0	1	0	1	0	0	$-2 V_{dc}$
1	0	0	1	1	0	0	0	$-3 V_{dc}$
0	0	0	1	1	0	0	1	$-4 V_{dc}$

The peak output voltage is given as (4).

$$V_{p.o} = V_1 + V_2 = V_{dc} + 3V_{dc} = 4\,V_{dc} \tag{4}$$

The summation of peak inverse voltage that appear across any of semiconductor switches is called total standing voltage TSV. However, TSV is an important factor in choosing the semiconductor switches of power circuit. The value of TSV is equal for each pair of complementary switches, as given in (1).

$$\left.\begin{aligned}V_{PIV.S1} &= V_{PIV.S2} = 3\,Vdc\\ V_{PIV.S3} &= V_{PIV.S4} = 3\,Vdc\\ V_{PIV.S5} &= V_{PIV.S6} = Vdc\\ V_{PIV.S7} &= V_{PIV.S8} = 4\,Vdc\end{aligned}\right\} \tag{5}$$

So, the TSV is calculated as (6).

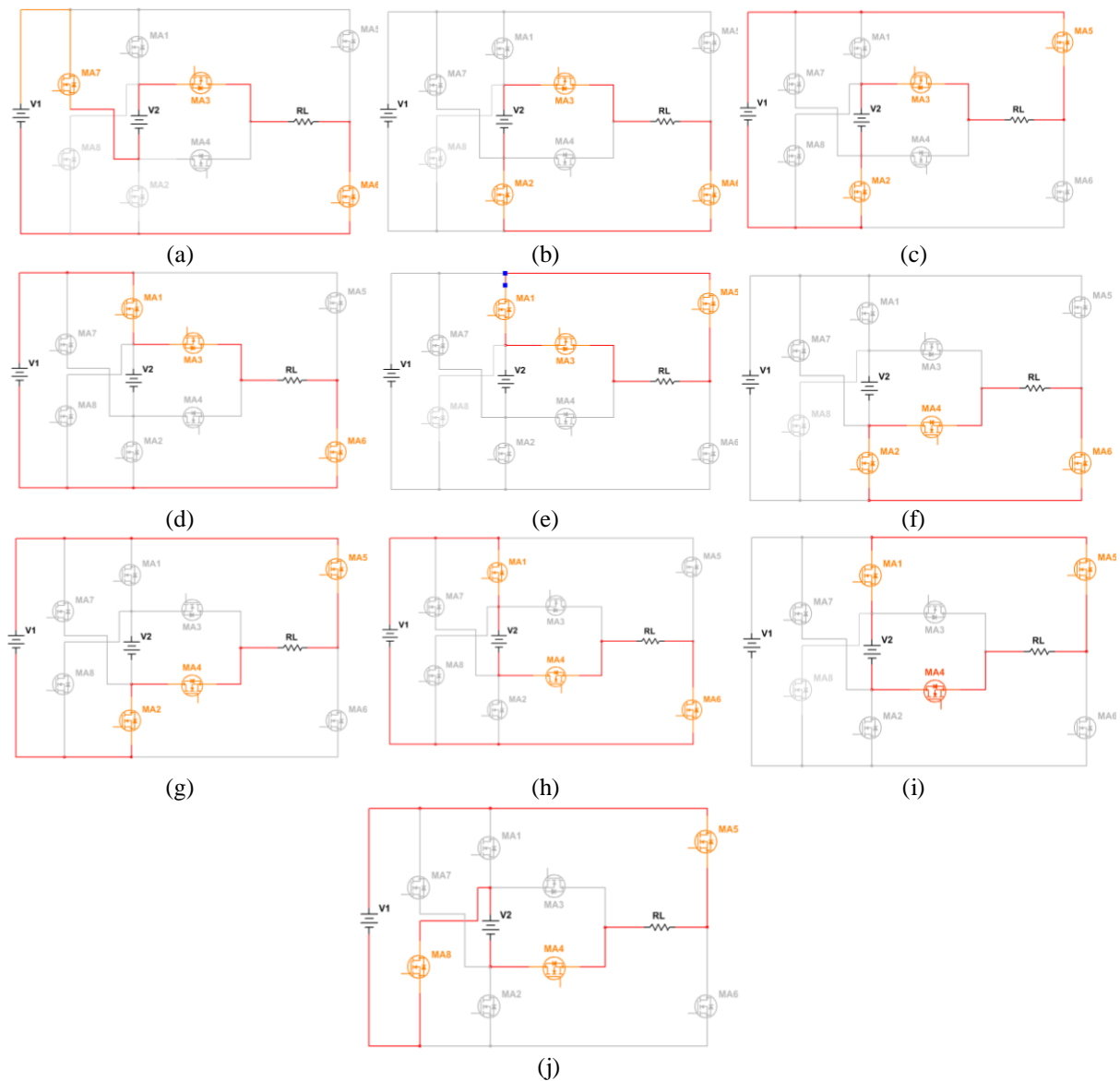$$TSV = 2 \times (V_{PIV.S1} + V_{PIV.S3} + V_{PIV.S5} + V_{PIV.S7}) = 22V_{dc} \tag{6}$$

Figure 3. Path of connection in each switching states of asymmetrical (2S, 9L, 8SW) MLI (a) $V_o = +4V_{dc}$, (b) $V_o = +3V_{dc}$, (c) $V_o = +2V_{dc}$, (d) $V_o = +1V_{dc}$, (e) $V_o = 0$, (f) $V_o = 0$, (g) $V_o = -1V_{dc}$, (h) $V_o = -2V_{dc}$, (i) $V_o = -4V_{dc}$, and (j) $V_o = -4V_{dc}$

4.   COMPARATIVE STUDY

This section is view for a comparative between the proposed topology of MLI with two sources, eight unidirectional switches at asymmetric operation mode, and conventional topologies of MLI (NPC, FC and CHB). The proposed topology has been compared in terms of number of power switches, power diode, isolated DC supply, DC bus capacitors, and balancing capacitors for the same number of levels in the output. Table 3 shows a numerical comparison among aforementioned topologies. the table shows that the proposed topology generates the same number of levels in the output with a smaller number of semiconductor switches and no need for capacitors (-). The number of isolated DC source is higher than NPC and FC topologies, but that against decrease the number of power switches in half, and for sure, that will mean reduce number of gate drive circuit [7].

Table 3. Comparison of electronic components and other requirements for the proposed MLI topology [7]

MLI Topology	Number of levels	Power switches	Power diode	Isolated DC supply	DC bus capacitor	Balancing Capacitors
NPC	9	16	12	1	4	-
FC	9	16	-	1	4	6
CHB	9	16	-	4	4	-
Proposed topology	9	8	-	2	-	-

5. SIMULATION AND RESULTS

The proposed topology of MLI shown in Figure 4 have been simulated using MATLAB/Simulink environment. This proposed topology and its representation in MATLAB will prove the possibility of reducing the number of switches and DC sources. In return of that, the proposed topology obtaining a higher number of levels in the output voltage. All that by using a control method to govern these switches, and to govern the electric power flows through theses switches. The circuit consist of two separated DC source, eight unidirectional metal oxide semiconductor field effect transistor (MOSFETs) switches and load. Gates pulses are generated for each switch individually to insure following of switching states strategies. The Model of proposed MLI operate in two modes, symmetrical ($V_1=V_2=100V$) and asymmetrical ($V_1=100$ V, $V_2=3V_1=300$ V) to produce five level and nine level respectively, from the same power circuit.
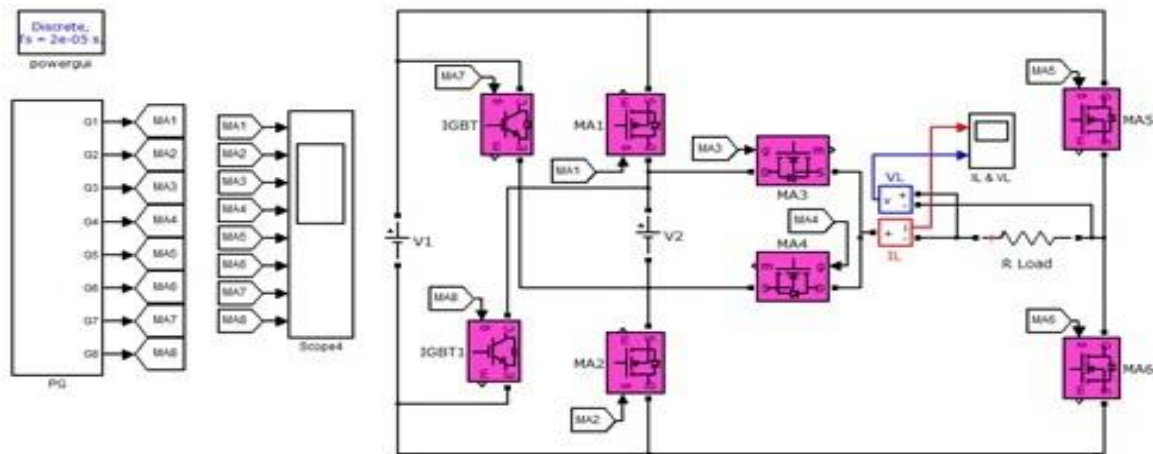
Figure 4. MATLAB model of proposed MLI

5.1. Symmetrical mode (2S-5L-8SW) MLI results

As mentioned before, symmetrical mode has two equal DC sources. Due to that limitation, levels in the output are limited to five level only. Moreover, the switching states of power switches have designed in such a manner to achieve these levels. The fundamental switching frequency techniques modulation has been used. There are several techniques under this topic, and the technique used to control the switches in the proposed topology is called a nearest level control modulation (NLCM), which is used due to its easy control and implementation especially when working on high level inverter. Figure 5 shows the pulses of the eight switches, these pulses must insure not turn on any of two complementary switches at the same time to avoid short-circuiting the sources. Whenever, Figure 6 shows NLCM in symmetrical mode and illustrate the five levels in output. Figure 7 illustrate output voltage and current on the resistive load (R=25 Ω). The wave forms of voltage and current have the same shape waveform, and in same phase. To illustrate the current waveform clearly, it has been multiplied by the value of ten. Figure 8 shows output voltage and current waveform at (R=25, L=80 mH). Noticed, there are a phase shift between voltage and current in the load, whereas, the current waveform lagged by (45°).

One of the most important advantages of a MLI over a conventional two-level inverter is that it can construct a voltage waveform at the output with a much lower ratio of total harmonic distortion (THD). Figure 9 shows total harmonic distortion of output current to (2S-5L-8SW) MLI. The value of fundamental harmonic is 7.478 A with THD equal to 19.64%. The total harmonic distortion of current waveform can be reduced significantly with inductive load. Whenever, Figure 10 illustrate THD of the output current which is equal to (3.52%).
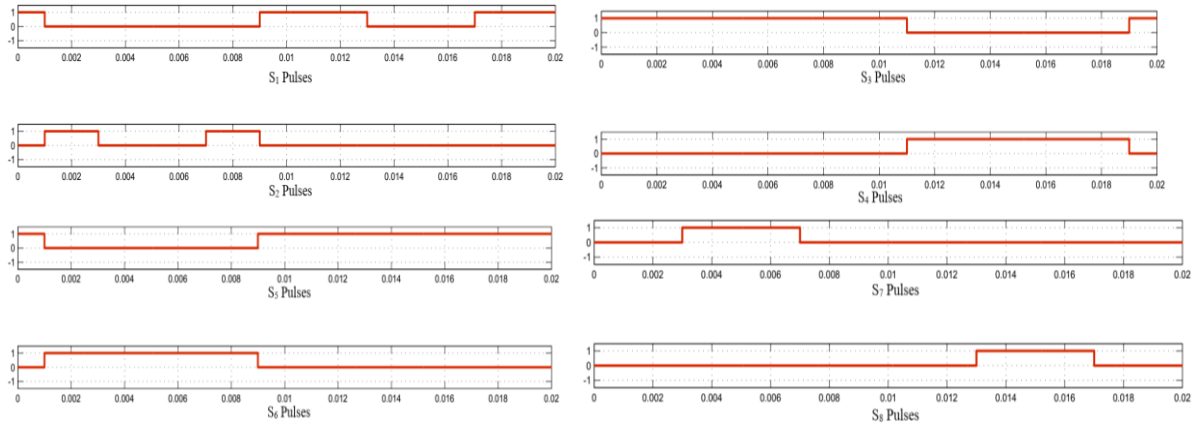
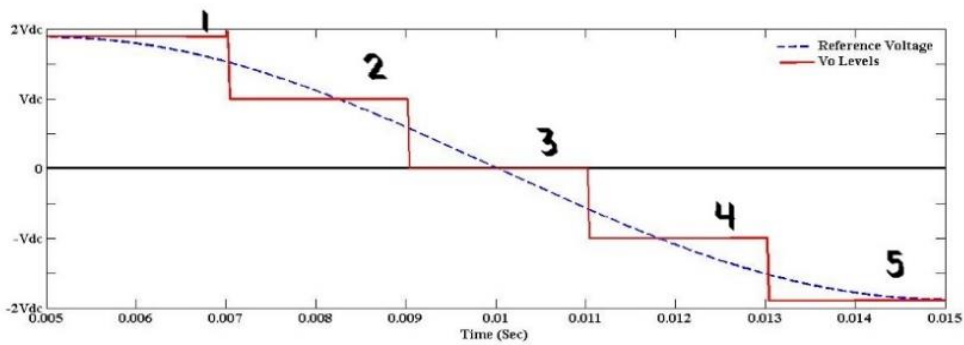Figure 5. Pulses of the 8 switches of symmetrical (2S-5L-8SW) MLI

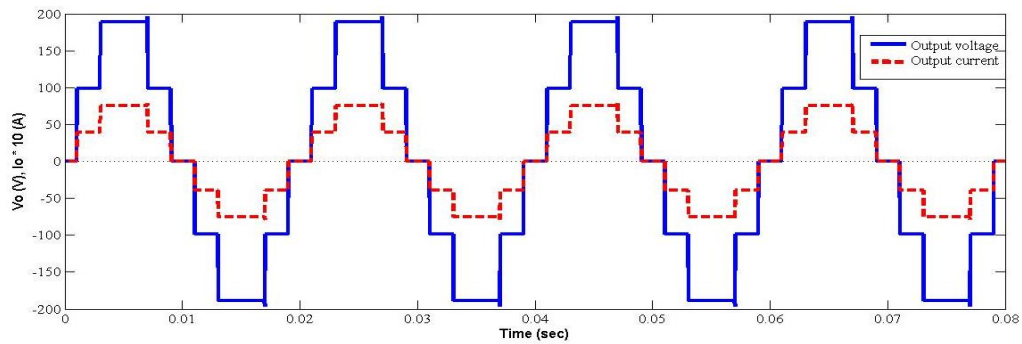Figure 6. NLCM of symmetrical (2S-5L-8SW) MLI

Figure 7. Output voltage and current waveform of symmetrical (2S-5L-8SW) MLI at (R=25 Ω)
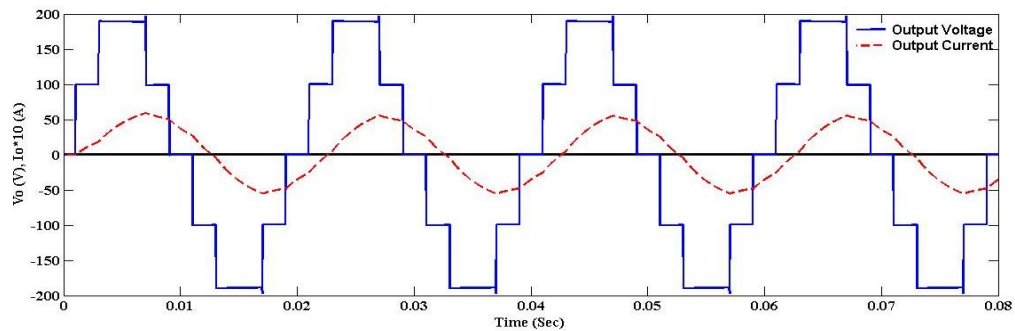

Figure 8. Output voltage and current of symmetrical (2S-5L-8SW) MLI at (R=25 Ω, L=80 mH)
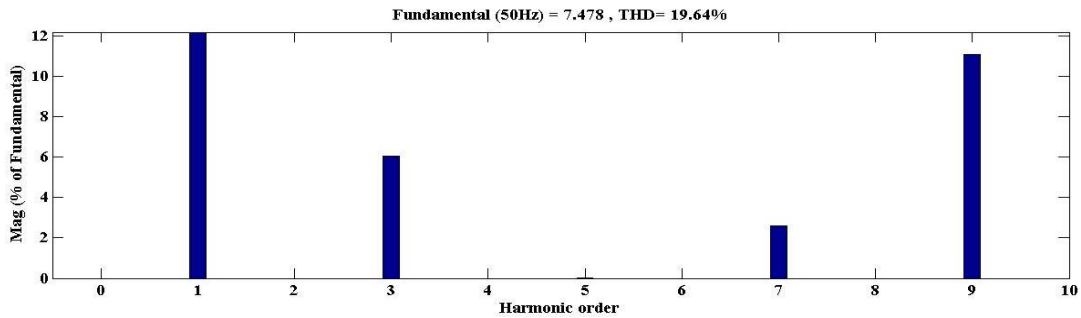
Fundamental (50Hz) = 7.478 , THD= 19.64%

Figure 9. FFT analysis of output current of symmetrical (2S-5L-8SW) MLI at (R=25 Ω)

Fundamental (50Hz) = 5.295 , THD= 3.52%
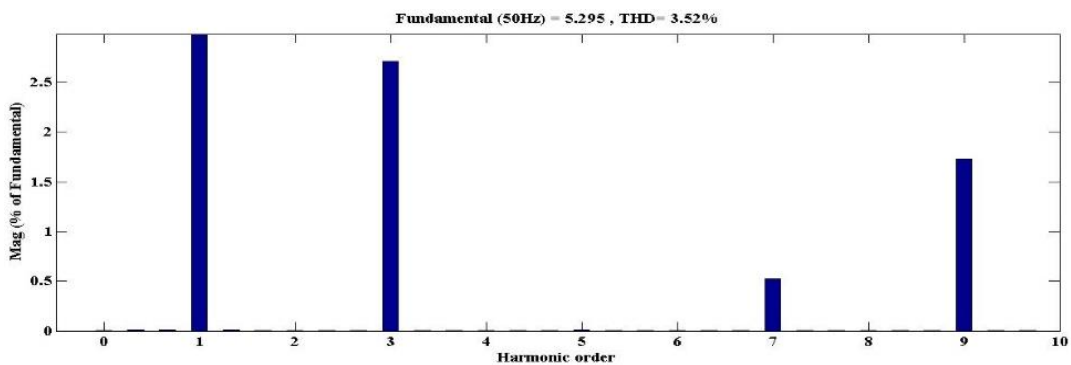
Figure 10. FFT analysis of output current of symmetrical (2S-5L-8SW) MLI at (R=25 Ω, L= 80 mH)

5.2. Asymmetrical mode (2S-5L-8SW) MLI results

A nine levels can induce in asymmetrical mode from the same power circuit topology of MLI. However, to get these nine levels, the switching states of the eight power switches have to follow the strategy illustrated in Table 2. Figure 11 shows the pulses used to trigger MLI's switches. As a reminder, it is not allowed to turn on two complementary switches at the same time. Whenever, Figure 12 shows the nearest level control modulation technique (NLCM) which is used to generate pulses of switches in asymmetrical operation mode. Also, its illustrate the nine levels in the output voltage.

The output voltage and current are shown in Figure 13. Which is in the same phase and shape, because the load is a pure resistive R=30 Ω. Figure 14 shows the output voltage and current at RL load, whereas R=30 Ω and L=45 mH. The output current is approximately a sinusoidal waveform with lagging phase shift about (22.5º) due to inductive load, which operate as a low pass filter. Also, the output current waveform multiplied by 10 to illustrate its shape clearly.
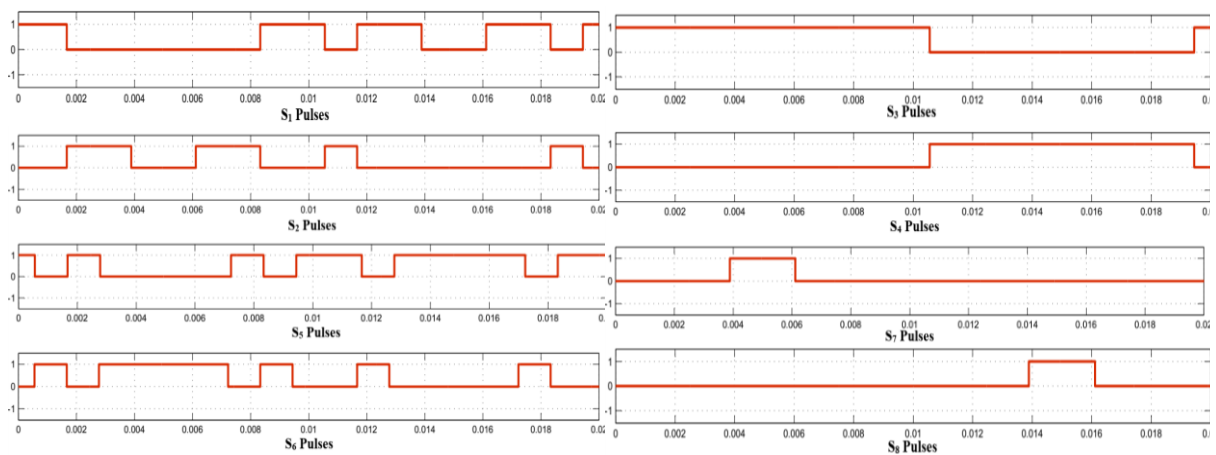
Figure 11. Pulses of the 8 switches of asymmetrical (2S-9L-8SW) MLI

A new topology of multilevel inverter with switches count reducing … (Mohammed D. Albakhait)

The FFT analysis of output current is shown in Figure 15, the fundamental harmonic is 11.8 A with THD is equal to 14.27%, most of this distortion is due to odd multiples harmonics of the fundamental harmonic. This value of THD is reduce by inductive load. However, the current waveform has been shown clearly in FFT analysis at Figure 16. The recorded THD in the output current is equal to 6.12%, most of this THD due to odd harmonics of fundamental harmonic.
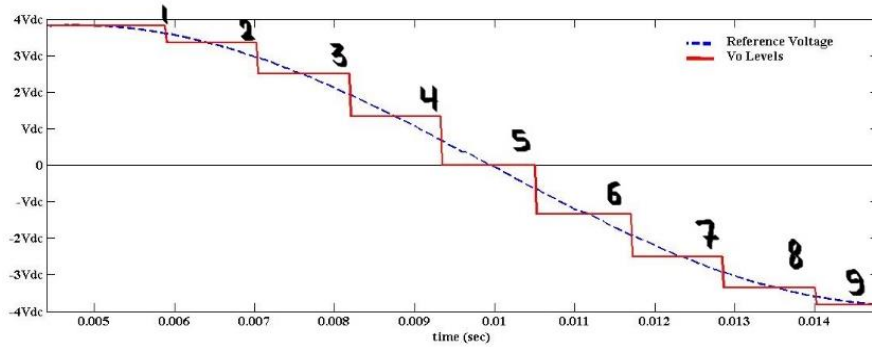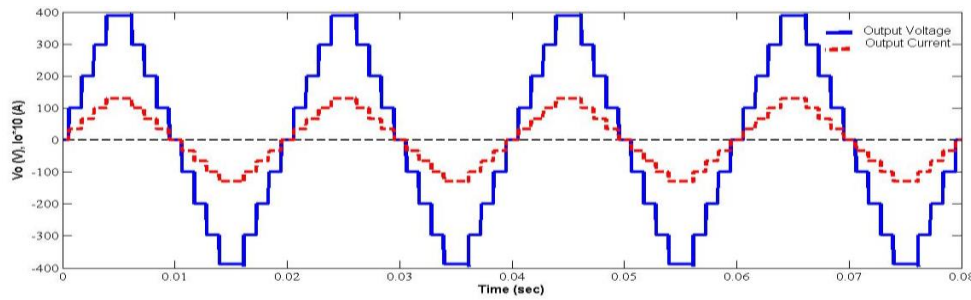
Figure 12. NLCM of asymmetrical (2S-9L-8SW) MLI

Figure 13. Output voltage and current waveform of asymmetrical (2S-9L-8SW) MLI at (R = 30 Ω)
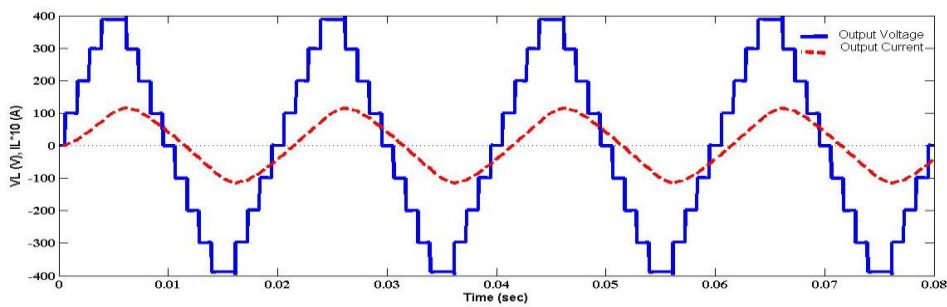
Figure 14. Output voltage and current of asymmetrical (2S-9L-8SW) MLI at (R=30 Ω, L = 45 mH)
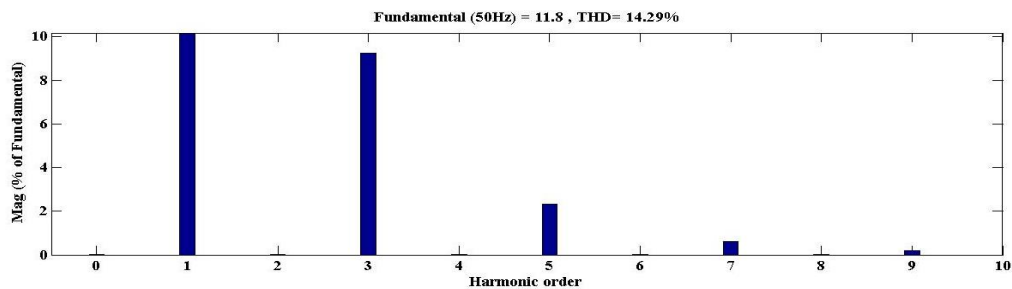
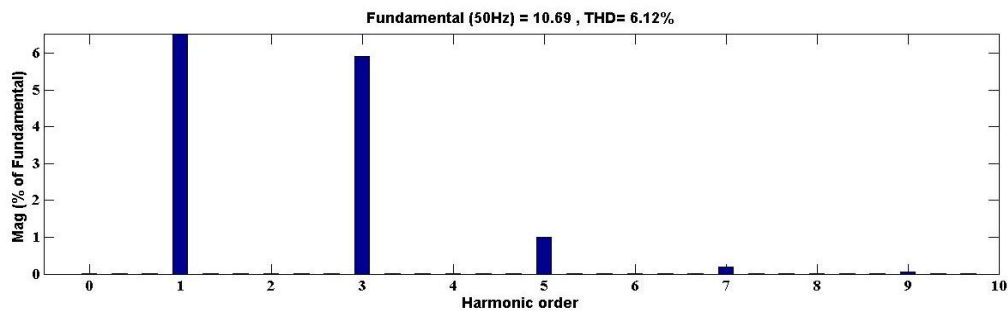Figure 15. FFT analysis of output voltage of asymmetrical (2S-9L-8SW) MLI at (R = 30 Ω)

Figure 16. FFT analysis of Io of asymmetrical (2S-9L-8SW) MLI at (R=30 Ω, L=45 mH)

6. CONCLUSION

This paper presented a new topology for the MLI. The proposed topology takes into account the importance of reducing the switches of power circuit while increasing the number of levels in the output. The proposed circuit has produced nine/five levels of output for the asymmetric/symmetric operation condition respectively, with reducing number of switches in half, no need for capacitors and with two asymmetric or symmetric DC sources. As a reminder, reducing the number of switches results in a reduction in the number of drive circuits, less complexity, in addition to reducing its size and lowering its cost. On the other hand, the lack of need for capacitors saved us from the complications and problems of voltage distribution and balancing it between these capacitors. The circuit was modeled using MATLAB environment, and the circuit was operated under both resistive and inductive loads. The effect of the presence of inductive reactance is observed on reducing the THD in the output current to (3.52%, 6.12%) in the symmetric and asymmetric operation modes respectively. This proposed model can be developed to reach a greater number of levels in the output, thus more reducing in THD by adding more DC links and switches.

REFERENCES

[1]   M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, pp. 58584–58594, 2019, doi: 10.1109/ACCESS.2019.2914430.
[2]   C. Kannan, N. K. Mohanty, and R. Selvarasu, "A new topology for cascaded H-bridge multilevel inverter with PI and Fuzzy control," *Energy Procedia*, vol. 117, pp. 917–926, Jun. 2017, doi: 10.1016/j.egypro.2017.05.211.
[3]   M. S. Hasan, A. F. Sharaf, M. D. Albakhait, and A. I. Jaber, "High performance rectifier/multilevel inverter based BLDC motor drive with PI controller," *IOP Conference Series: Materials Science and Engineering*, vol. 745, no. 1, p. 12005, Feb. 2020, doi: 10.1088/1757-899X/745/1/012005.
[4]   A. M. Noman, A. A. Al-Shamma'a, K. E. Addoweesh, A. A. Alabduljabbar, and A. I. Alolah, "Cascaded multilevel inverter topology based on cascaded h-bridge multilevel inverter," *Energies*, vol. 11, no. 4, p. 895, Apr. 2018, doi: 10.3390/en11040895.
[5]   A. Masaoud, H. W. Ping, S. Mekhilef, A. Taallah, and H. Belkamel, "Design and implementation of a new multilevel DC-link three-phase inverter," *Journal of Power Electronics*, vol. 14, no. 2, pp. 292–301, Mar. 2014, doi: 10.6113/JPE.2014.14.2.292.
[6]   M. Q. Kasim and R. F. Hassan, "Active voltage balancing strategy of asymmetric stacked multilevel inverter," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 23, no. 2, pp. 665–674, Aug. 2021, doi: 10.11591/ijeecs.v23.i2.pp665-674.
[7]   W. A. Halim, S. Ganeson, M. Azri, and T. N. A. T. Azam, "Review of multilevel inverter topologies and its applications," *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, vol. 8, pp. 51–56, 2016.
[8]   M. Rasheed, R. Omar, M. Sulaiman, W. A. Halim, and M. M. A. Alakkad, "Analysis of a switching angle calculation by ANN for nine level inverter apply into experimental case study with elimination of lower and higher order harmonics," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 20, no. 2, pp. 948–959, Nov. 2020, doi: 10.11591/ijeecs.v20.i2.pp948-959.
[9]   D. Karthikeyan, K. Vijayakumar, D. S. Kumar, and D. Krishnachaitanya, "Mathematical analysis of cost function and reliability condition for new proposed multilevel inverter topology," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 20, no. 2, pp. 654–661, Nov. 2020, doi: 10.11591/ijeecs.v20.i2.pp654-661.
[10]   M. D. Siddique *et al.*, "Low switching frequency based asymmetrical multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 86374–86383, 2019, doi: 10.1109/ACCESS.2019.2925277.
[11]   G. Sagarbabu, M. Prasad, and V. Jagathesan, "Multilevel DC-link inverter topology with less number of switches," *Ripublication.Com*, vol. 4, no. 1, pp. 67–72, 2014, Accessed: Mar. 11, 2022. [Online]. Available: http://www.ripublication.com/aeee_spl/aeeev4n1spl_10.pdf
[12]   R. F. Abdelgoui, R. Taleb, A. Bentaallah, and F. Chabni, "Improved hybrid algorithm based on GA and local search method for asymmetrical 9-level inverter," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 21, no. 3, pp. 1309–1316, Mar. 2021, doi: 10.11591/ijeecs.v21.i3.pp1309-1316.
[13]   T. Brückner, S. Bernet, and H. Güldner, "The active NPC converter and its loss-balancing control," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 855–868, Jun. 2005, doi: 10.1109/TIE.2005.847586.
[14]   C. I. Odeh and D. B. N. Nnadi, "Single-phase 9-level hybridised cascaded multilevel inverter," *IET Power Electronics*, vol. 6, no. 3, pp. 468–477, Mar. 2013, doi: 10.1049/iet-pel.2012.0199.
[15]   A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna PowerTech - Conference Proceedings*, 2003, vol. 3, pp. 6–11, doi: 10.1109/PTC.2003.1304403.

[16]   M. Rasheed, R. Omar, M. Sulaiman, and W. A. Halim, "Particle swarm optimisation (PSO) algorithm with reduced numberof switches in multilevel inverter (MLI)," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 14, no. 3, pp. 1114–1124, Jun. 2019, doi: 10.11591/ijeecs.v14.i3.pp1114-1124.

[17]   Y. R. Manjunatha and B. A. Anand, "Multilevel DC link inverter with reduced switches and batteries," *International Journal of Power Electronics and Drive Systems*, vol. 4, no. 3, pp. 299–307, Sep. 2014, doi: 10.11591/ijpeds.v4i3.4618.

[18]   D. Sankar and C. A. Babu, "Design and analysis of a novel quasi Z source based asymmetric multilevel inverter for PV applications," *International Journal of Power Electronics and Drive Systems*, vol. 11, no. 3, pp. 1368–1378, Sep. 2020, doi: 10.11591/ijpeds.v11.i3.pp1368-1378.

[19]   M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019, doi: 10.1109/ACCESS.2019.2890872.

[20]   A. Chlaihawi, A. Sabbar, and H. Jedi, "A high-performance multilevel inverter with reduced power electronic devices," *International Journal of Power Electronics and Drive Systems*, vol. 11, no. 4, pp. 1883–1889, Dec. 2020, doi: 10.11591/ijpeds.v11.i4.pp1883-1889.

[21]   R. Majdoul, A. Touati, A. Ouchatti, A. Taouni, and E. Abdelmounim, "A nine-switch nine-level converter new topology with optimal modulation control," *International Journal of Power Electronics and Drive Systems*, vol. 12, no. 2, pp. 932–942, Jun. 2021, doi: 10.11591/ijpeds.v12.i2.pp932-942.

[22]   M. Nandhini G, P. Ram Prakas, and M. Amarnath, "Performance evaluation of modified cascaded multilevel inverter," *Journal of Applied Sciences*, vol. 14, no. 15, pp. 1750–1756, Jul. 2014, doi: 10.3923/jas.2014.1750.1756.

[23]   P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano, and G. Panda, "Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: topologies, comprehensive analysis and comparative evaluation," *IEEE Access*, vol. 7, pp. 54888–54909, 2019, doi: 10.1109/ACCESS.2019.2913447.

[24]   J. R. Rahul and K. Annamalai, "Multistring seven-level quasi Z-source based asymmetrical inverter," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 15, no. 1, pp. 88–94, Jul. 2019, doi: 10.11591/ijeecs.v15.i1.pp88-94.

[25]   B. Ashok and A. Rajendran, "Selective harmonic elimination of multilevel inverter using SHEPWM technique," *International Journal of Soft Computing and Engineering (IJSCE)*, no. 3, p. 79, 2013.

[26]   J. K. Abed, M. J. Mnati, and B. M. Yaseen, "The effect of using filter on total harmonic distortion in multilevel inverter," *Journal of Engineering and Applied Sciences*, vol. 14, no. 1, pp. 13–20, Dec. 2019, doi: 10.36478/jeasci.2019.13.20.

[27]   F. Umbría, F. G.-Estern, F. Gordillo, and F. Salas, "Voltage balancing in five-level diode-clamped power converters," *IFAC Proceedings Volumes (IFAC-PapersOnline)*, vol. 9, no. PART 1, 2013, pp. 365–370, doi: 10.3182/20130904-3-FR-2041.00166.

[28]   S. F. V. Rose and B. V. Manikandan, "Simulation and implementation of multilevel inverter based induction motor drive," *2009 International Conference on Control Automation, Communication and Energy Conservation, INCACEC 2009*, 2009, Accessed: Mar. 11, 2022. [Online]. Available: www.ijedr.org

BIOGRAPHIES OF AUTHORS

Mohammed D. Albakhait 🆔 Ⓖ SC Ⓟ recived his B.Sc from Univerity of Mosul/Iraq 2008 from Power and Electrical Machines Department, M.Sc from University of Mosul/Iraq. 2011 in Power Electronics specification. He is currently Assist Lecturer in Dept. of Electrical Power Engineering Techniques/Electrical Engineering Technical College/Middle Technical University. He can be contacted at email: mohammedalbakhait@mtu.edu.iq.

Arwa Amer Abdulkareem 🆔 Ⓖ SC Ⓟ recived his B.Sc from Middle Technical University/Iraq 2005 from Electrical Power Engineering Techniques Dept., M.Sc from Middle Technical University/Iraq 2008 in Electrical power Engineering. She is currently Assist Lecturer in Dept. of Electrical Power Engineering Techniques/Electrical Engineering Technical College/Middle Technical University. She can be contacted at email: eleceng.aamer@gmail.com.