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A simple architecture for high performance class-D audio amplifier with novel RC network as negative feedback loop

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ABSTRACT

In this work, we have designed and simulated a proposed architecture and good performances single-ended class-D audio amplifier (CDA). The proposed circuit is build using pulse-width modulation (PWM). We have proposed a novel RC network as negative feedback loop attached to a second-order integrator to get free of high-frequency carrier ripples and to reach improved output accuracy, thus improved performance and efficiency. This proposed negative feedback loop extremely reduces total harmonic distortion plus noise (THD+N). We have used a passive second-order butterworth output filter. This circuit fulfills a power supply rejection ratio (PSRR) of 75 dB, a THD+N of 0.004%, 3 times less than attained by usual feedback loop. The proposed circuit with quiescent current of 0.02 mA, signal to noise ratio (SNR) of 89 dB, and peak efficiency of 90% is running at 400 kHz switching frequency. The results of simulation demonstrate that this circuit significantly keeps up with the performance of other circuits but taking advantage of its simple architecture.

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1. INTRODUCTION

Class-D amplifiers are likewise exceedingly known as “pulse-width modulation (PWM) amplifiers”, “switching amplifiers” as well, “digital amplifiers”. They are intended for audio signals power amplification, employing various principle of operation compared to traditional amplifiers. Traditional amplifiers (class A, B, and AB) rely on linear mode, adapt the processed signal to the required level and load impedance, class-D amplifiers do same process, depend on pulse width modulation technique [1]. In traditional audio amplifiers, better linearity is obtained but in return, poorer power efficiency, thus their applications are bounded [2]-[4]. The efficiency of class-D amplifiers exceeded the traditional amplifiers one, thus they have become prevalent in recent years. In addition to provide high efficiency, they’re distinguished by low power consumption [5]. In class-D amplifiers, PWM is the most common and the most used. It provides simple and stable circuitry with low power consumption [6]. With regard to class-D amplifier, since its output stage composed of switches (MOSFETs in our case) that operate in on/off mode, efficiency over than 80% is achieved [7]. Basically, class-D audio amplifier (CDAs) are becoming preferred and catchy for many applications used in smartphones and others to extend battery life [8], [9].

An audio amplifier delivers its audio electrical signal to a transducer (load): EM/PZ speaker [10]. As the preferred transistor in modern electronics is the MOSFET, it is then widely used in the CDA output stage as a switch delivering power supply current to the load (speaker) via simple filter. Thus, the amplifier efficiency is related to MOSFET total power losses.

Class-D amplifiers based on PWM to output switching signal. Due to low power dissipation and simple architecture, PWM is the most used in class-D amplifier designs, based on generating high/low pulsing waveform train. It is deemed most compatible modulation to reduce harmonic [11]. This is the reason behind using it in many other applications [12], [13]. In PWM-based CDA, the input signal is compared with much higher frequency triangle reference waveform to acquire accurate audio signal. The carrier signal high frequency f_{sw} is 0.1 MHz<f_{sw}<1 MHz and the audio sinusoidal signal frequency f_a is 20 Hz<f_a<20 kHz [14], [15].

Figure 1 depicte s a closed-loop class-D amplifier basic design. It composes of filters and integrator, a modulator, switches, and a load. Filters and integrator improve total harmonic distortion (THD) [14], in the loop: decrease and get rid of undesirable carrier components and provide steady gain. The modulator provides pulse width modulated train by modulating the input signal, which serves as a switch manipulator of the power (output) stage. The power stage provides adequate power to run both load and low pass (LP) filter [16] and the MOSFETs switches should be carefully selected as the major portion of the distortion is caused ofen, by the power amplifier [17].

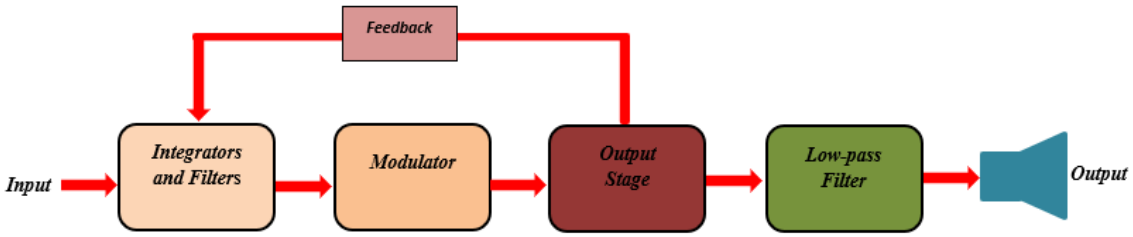

Figure 1. A closed-loop class-D amplifier block diagram

2. PROPOSED CIRCUIT

The proposed CDA circuit is depicted in Figure 2. It composes of: i) An input sine wave which represents the audio signal with 20 kHz bandwidth; ii) A second-order integrator with increased bandwidth to improve THD; iii) A comparator with low propagation delay t_{pd} compared to PWM period T_{PWM} (t_{pd}<<T_{PWM}); iv) A triangular carrier wave with high performances especially in terms of linearity; v) Two gate drivers based on bipolar technology: level-shifted for P-channel MOSFET and totem-pole driver for N-channel MOSFET; vi) A power stage consists of two MOSFETs with low on-resistance ($R_{DS(on)}$) compared with the input impedance of the output filter; vii) A low-pass second-order LC filter which theoretically consumes zero active power; viii) A proposed negative RC network as feedback loop and as high-frequency (f>>f_{PWM}) stopping filter through the low output resistance of the switching circuit; and ix) A resistive load as low power speaker.

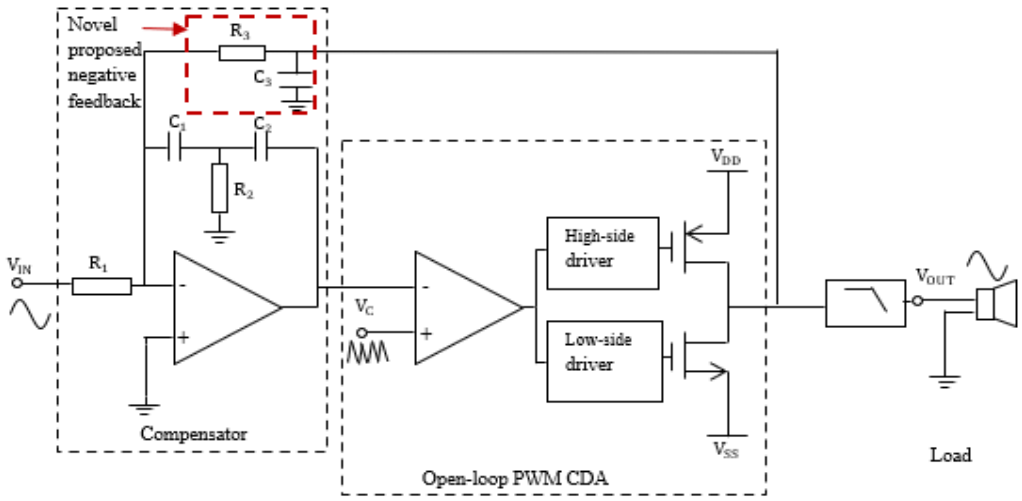

Figure 2. Architecture of the proposed circuit

Its mechanism work could be explained as: the feedback signal is compared with the input signal, using a second-order integrator, to produce an error signal. The comparator input terminals are connected to the error signal and to the carrier (high-frequency triangular signal) to compare together and produce a switch manipulator signal to drive the switching stage which drives load and LC filter [18].

This proposed audio amplifier operates with power supplies ± 3 V and gives 90 mW RMS output power. The chosen comparator is MAX942, it combines high speed, low power and rail-to-rail input. We used a low power amplifier TL061 to build second-order integrator. The power stage composes of fast-switching NMOS and PMOS MOSFETs, IRF520 and IRF9530. We used bipolar transistors: 2N3904 and 2N3906 to build gate drivers. The proposed architecture reduces overlapping of MOSFETs inputs, guarantees power, and voltage-level adaptation and decreasing switching time by conveniently discharging different MOSFETs capacitors. The picked MOSFET transistors have very small "on" output resistance and small gate capacitance which guarantee low dissipation in portable applications [19].

The PWM logic level would not be enough to fully turn on a used power device, thus an interface is requisite between the logic/control circuitry and the power device. A high ability gate driver enables fast switching so decreases switching power loss and drives to a more effective system [20]. The PWM must be level shifted for one of the MOSFETs. For the PMOS, the PWM has to be shifted to a level above the switching stage supply voltage to ensure it is in the cut-off region. We have used a bipolar junction transistor (BJT) driver.

The totem-pole is one of the most popular and cost-effective driver. It handles the current spikes and power losses, making it more favorable for PWM technique. It decreases the turn on/off time of the N-MOSFET, increases the gate flowing current and gives quicker charging to the gate capacitor. The level-shifter output resistance is greater than that of the totem-pole. This makes charging/discharging times of MOSFET capacitors different and contributes in reducing crossover problem.

As depicted in Figure 2, the proposed feedback loop consists of a resistor and a capacitor. It is used as a negative feedback loop added to second-order integrator provided with two capacitors and a resistor. It operates as a low-pass filter for undesirable high frequencies. This novel proposed closed-loop attenuates extremely the total harmonic distortion plus noise produced by power stage. Also, improves the power supply rejection ratio, attenuates non-linearities and non-idealities, the pulse-height errors, and ripples. The transfer function of the compensator is given by (1).

$$G_C(s) = -\frac{R_2(R_1+R_3)(C_1+C_2)s+R_1+R_3}{R_1R_2R_3C_1C_2s^2} \quad (1)$$

The butterworth low-pass second-order filter is with about 18 kHz cut-off frequency. This filter eliminates undesirable signals above audio frequencies and recaptures the original audio signal. Its transfer function is given by (2).

$$G_F(s) = \frac{1}{LCs^2+\frac{L}{R}s+1} \quad (2)$$

3. RESULTS AND DISCUSSION

This low-power second-order PWM class-D audio amplifier was simulated using OrCad-PSpice, the target was to achieve high performance and high efficiency. We used Matlab to get results. Obtained results are summarized in figures and tables. Figure 3 illustrates the output signal spectrum. The lowlest THD+N is 0.004%, obtained at 1 kHz and attains its maximum at 10 kHz with 0.03%. The harmonics above 20 kHz could be easily filtred.

Figure 4 depicte s the output voltage. The drop in this voltage in comparison to the full dynamic range is due the output impedance of the LP filter which also includes the effect of the R_{DSon} resistance and mainly the closed-loop. The input signal features: 1 kHz input frequency/0.9 modulation index. Figure 5 illustrates the variation of THD+N versus input frequency. The THD+N is 4×10-5 at 1 kHz and then amounts to its extreme at 10 kHz. Figure 6 shows the comparison between proposed novel negative feedback and usual negative feedback loops of THD+N. The THD+N is 4×10-5 at 1 kHz with novel feedback loop and 1.1×10-4 at 1 kHz with usual feedback loop. From Figure 6, we could perceive obviously the considerable difference between the proposed novel feedback and the usual feedback. The novel feedback loop gives reduced THD+N, less than the obtained by the usual one almost 3 times @1 kHz. Since the human ear could hear between 20 Hz and 20 kHz but it's really most sensitive to what occurs between 250 Hz to 5 kHz, consequently, the novel proposed feedback loop is better in every way. Signal to noise ratio is almost constant with a value of 89 dB and only softly decreases above 10 kHz input frequency as shown in Figure 7. The signal to noise ratio (SNR) is softly inversely symmetrical to the input frequency. This may indicate that

the noise can be modeled by a power function. Power supply rejection ratio (PSRR) versus frequency is presented in Figure 8, where 100 mV_{pp} of ripple voltage is superimposed the power supply. It is inversely proportional to Log(f) and it is possibly the effect of CR filter of the integrator. The variation of the efficiency versus modulation index is depicted in Figure 9. It is the image of the power consumed by the resistive charge R_L. It presents an exponential function and amounts to its extreme at around 0.5.

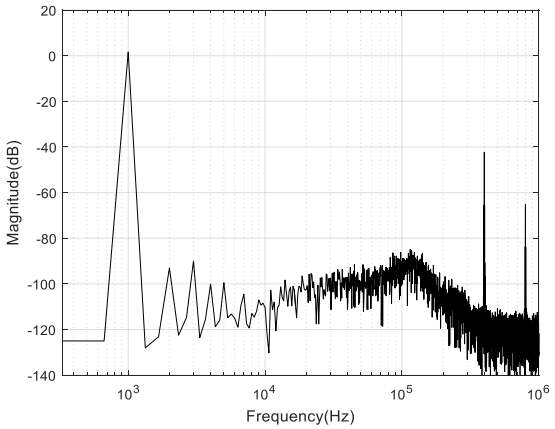

Figure 3. Output signal spectrum

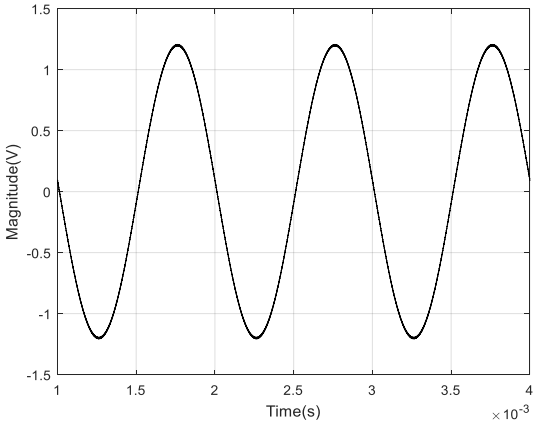

Figure 4. Output voltage (2.4 V_{pp})

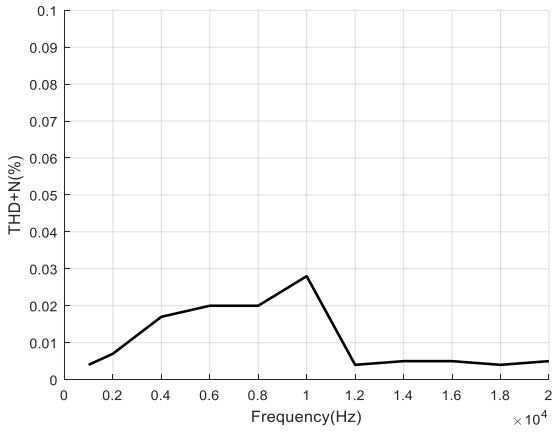

Figure 5. THD+N versus input frequency with novel proposed feedback loop

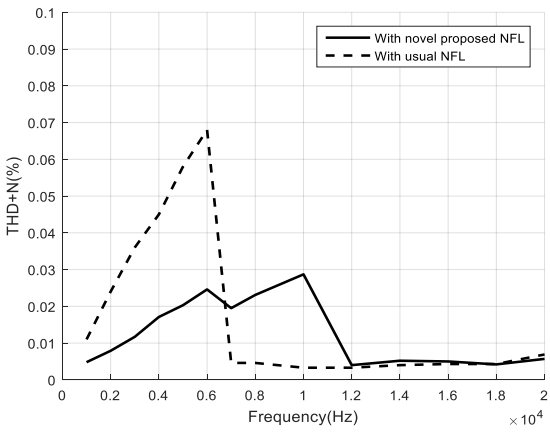

Figure 6. Comparison of THD+N versus input frequency

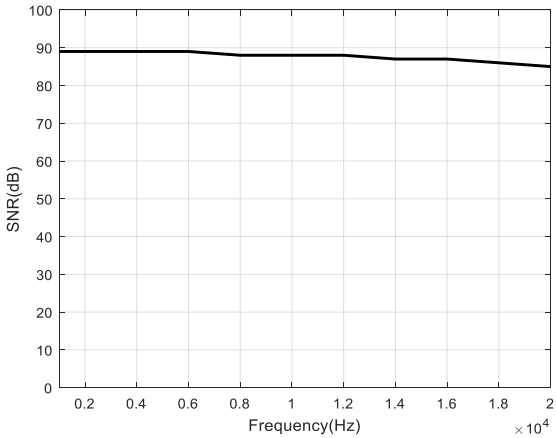

Figure 7. SNR versus input frequency

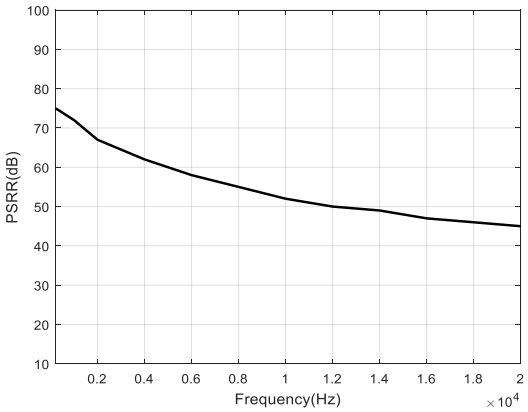

Figure 8. PSRR versus input frequency

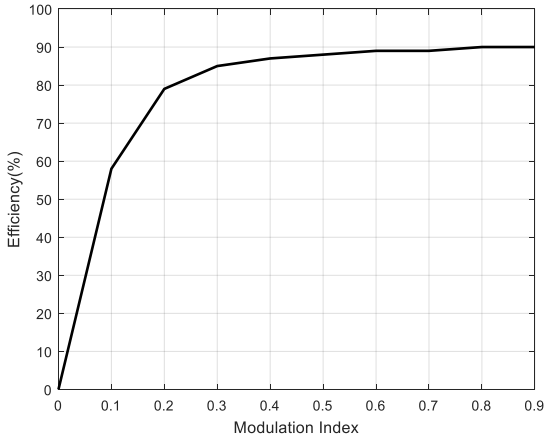

Figure 9. Efficiency versus modulation index

3.1. Simulink results

The proposed circuit is modeled with a closed-loop linear model and simulated with Simulink. Figures 10 and 11 present the model and the bode plot for the resulting linear model. Where K_i (i=1:5) are functions of circuit elements. At frequencies below cut-off frequency, it is a horizontal line at almost 0 dB, and at high frequencies it is 60 dB/decade attenuation.

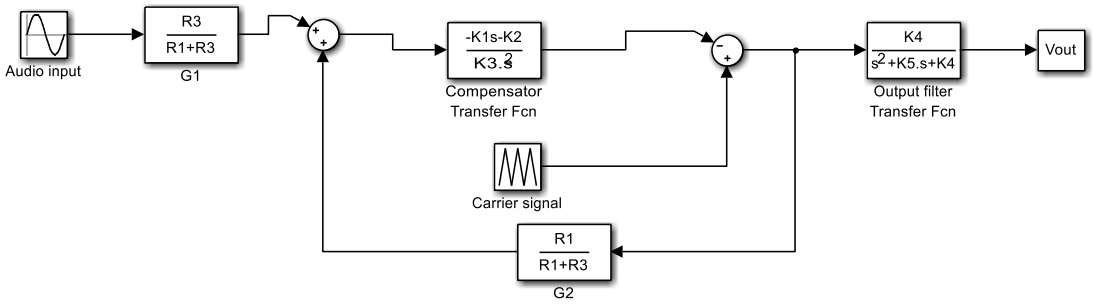

Figure 10. Matlab Simulink of proposed circuit

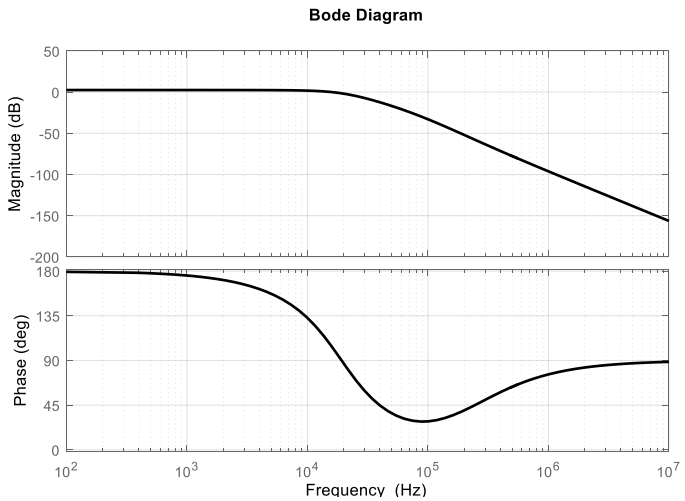

Figure 11. Simulink results of proposed circuit

To show the effectiveness of our proposed circuit, we compared our results to others in literature. Results are recapitulated below in Table 1. Our architecture is effective and smooth.

Table 1. Performance comparison

Parameter	This work	[21]	[22]	[23]	[24]	[25]	[26]
THD+N (%) at 1 kHz	0.004	0.018	0.01	0.01	0.7	0.06	0.02
SNR (dB)	89	92	97	-	84	-	-
PSRR (dB) at 217 Hz	75	88	70	90 (at 1 kHz)	60	-	80
f_{sw} (kHz)	400	320	450	2300	384	48	300
Efficiency (%)	90	85.5	90	86	88	90	90

4. CONCLUSION

For the purpose of fulfillment high performance, we have designed and simulated a class-D audio amplifier circuit. We proposed a novel RC network which remarkably decreases THD+N: 3 times less than usual negative feedback loop, ameliorates the PSRR and improves performance. The proposed circuit shows good results scheduled above with comparison to other works in literature, with taking advantage of its simple designed architecture.

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