Indonesian Journal of Electrical Engineering and Computer Science
Vol. 24, No. 2, November 2021, pp. 689~696
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v24.i2.pp689-696

High gain multiphase boost converter based-on capacitor clamping structure

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Article Info

Article history:

Received Jun 14, 2021
Revised Aug 31, 2021
Accepted Sep 4, 2021

Keywords:

Capacitor clamping structure
DC-DC converter
High voltage gain
Multiphase boost converter

ABSTRACT

In the last few years, the non-isolated dc converters involving high voltage gain with adequate performance are becoming quite popular in industrial applications. This is resulting in high voltage and current stress on the power device (switches and diodes), as well as a limited output voltage with a high duty cycle. This paper proposes a multi-phase non-isolated boost converter that uses capacitor clamping to increase output voltage while reducing stress across the power device. There are two stages in the proposed converter (first stage is three inductors and three switches and the second stage is clamper circuit of three capacitors and three diodes). The proposed converter is high voltage gain, with low voltage stress through switches transistors. To justify the theoretical analysis, the concept was validated through mathematical analysis and by simulation using MATLAB/SIMULINK. The results carried out the results permit the converter behavior and performance to be accurately.

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1. INTRODUCTION

Due to its sustainable and endless source supply nature, renewable energy sources (photovoltaic, fuel cells, and uninterruptible power supply (UPS)) are developed continuously and swiftly replenished, and it is employed in remote places. The output voltage of these energy sources is still much lower than a direct current (DC) system requirement [1]-[3]. On the other side The large input current ripple, on the other hand, shortens the lifetime of photovoltaic (PV) and fuel cells [3]-[5]. High current ripple and unregulated low voltage are two major drawbacks of adopting renewable energy sources. As a result, in recent years, numerous approaches have been presented to achieve high voltage gain, reduced current ripple, component size reduction, and increased efficiency [1]-[25].

The traditional boost converter concept can be thought of as a basic key to suggesting a DC voltage boosting device. The typical boost converter, on the other hand, has some shortcomings, such as high input current ripple, voltage gain limitation, high current stress, and low efficiency. Another disadvantage of standard DC converters is that they have the biggest conduction losses due to the switching system, which is a major issue that affects the converter output power [6]-[8]. The used of high frequency pulsewidth modulation (PWM) topology is very important to increase voltage gain, reduce losses, ripple and component siz [9]-[11].

The multiphase switching inductors technique used as first stage is essentially a mix of three ordinary DC converters connected in a parallel layout. Because of the benefit of current redistribution among the phases, this configuration can reduce output voltage and input current ripple but the voltage conversion ratio still the same of conventional converter. Because the input current is shared according to multiphase in parallel, the multiphase switching approach has a faster transient response due to low switching losses. This benefit reduces their switching losses, increasing efficiency, and it also reduces current stress. In addition, due to the input distributed current, the size and component rating are lowered [12]-[15].

Using a clamper capacitor circuit in the second stage provides the following advantages:

a) A huge voltage spike was limited across switches by the passive clamp function [16].
b) Low voltage stress, high voltage gain and low input current ripple [17]-[20].
c) There is extra gain adding to main dc boost converter [21]-[25].

This paper offers a three-channel boost converter DC converter based on a capacitor clamping circuit. The capacitor clamping side achieves the high voltage gain. This design will provide low ripple at the input (current and voltage) and output (current and voltage) sides, as well as minimize switch element stress to the (Vout/3) lowerthan the output voltage.

2. THREE PHASE BOOST CONVERTER BASED-ON CAPACITOR CLAMPING OPERATION IN (CCM) MODE

Figure 1 is present the proposed converter. It is constituted by three channels inductors and capacitor clamping structure. The proposed converter consists of three shared inductors and switches that controlled by three PWM operation signals with 120-degree phase shift between them. The suggested converter has six modes of operation. The following is a discussion of the converter operating in continuous conduction mode during the steady state for one period.

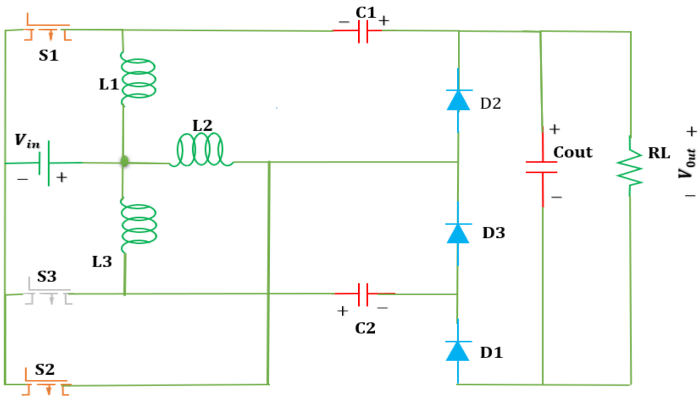

Figure 1. Proposed high gain multi-phase boost converter

a) Operational mode I: is shown in Figure 2. The three switches (S_1, S_2 and S_3) are turned ON. Thus, the diodes D_1, D_2 and D_3 tended to turn OFF (reverse bias state). This action causes storage energy in L_1, L_2, L_3. While C_{out} are discharged its energy towards to the load side.

$$V_{in} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = L_3 \frac{di_{L3}}{dt} \tag{1}$$

$$v_{c\,out} = v_o = R_L\, i_o \tag{2}$$

b) Operational mode II: is shown in Figure 3. Where S_1, S_3 keep ON while S_2 is turned OFF. So, the diodes D_1 and D_3 are reverse bias state. Whereas D_2 is in ON state (forward biased). In second mode the inductors L_1 and L_3 are stored energy with positive slope of $\frac{V_{in}}{L}$ where $L = L_1 = L_2 = L_3$. in the same time the supply energy V_{in} and the stored energy in L_2 are transfer energy in series to C_1 . Furthermore, C_{out} discharged its energy to R_L in series.

$$V_{in} = L_1 \frac{di_{L1}}{dt} = L_3 \frac{di_{L3}}{dt} \tag{3}$$

$$V_{in} - L_2 \frac{di_{L2}}{dt} - V_{c1} = 0 \tag{4}$$

$$V_{Cout} = R_L\, i_o = V_o \tag{5}$$

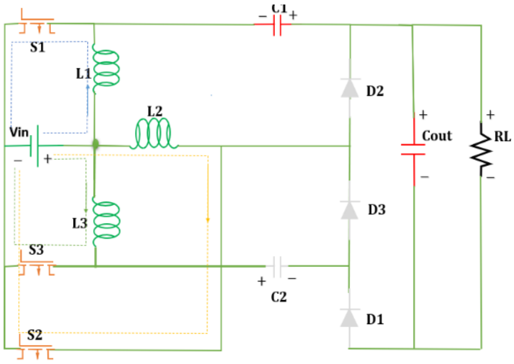

Figure 2. Mode 1, mode 3, and mode 5

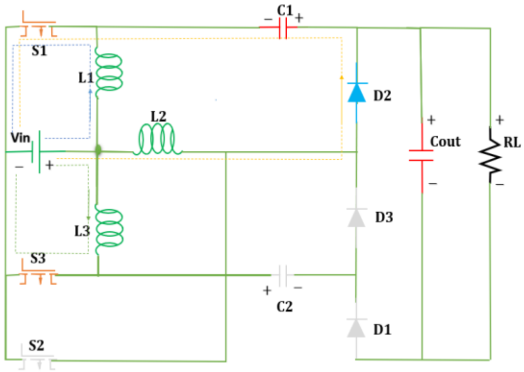

Figure 3. Mode 2

c) Operational mode III: (S_1, S_2 and S_3) are ON state. So, is equivalent to mode I.

d) Operational mode IV: is shown in Figure 4. S_3 Is turned off while $S_1$and S_2 keep turning-on. So, the diodes$D_1$and D_2 are reverse bias state. Whereas $D_3$is in ON state (forward biased). In fourth mode the inductors $L_1$and L_2 are stored energy with positive slope of $\frac{V_{in}}{L}$ where $L = L_1 = L_2 = L_3$. in the same time the supply energy V_{in} and the stored energy in L_3 are transfer energy in series to C_2 . Furthermore, C_{out} discharged its energy to R_L in series.

$$V_{in} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} \tag{6}$$

$$V_{in} - L_3 \frac{di_{L3}}{dt} - V_{C2} = 0 \tag{7}$$

$$V_{Cout} = R_L\, i_o = V_o \tag{8}$$

e) Operational mode V: S1, S2 and S3 all are on. The operating principle is same as mode I.

f) Operational mode VI: As shown in Figure 5. The modes of operation waeforms shown in Figure 6. Where S_1 is turned off while $S_2$and S_3 keep turning-on. So, the diodes$D_2$and D_3 are reverse bias state. Whereas $D_1$is in ON state (forward biased) in sixth mode the inductors $L_2$and L_3 are stored energy with positive slope of $\frac{V_{in}}{L}$ where $L = L_1 = L_2 = L_3$. in the same time the supply energy V_{in} and the stored energy in L_1 are transfer energy in series with V_{c1} and V_{C2} transfer energy to C_{out} and in the same time to R_L.

$$V_{in} = L_2 \frac{di_{L2}}{dt} = L_3 \frac{di_{L3}}{dt} \tag{9}$$

$$V_{in} - L_1 \frac{di_{L1}}{dt} - V_{C1} - V_{C2} + V_{Cout} = 0 \tag{10}$$

$$V_{Cout} = R_L\, i_o = V_o \tag{11}$$

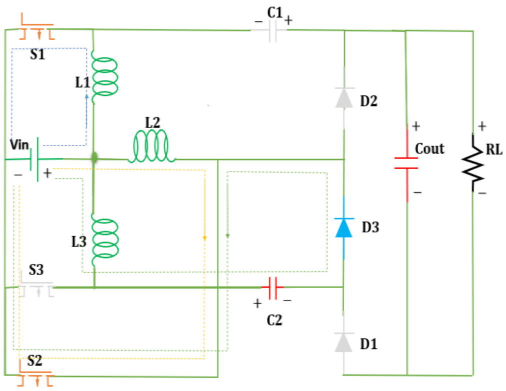

Figure 4. Mode 4

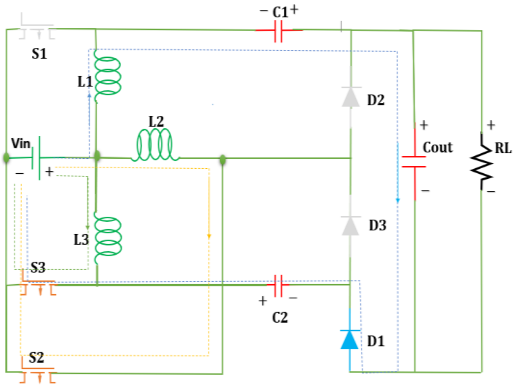

Figure 5. Mode 6

3. PROPOSED CONVERTER STEADY-STATE ANALYSIS

3.1. Voltage gain

According to volt-second balance principle on L_1., can be obtained:

$$V_{Lavg} = V_{in} * t_{on} + (V_{in} - V_{c1}) * t_{off} = 0 \quad where\ t_{on} = D \quad , \quad t_{off} = (1 - D)$$

$$V_{Lavg} = DV_{in} + (1 - D)(V_{in} - V_{c1}) = 0$$ Where: D: on period, (1-D): off period.

$$V_{in} - V_{c1}(1 - D) = 0 \quad so \quad V_{c1} = \frac{V_{in}}{1-D} \tag{12}$$

Also, according to volt-second balance principle on inductor L_3 the capacitor 2 voltage as shown (13):

$$V_{Lavg} = DV_{in} + (1 - D)(V_{in} - V_{c2}) = 0$$
$$V_{in} - V_{c2}(1 - D) = 0 \quad so \quad V_{c2} = \frac{V_{in}}{1-D} \tag{13}$$

At last, according to volt-second balance principle on inductor L_2 the output capacitor voltage as shown (14):

$$V_{Lavg} = V_{in} * t_{on} + (V_{in} - V_{Cout} + V_{c1} + V_{c2}) * t_{off} = 0 \qquad t_{on} = D \quad , \quad t_{off} = (1 - D)$$
$$V_{Lavg} = DV_{in} + (1 - D)(V_{in} - V_{Cout} + V_{c1} + V_{c2}) = 0$$
$$V_{Cout} = V_{in}/(1 - D) + (V_{c1} + V_{c2}) \tag{14}$$

By sub 12 & 13 in 14 we get:

$$V_O = V_{Cout} = \frac{V_{in}}{1-D} + (V_{c1} + V_{c2}) = \frac{V_{in}}{1-D} + \frac{V_{in}}{1-D} + \frac{V_{in}}{1-D}$$
$$V_O = 3\frac{V_{in}}{1-D} \tag{15}$$

3.2. Input current ripple

The input current for the proposed converter will distributed among three inductors L_1, L_2, L_3 with phase shift of 120 degree in switches operation between switches. Therefore, the operatetion frequency of the input current will be three times than operation frequency of switching Figure 6.

$$\Delta I_{in} = \frac{3V_{in}D}{LF_{sw}} \tag{16}$$

3.3. Output voltage ripple

The output voltage ripple can be reduced by the proposed converter because of the output frequency three times than the input frequency as shown in Figure 6:

$$V_{ripple} = \frac{\Delta V_o}{V_o} = \frac{D}{3F_{sw}CR_L} \tag{17}$$

3.4. Semiconductor voltage stress

3.4.1. Voltage stress across the switches

From mode 2, mode 4 and mode 6 the voltage stress across switches S_3, S_2, and S_1 as shown in Figure 6.

$$V_{S2\,stress} = V_{S1\,stress} = V_{S3\,stress} = \frac{V_{in}}{1-D} = \frac{V_o}{3} \tag{18}$$

3.4.2. Voltage stress across the diodes

The voltage stress across diode when diode be in reverse biasing, and it explained below:

- Voltage stress across D_1 pass in two stages: Stage 1 in mode 2 and Stage 2 in the mode 4.

$$V_{D1\,stress} = V_{Cout} - (V_{C1} + V_{C2}) = \frac{V_{in}}{1-D} = \frac{V_{out}}{3} \tag{19}$$

$$V_{D1\,stress} = V_{Cout} - V_{C1} = V_{D1\,stress} = \frac{2V_{in}}{1-D} = \frac{2V_{out}}{3} \tag{20}$$

- Voltage stress across D_2 pass in two stages: Stage 1 in the mode 4 and Stage 2 in the mode 6.

$$V_{D2\ stress} = V_{C1} = \frac{V_{in}}{1-D} = \frac{V_{out}}{3} \tag{21}$$

$$V_{D2\ stress} = V_{Cout} - V_{C2} = \frac{2V_{in}}{1-D} = \frac{2V_{out}}{3} \tag{22}$$

- Voltage stress across D_3 pass in two stages: Stage 1 in the mode 2 and Stage 2 in the mode 6.

$$V_{D3\ stress} = V_{C2} + V_{C1} = \frac{2V_{in}}{1-D} = \frac{2V_{out}}{3} \tag{23}$$

$$V_{D3\ stress} = V_{C2} = \frac{V_{in}}{1-D} = \frac{V_{out}}{3} \tag{24}$$

The voltage stress across diodes with respect to modes of operation are shown in Figure 6.

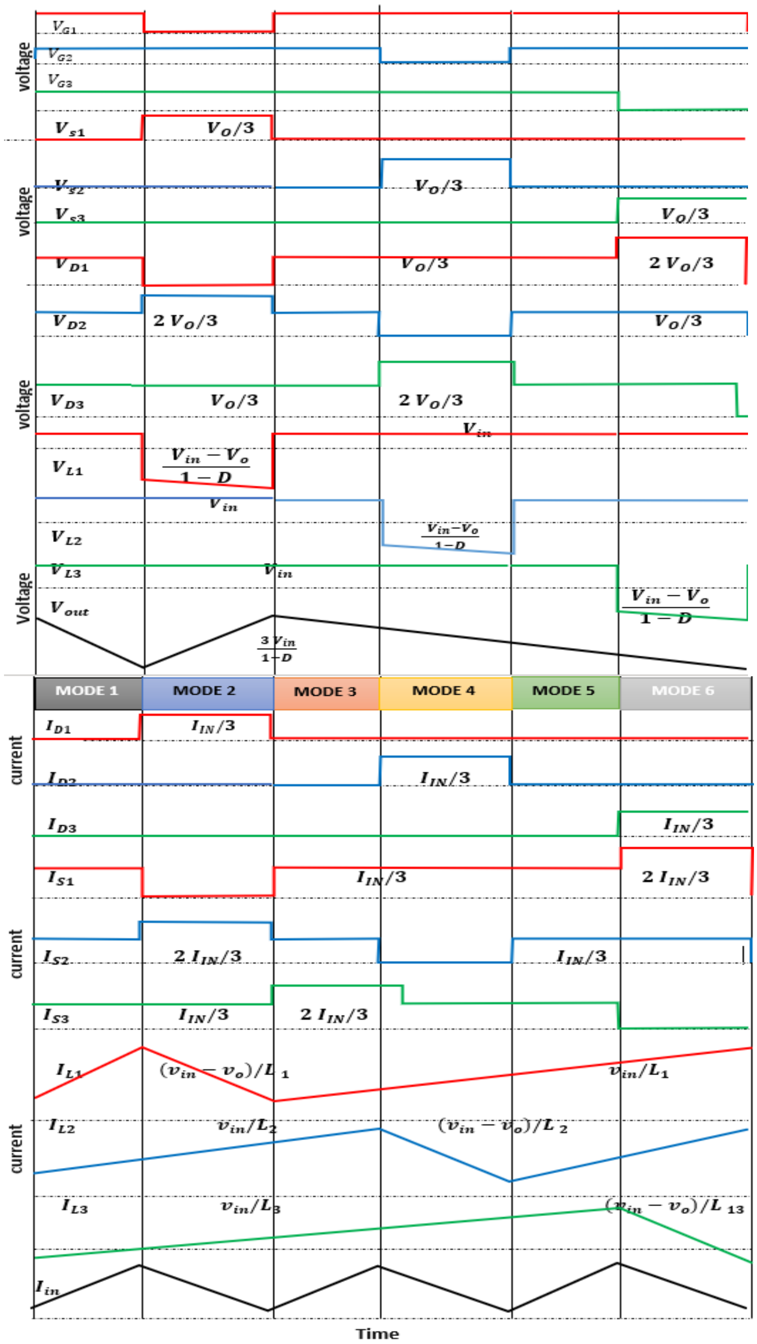

Figure 6. Key waveform for proposed converter

4. SIMULATION AND RESULTS

The use of MATLAB R2018B to simulate the proposed converter and converter parameter listed in Table 1. The three control signals with phase shift 120 degree shown in Figure 7. Output voltage is 480V as shown in Figure 8. The three inductors voltages waveform are shown in Figure 9 voltage stress across diodes is 160V as shown in Figure 10. The maximum voltage stress across switches is 320V as shown in Figure 11.

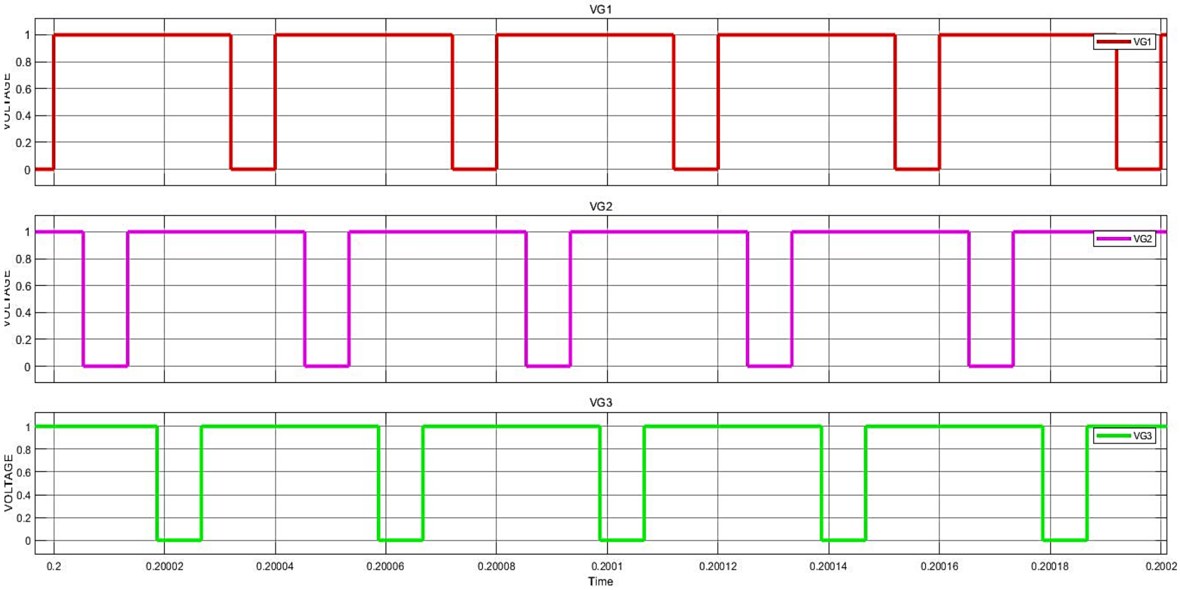

Figure 7. Power switches voltage control waveform

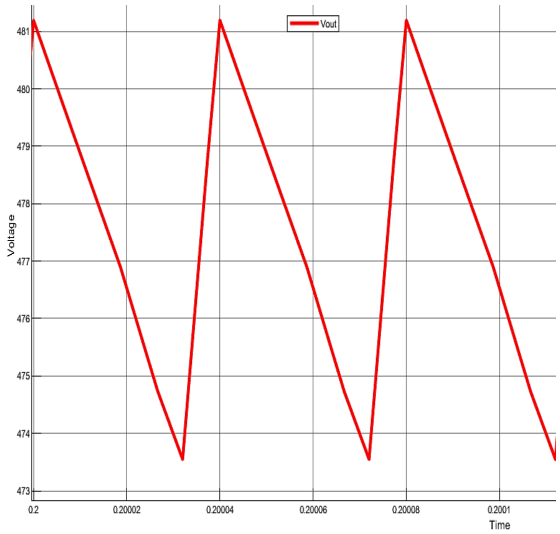

Figure 8.Output voltage waveform

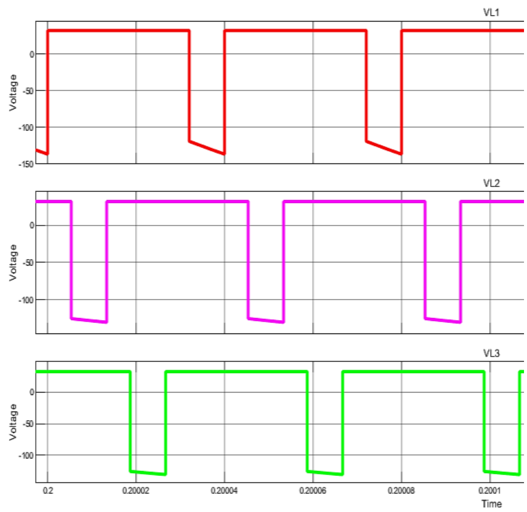

Figure 9. Inductors voltage waveform

Table 1. Parameter of the proposed converter

Parameter	Value
L_1, L_2, L_3	700 μH
C_1, C_2, C_3	20 μF
Load Resistance R_L	230 Ω
Switching Frequency - f_{sw}	25 kHz
Input Voltage	32 V
Output Voltage	480 V
Duty Cycle	80%

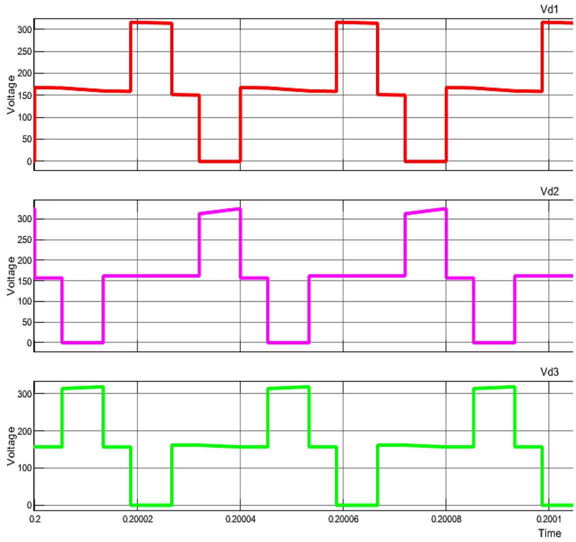

Figure 10. Voltage stress across switches waveform

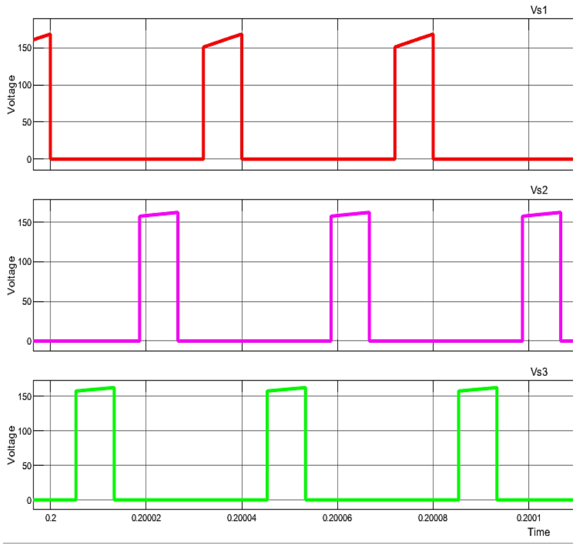

Figure 11. Voltage stress across diodes waveform

5. CONCLUSION

This paper presented a non-isolated DC-DC converter consist of two construction (three shared inductor and clamper capacitor circuit). This converter fed by single input source. The converter provides a high transformation ratio, lower voltage stress across power device (switches and diodes). The proposed converter suitable for power application where using renewable energy (P. V, Fuel cell and UPS) source. Because the input current of this source will be continuous and has lowest ripple. In this paper illustrated the analysis of the proposed converter and its design and checked it with MATLAB Simulation. The efficiency of proposed converter is 93%. Because of lower voltage stress across power device the total cost of converter will reduced.

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