

Design of high power amplifier based on wilkinson power combiner for wireless communications

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ABSTRACT

This article presents the design and fabrication of a high power amplifier based on wilkinson power combiner. A 45W basic amplifier module is designed using laterally-diffused metal-oxide semiconductor (LDMOS) field effect transistor (FET) PTFA260451E transistor. Wilkinson power combiner is used to combine two input powers to produce 90W of power. The proposed power amplifier is researched, designed and optimized using advanced design system (ADS) software. Experimental results show that the gain is 11.5 dB greater than at 2.45-3.0 GHz frequency band and achieving maximum power gain of 13.5 dB at 2.65 GHz centre frequency; output power increased to 49.3 dBm; Power added efficiency of 62.1% and good impedances matching: input reflection coefficient (S_{11}) < -10 dB, output reflection coefficient (S_{22}) < -15 dB. The designed amplifier can be used for 4G, 5G mobile communications and S-band satellite communication.

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1. INTRODUCTION

Power amplifier (PA) is an indispensable component in radio communication systems, especially in large distance communication systems such as satellites, mobile communication. PA is the most important block that amplifies the RF signal to power the antenna and provides the highest possible gain with the lowest possible reflectance. There have been many studies on designing and manufacturing power amplifiers performed in different frequency bands [1]-[25] and solving issues such as: increase power and efficiency [3], [6]-[8], [12], [16], increase circuit bandwidth and reduce intermodulation distortion [1], [5], [9]-[11], [13]-[15], [17]-[25].

Recently, different approaches to design high power and wideband PAs have been studied and proposed around the world. One of the most used research directions is to rely on multi-stage power amplifier circuit [5], [8], [16]. However, this method has low reliability, because when one of the power amplifiers fails, the system will not function. Other research directions are researched and suggested, in which the designs are based on parallel power amplifier with power divider/combiner [5], [10], [17].

Therefore, this paper focuses on increasing the power of an amplifier using a wilkinson power divider/combiner with a wide frequency band. To do this, two narrowband low-power amplifiers are designed and then combined using the power combiner. Figure 1 shows the block diagram of power amplifier.

In this case, the article use a 1:2 wilkinson power divider (WPD) and a 2:1 combiner. To guarantee a 90W amplifier output power, A 45W basic amplifier module is designed using LDMOS FET PTFA260451E transistor. To achieve maximum power output, the amplifier input value must reach 33dBm, so the signal before the divider is 36dBm, this is achieved by the pre-amplifiers.

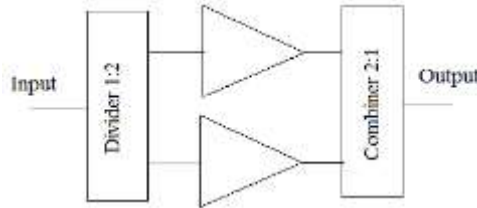


Figure 1. Block diagram of the proposed PA

2. DESIGN AND SIMULATION

2.1. Design of Wilkinson power divider/combiner

A power dividers is a device used to divide input power into multiple output power according to design requirements and power combiner are used to combine multiple input powers into output power. In practice the designer can use many different types of dividers such as directional couplers, T-junction splitters and Wilkinson splitters. The T-junction power divider is the simplest one, it is a three-port network with one input and two outputs. However, disadvantages of this circuit is the poor isolation between output ports. To solve this problem, a wilkinson power splitter (WPD) will be used in this article. In the wilmington power divider the shunt resistor inserted between the output ports will create a high isolation ability. Single section WPD is shown in Figure 2 [4].

The 2-way Wilkinson power divider uses a quarter wavelength ($\lambda/4$) line to coordinate the input Z_0 impedance with the $2*Z_0$ impedance connecting the two outputs. Then the impedance of the segment $\lambda/4$ will be $Z_{\lambda/4} = \sqrt{2} * Z_0$. This divider achieves narrow band. In order to achieve wideband divider/combiner, this paper proposes a multi-section impedance matching method with $\lambda/4$ segments at the 2.65GHz frequency center. Number of sections is choosen 2 and $Z_0=50 \Omega$, and $Z_L=100 \Omega$. Table 1 shows the calculation results of the impedance characteristics of the WPD.

The WPD uses a substrate FR4 1.5mm height with a dielectric substrate of 4.34 and a thickness of 0.035mm, the length and width of the microstrip line is calculated by lincalc tool in Advance Design System software, the schematic diagram of proposed WPD is shown in Figure 3 and simulation results is shown in Figure 4. From the Figure 4, it can be figured out that the transmission coefficient is good at -3.3dB, the forward reflection S11 is less than -25dB and the attenuation coefficient is less than -19.0dB on the 2GHz to 3GHz band.

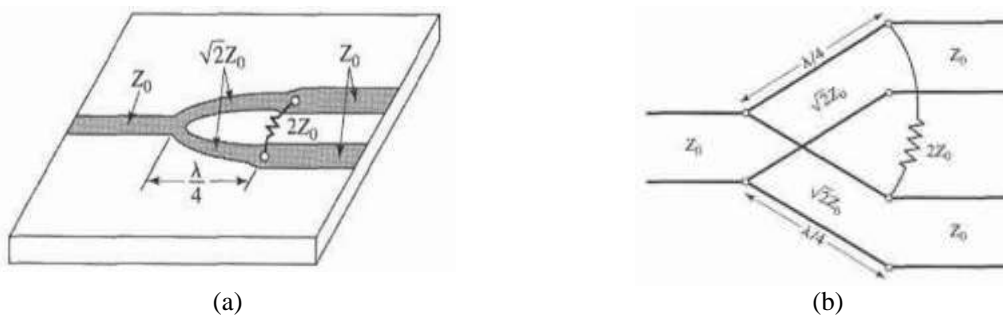


Figure 2. These figures are; (a) wilkinson power devider in micro-trip form, (b) equivalent transmission line circuit

Table 1. Characteristics impedances of WPD

No of section	Z_0	Z_1	Z_2
Two	50 Ω	84.09 Ω	59.46 Ω

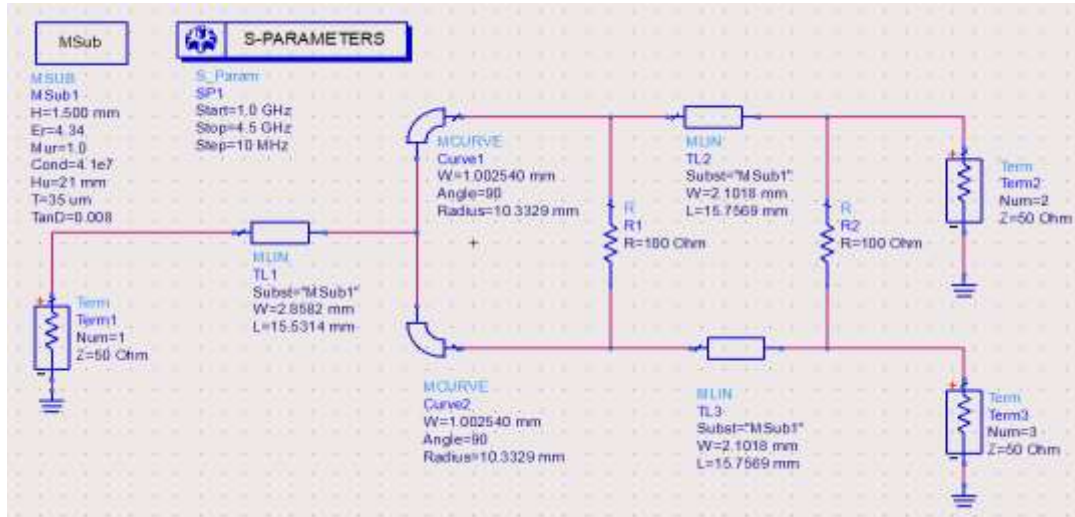


Figure 3. Schematic diagram of multi-section WDP

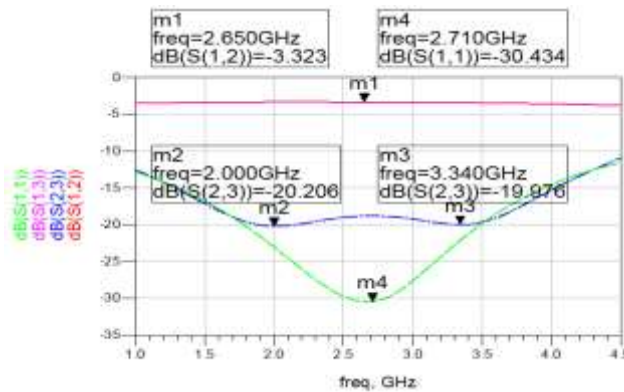


Figure 4. The simulated results of WDP

2.2. Design of power amplifier

To design 45W power amplifier, the article selects appropriate transistor that is PTFA260451E transistor provided by infineon Technologies. It is a thermally-enhanced high power LDMOS FET transistor with 45W output power and operate at 2.65 GHz center frequency. To design a power amplifier is done through the following steps:

Firstly, transistor must be check for stability using the s-parameter of the transistor. The amplifier must be stabilized within the required frequency range. One of the standards used to determine stability of PA is to use parameters K and Δ [4]:

$$K = \frac{1-|S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \tag{1}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2}$$

A PA operates unconditionally stable if $K > 1$ and $|\Delta| < 1$.

Secondly, Based on the scattering parameter of the transistor to design a input and output impedance matching of the transistor with the source and load impedance. There are many methods of designing impedance matching such as using lumped elements; microtrip line such as single-stub or double-stub. However, these methods give narrow impedance matching. In order to achieve high power with wideband impedance matching and stability, this design proposes using the multi-section transformers. The PA is designed at 2.65 GHz center frequency. The PA consists of input impedance matching, output matching, and DC biasing is shown in Figure 5. DC power is supplied across quarter-wavelength transmission line so as not to interfere with the AC signals.

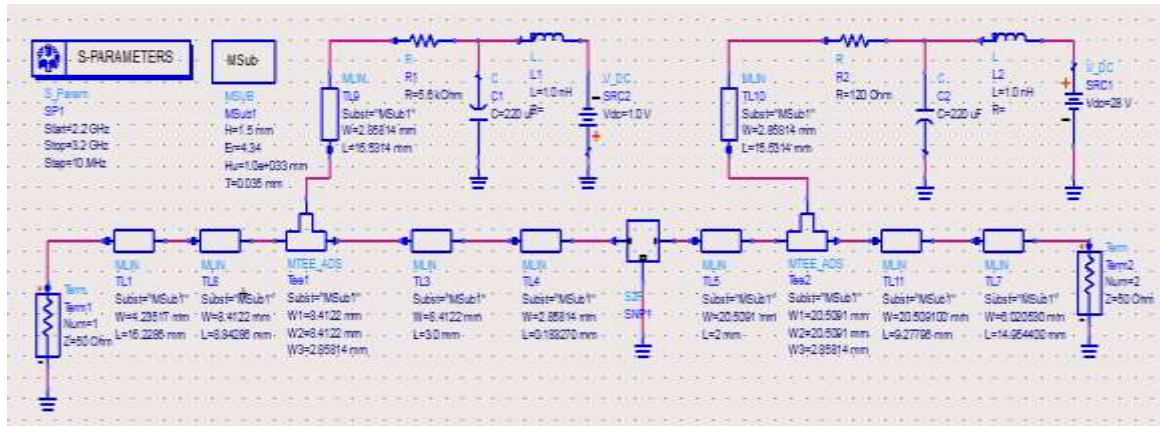


Figure 5. Schematic diagram of PA

The PA also uses the substrate FR4 with a height of 1.5mm, dielectric substrate of 4.34 and a thickness of 0.035mm. To simulate amplifier circuit in small signal mode, the circuit uses scattering parameters with simulated frequency range from 2.2 to 3.2 GHz. Figure 6 shows the results of simulation parameters scattering of the proposed PA circuit. From the simulation results in Figure 6, it shows that the power gain of the amplifier circuit is greater than 10dB with the isolation coefficient (S12) and the return loss is less than -10dB on bandwidth

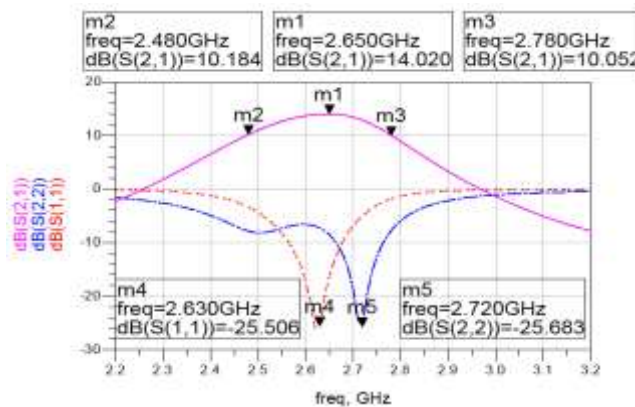


Figure 6. Simulated results of S parameters

For power amplifier circuits, in addition to the characteristic parameters such as output power level (P_{out}), gain (G), there are also extremely important parameters that are drain efficiency (DE) and power added efficiency (PAE). The drain efficiency is determined by the ratio of the output power (P_{out}) to the dissipated power (P_{DC}) [4]:

$$E = \frac{P_{out}}{P_{DC}} \tag{3}$$

The power added efficiency is defined by the ratio of the difference between the output and the input power to the dissipated power [4]:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{4}$$

Perform circuit simulation with supplies power $V_{ds}=28V$ and $V_{gs}=-3.5V$. The power amplifier operates at 2.65 GHz with input power levels from 20 to 45 dbm. The Simulation results of power added efficiency are shown in Figure 7.

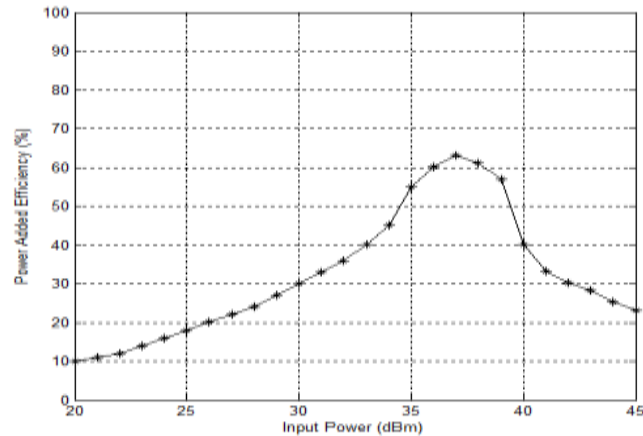


Figure 7. Simulated results of PAE

3. EXPERIMENTAL RESULTS AND DISCUSSIONS

Based on the designed WPD circuit, the layout of the circuit is designed and fabricated using the LPKF C40. The WPD's printed circuit board (PCB) is shown in

Figure 8. The WPD's PCB circuit is measured using Vector Network Analyzer Anritsu. The forward transmission of WPD is shown in **Error! Reference source not found.** It shows the forward gain of -3.326 dB in comparison with a simulation's forward gain of -3.323 dB in Figure 6.

The PA circuit is designed and fabricated experimentally with supplies V_{ds} and V_{gs} through the DC and RF filters. The printed circuit board of PA is shown Figure 10. The drain current has measured about 1000 mA. The measured results of S parameter using Vector Network Analyzer is shown in the following figures. The measurement result in the

Figure 10 determines a peak gain of 13.519 dB at 2.645 GHz, working in a wide frequency range from 2.45 GHz to 3GHz and having a gain greater than 11.5 dB. From Figure 11, it shows that the gain is the same between simulation and the measured results.

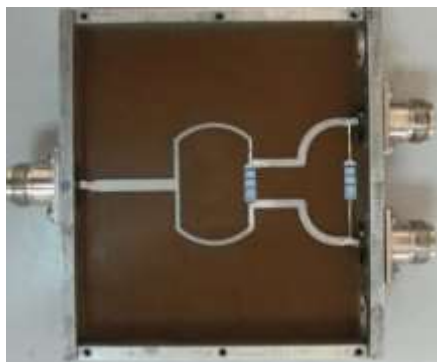


Figure 8. WPD's printed circuit board

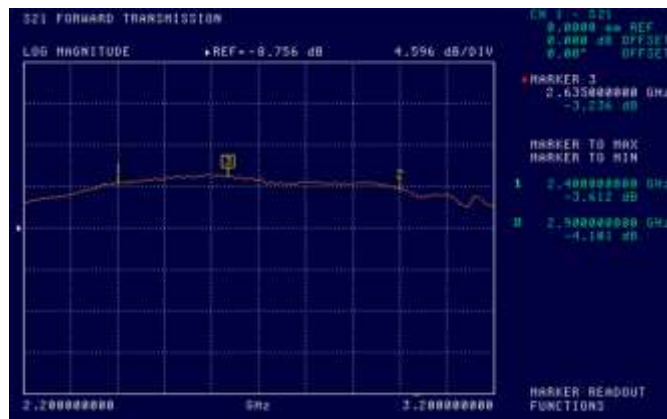


Figure 9. The forward transmission of WPD

From Figure 12, it can be seen the value of the forward reflection (S_{11}) achieves -26.657 dB at 2.6395GHz and is less than -10 dB in band from 2.5GHz to 2.8GHz. Looking at the simulation result in Figure 6 and measurement results in Figure 12, it shows a relatively good similarity.

The measurement result of S_{22} in Figure 13 shows that it reaches -24.457 dB at 2.755 GHz and is less than -15 dB in the working frequency band. The measured output return loss compared to the simulated value is quite similar.

The large signals of PA circuit were measured using Spectrum analyzer ESP13 Rohde&Schwarz and Signal Generator 8648C Agilent. Figure 13 illustrates the measurement's output power of 49.3 dBm at input power of 37 dBm.

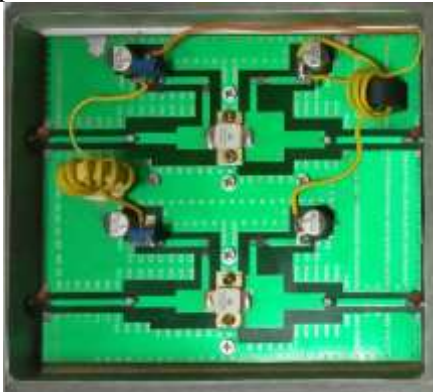


Figure 9. Power amplifier's printed circuit board



Figure 10. The forward transmission of PA

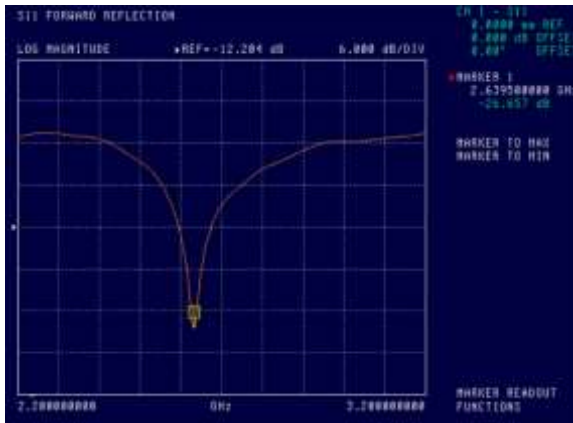


Figure 11. The measurement result of input return loss S_{11}



Figure 12. The measurement result of output return loss S_{22}

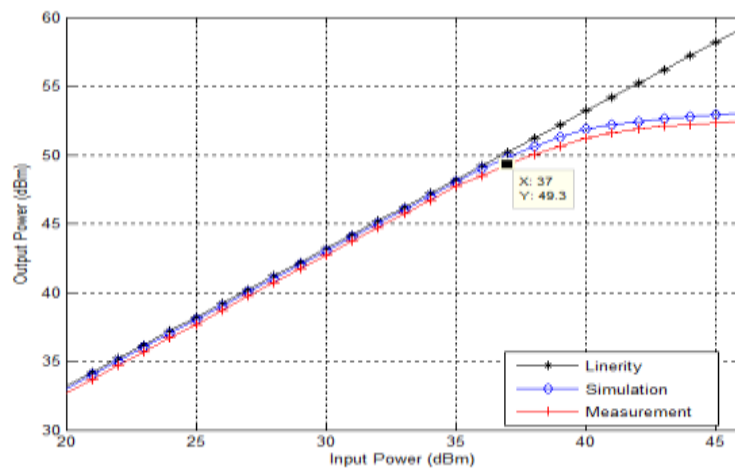


Figure 13. Output power of PA

Table 2 shows the results of comparing the the power amplifier simulation and measurement performance in the frequency band (2.45 GHz – 3.0 GHz). The results show a measured gain of 11.5 dB and a power added efficiency of 61.1% for an input power of 37 dBm at 2.65 GHz. Table 3 shows the results of comparing the parameters of the proposed design with the previously published works. From the table it can be seen that the proposed design has the highest output power and bandwidth.

Table 2. Measured and simulated results with input power of 37 dBm

	Simulation	Measurement
Pout (dBm)	49.5	49.3
Gain (dB)	14.02	11.5
PAE (%)	63.2	62.1

Table 3. Comparison with state of the art

Reference	Frequency (GHz)	Pout (dBm)	Gain (dB)	PAE (%)
6	2.45	50.4	9.2	62
7	2.5-3.8	48.8-49.8	9.3-12.7	54-67
8	1.3-3.4	42.2-43.9	7.2-11.2	45–62.3
This work	2.4-3.0	48.5-49.3	11.5-13.5	54-62.1

4. CONCLUSION

In conclusion, the power amplifier for wireless communications at center frequency of 2.65GHz has been successfully designed and fabricated. The two 45W power amplifiers was designed using LDMOS FET. In addition, combining two power amplifier modules using Wilkinson produces up to 90W of output power. This technology can be applied to combine higher power if it use n-way WPD. The measurement results have been achieved the output power of 49.3 dBm; PAE of 62.1%; the forward gain of 13.5 dB is more than 11.5 dB inband and the input/output return loss is less than -10 dB. The designed amplifier can be used for 4G, 5G mobile communications and S-band satellite communication.

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