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Hardware implementation and performance evaluation of microcontroller-based 7-level inverter using POD-SPWM technique

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ABSTRACT

Renewable energy sources are considered as inexhaustible sources for the very long-term, as they come from natural processes that are constantly replenished. However, there are a number of challenges facing renewable energy technology adoption, like the grid connecting problems. One of the main challenges relates to the grid connecting problem is the power quality issues for power converter, such as harmonics, voltage stability, and frequency fluctuation. Hence, the inverter remains the first element to be built because of its undeniable advantages in alternative continuous conversion. However, it has some disadvantages such as high component count and complex control method. This paper presents the design and implementation of a new 7-level inverter architecture with only six switches. This architecture requires fewer components compared to other 7-level inverter topologies therefore, the overall cost, control technique complexity, and conduction losses are highly reduced. A digital phase opposition disposition sinusoidal pulse width modulation (POD-SPWM) strategy using the Arduino is adopted to improve the performance of the proposed multi-level inverter (MLI) which leads to further reduction in total harmonic sistortion (THD). In this paper, the proposed inverter is tested using Proteus software and Matlab Simulink. Finally, a laboratory setup of the proposed inverter was built to validate its workability by the experimental results.

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1. INTRODUCTION

The use of photovoltaic energy has increased exponentially in the world. This development is boosted by international and national policies which aim to reduce the use of fossil fuels according to the objectives of the Kyoto Protocol [1], [2]. For example, in Morocco, the government has implemented several measures to develop the photovoltaic industry. These aids are intended to make the photovoltaic (PV) industry economically viable and competitive with fossil fuels. The recent development of the photovoltaic (PV) system has motivated researchers to improve the electrical energy conversion systems [3], [4], hence multi-level inverter technology has become a very important alternative in the field of energy control in high power of medium voltage. A multi-level inverter is a static converter ensuring the conversion of electrical energy from the continuous direct current (DC) output of PV module to the alternative alternating current (AC) voltage [5].

The concept of using inverters with multiple voltage levels was presented by MIT researcher some 30 years ago [6]-[8]. Nowadays, in the areas of medium and high voltage [9], multi-level converters, with natural or hybrid topologies, present options which have been widely proved. Multi-level inverters offer more advantages, such as good quality of the output voltage with reduced harmonic distortion compared to a conventional inverter. However, this technique requires the use of a greater number of power semiconductors, this can make the general system more expensive and complex [10].

Three converter topologies have been proposed for multilevel inverters during the last two decades [11] ,cascaded H-bridge converters (CHB) with separate continuous sources, neutral point clamped (NPC) and flying capacitor converters (FC). These three topologies use various mechanisms to generate the required output. In the first topology the inverters are built around a series connection of several single-phase H-bridge inverters with galvanic isolated DC voltage sources[12], [13], although, in flying capacitor topology, floating capacitors are used [14].

P. Maheshkar and P. P. Gajbhiye [15], proposed a 7-level MLI using 9 switches, minimizing 3 switches from the conventional structure of cascaded MLI [7]. It gives good results by generating desired 7-level output waveform with low THD. Moreover, a 7 level MLI using 7 switches lessening 2 more switches was presented in [16], from the precedent topology. In order to minimize the number of switches, the number of DC sources and minimizing complexity of the multi-level inverter, the new topology is proposed using only 6 switches and 3 DC sources for 7 levels. The main purpose of this paper is to develop, simulate and real-time implement a new 7-level converter structure with six switches, this inverter is controlled by a digital POD-SPWM command in order to decreases the total harmonic distortion rate. In section 2, the design of the proposed inverter is presented. Section 3 presents POD-SPWM technique. Section 4 presents the simulation of inverter in ISIS Proteus and Matlab Simulink. Section 5 presents a hardware results and finally conclusion is summarized in section 6.

2. PROPOSED TOPOLOGY OF 7-LEVEL INVERTER

2.1. Presentation of proposed architecture

The purpose of this architecture is to reduce the number of switching devices. Thus, reducing the cost of circuit building, reduce the complexity of control technique and reduce the total harmonic distortion. As shown in Figure 1 the proposed 7-level inverter contains three DC voltage sources of 10 V, six MOSFET switches (S1, S2, S3, S4, S5 and S6) and diode D1, to ensure the seven level output voltage of our system.

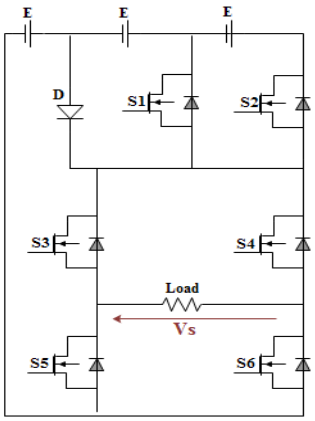


Figure 1. The proposed 7-level inverter circuit

The proposed architecture can be expanded to increase the number of levels at the output. This could be achieved by adding more DC sources and more switches to the system. The number of switching devices and DC sources used in the system are determined by (1) and (2) respectively.

$$\text{DC voltage number,} \quad N_{DC} = \frac{m+1}{2} \tag{1}$$

$$\text{switches number,} \quad N_{switch} = \frac{m+5}{2} \tag{2}$$

where m is the number of levels, with $m \geq 5$.

Although, with increased number of switches, circuit size and cost, power loss and complexity increases. However, in the proposed architecture at any level a maximum of three switches conduct to achieve the desired output voltage level, which results in a lower amount of conduction losses, which is an added advantage to the proposed architecture.

2.2. Operation mode

The operation mode of the proposed 7-level inverter is illustrating in Figure 2. The red arrows in the figure indicate the current path. As shown in the figure, the operation mode can be divided into seven modes, four modes for generating the positive levels including the 0 level and three modes to generate the negative levels. Table 1 summarizes the switches different states to produce the desired 7-level output waveform presented in Figure 3.

The positive levels are generated as follows:

- **MODE 1:** During this mode of operation, switches S3 and S6 will be turned ON and the other switches will be OFF. Thus, the diode D1 will conduct current in and the voltage across the load Vs will be equal to E, as shown in Figure 2 (a).
- **MODE 2:** During this mode, switches S1, S3 and S6 will be turned ON and the other switches will be OFF. The diode D1 will be OFF and the voltage across the load Vs will be equal to 2E, as shown in Figure 2 (b).
- **MODE 3:** During this mode, switches S2, S3 and S6 will be turned ON and the other switches will be OFF. The diode D1 will be OFF and the voltage Vs will be equal to 3E, as shown in Figure 2 (c).
- **MODE 4:** During this mode, either all the switches and the diode D1 will be turned ON or all of them will be OFF. Thus the voltage across the load will be equal to 0v, as shown in Figure 2 (d).

The negative levels are generated as follows:

- **MODE 5:** During this mode, switches S4 and S5 will be turned ON and the other switches will be OFF. Thus, the diode D1 will conduct current in and the voltage across the load Vs will be equal to the negative voltage –E, as shown in Figure 2 (e).
- **MODE 6:** During this mode, switches S1, S4 and S5 will be turned ON and the diode D1 will be OFF. The negative voltage –2E will be obtained across the load, as shown in Figure 2 (f).
- **MODE 7:** During this mode, switches S2, S4 and S5 will be turned ON and the other switches will be OFF. The diode D1 will be OFF and the voltage Vs will be equal to a negative voltage -3E, as shown in Figure 2 (g).

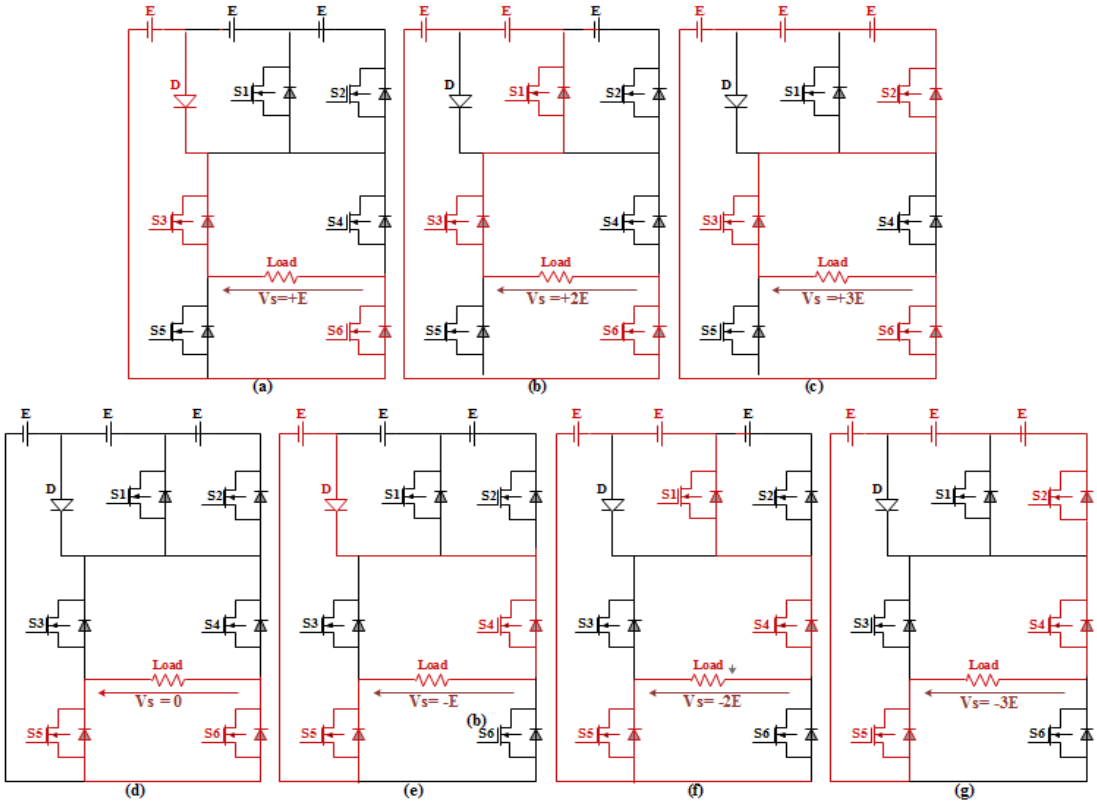


Figure 2. Operation modes for the proposed 7-level inverter architecture

Table 1. Switching states for proposed 7-level inverter

D1	S1	S2	S3	S4	S5	S6	Levels
ON	0	0	1	0	0	1	E
OFF	1	0	1	0	0	1	+2E
OFF	0	1	1	0	0	1	+3E
X	X	X	X	X	1	1	0
ON	0	0	0	1	1	0	-E
OFF	1	0	0	1	1	0	-2E
OFF	0	1	0	1	1	0	-3E

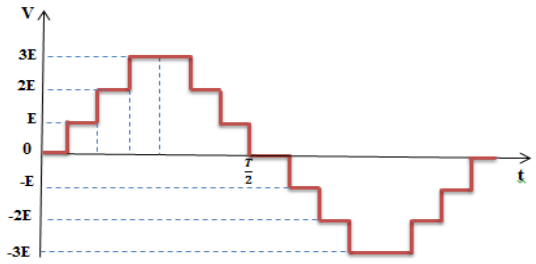


Figure 3. Typical output voltage waveform of a 7-level inverter

3. SWITCHING CONTROL STRATEGY

3.1. Phase opposition disposition sinusoidal pulse width modulation

The SPWM technique is widely used in power converters because of its simplicity and strong control technique [17]-[19], it is used to control the output voltage shape of the inverter by changing the duty cycles of the pulses [20]. SPWM is produced by comparing a reference sinusoidal signal of required frequency and a carrier triangular signal of high frequency (in serval KHz) [21], [22]. Conventionally, SPWM uses N-1 carrier signals to produce the output voltage of the N-level inverter [23]. In our case to generate the switching pulses of the proposed 7-level inverter, we used (POD-SPWM) technique in which we compared six carrier signals with equal frequency and amplitudes to a reference sine waveform of 50 Hz frequency. In this POD-SPWM technique, both the three carrier signals above the X- axes and those below the X- axes are in same phase, but are shifted from each other in phase 180 degrees as shown in Figure 4.

In order to produce the SPWM control signals, we have opted for digital technologies to avoid the inconvenience of analog circuits [24]. Digital technologies are more flexible and cheaper, hence the hardware cost of the system is significantly reduced. In our case, we used a microcontroller to produce the six SPWM control signals by varying the duty cycles of SPWM according to a sine lookup table whose frequency (fr=50Hz) is the intended frequency of the sinusoidal signal obtained at the output of the inverter.

Generally, SPWM is generated for one half cycle and it can be used for both positive and negative cycle. In this work the time period desired for half cycle is 10 ms and the second half cycle remain zero. For the switching frequency we used a SPWM frequency of fc=16KHz.

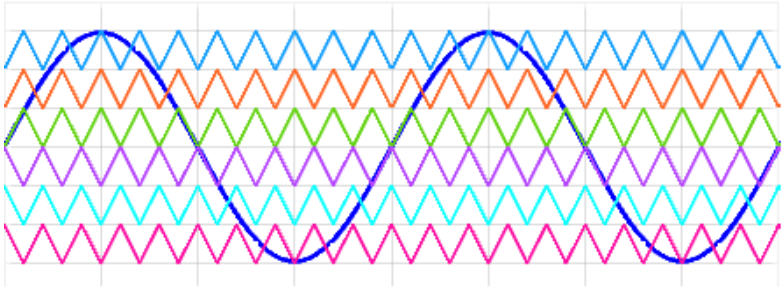


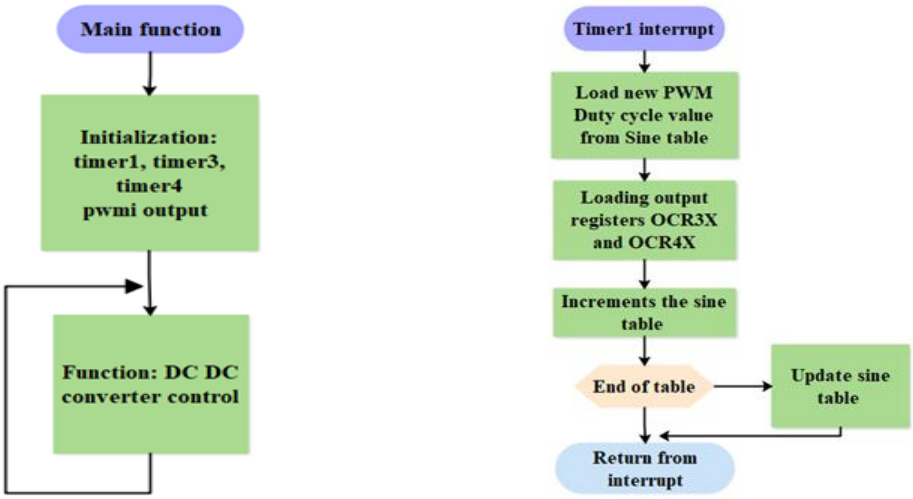
Figure 4. Modulation and carrier signals of POD-SPWM technique for 7-level inverter

3.2. POD-SPWM flow chart

To generate the six SPWM control signals we used Arduino ATmega which has 15 Pulse-width modulation (PWM) outputs and 6 timers. These timers are used to modify the switching frequency via its registers. Timers 3 and 4 were configured in a way that the frequency of PWMs outputs is set at 16 KHz and that timer 2 generates interruption every 62.5µs

The program flowchart that has been implemented in microcontroller is presented in Figure 5. Figure 5(a) presents the main function in which the SPWMs outputs and the timer are initialized alongside other functions. Figure 5(b) shows the interrupt function that is generated every 62.5µs by timer 1 in which the sine look up table is declared and each time the interrupt occurs a new value of duty cycle is picked up from the sine look up table. For the positive half cycle (0ms to10ms) the 3 registers OCR3A, OCR3B and OCR3C will be loaded with the duty cycle values to generate SPWM1, SPWM2 and SPWM3 respectively. For the other half cycle (10ms to 20ms) the registers OCR4A, OCR4B and OCR4C will be loaded to

generate SPWM4, SPWM5 and SPWM6 respectively. To achieve the required switching pulses for the six switches, a logical operator was used to convert the SPWM control signals to a proper pulse of each switch. Binary representation of switching operation is presented in Table 2 and Logical equations obtained from the truth table are presented in the table.



(a) (b)

Figure 5. SPWM flow chart

Table 2. Truth table of switching operation

SPWM1	SPWM2	SPWM3	SPWM4	SPWM5	SPWM6	S1	S2	S3	S4	S5	S6	Levels
1	0	0	X	X	X	0	0	1	0	0	1	E
1	1	0	X	X	X	1	0	1	0	0	1	+2E
1	1	1	X	X	X	0	1	1	0	0	1	+3E
X	X	X	X	X	X	X	X	X	X	X	X	0
X	X	X	1	0	0	0	0	0	1	1	0	-E
X	X	X	1	1	0	1	0	0	1	1	0	-2E
X	X	X	1	1	1	0	1	0	1	1	0	-3E

$$S_1 = PWM_1.PWM_2 + PWM_4.PWM_5 = PWM_2 + PWM_5 \quad (3)$$

$$S_2 = PWM_1.PWM_2.PWM_3 + PWM_4.PWM_5.PWM_6 = PWM_3 + PWM_6 \quad (4)$$

$$S_3 = S_6 = PWM_1 \quad (5)$$

$$S_4 = S_5 = PWM_4 \quad (6)$$

4. RESULTS AND DISCUSSION

4.1. Global system analysis

In this section, simulation studies of the proposed 7-level topology with and without filter are presented to confirm the workability of the proposed inverter and demonstrate the theoretical analysis, the simulation is carried out in ISIS Proteus and Matlab/Simulink simulator for harmonic analysis. The simulation of 7-level inverter is developed by implementing the circuit diagram shown in Figure 6 using ISIS PROTEUS. The system consists of Arduino microcontroller ATmega2560 used to produce six SPWM control signals, then the gating signals for the six MOSFET switches of the inverter are generated using logic combination of the SPWM signals. The isolation circuit is provided by high speed optocouplers 6N137 to completely isolate the low power part (microcontroller) and the high power part that consists of six MOSFET IRF 840 switches. Those switches are used to convert the applied DC voltage to AC voltage. Moreover, to ensure that the MOSFETs will trigger, we used MOSFET driver IR 2110 designed for bootstrap operation, afterwards, a second order LC filter was used to reduce harmonic content and obtain pure sine wave output at the desired frequency of 50Hz.

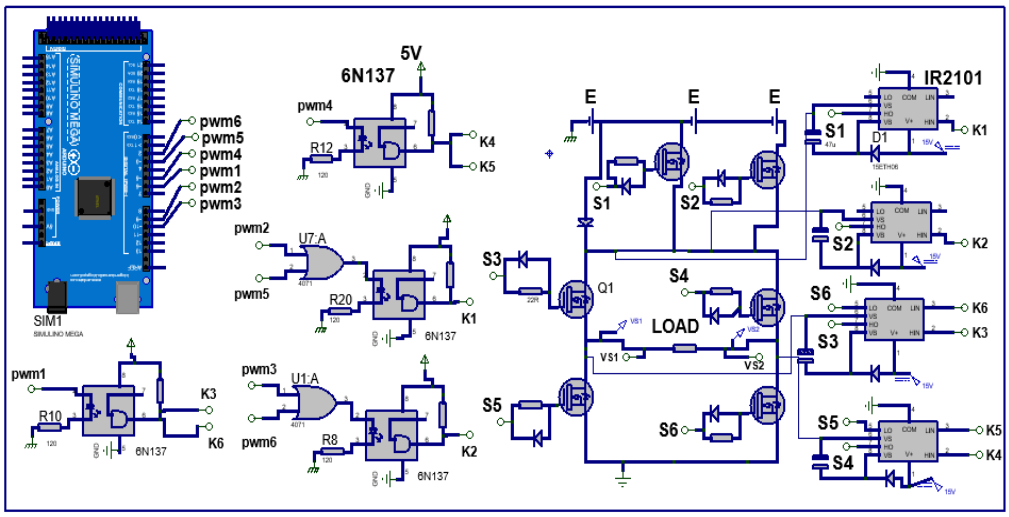
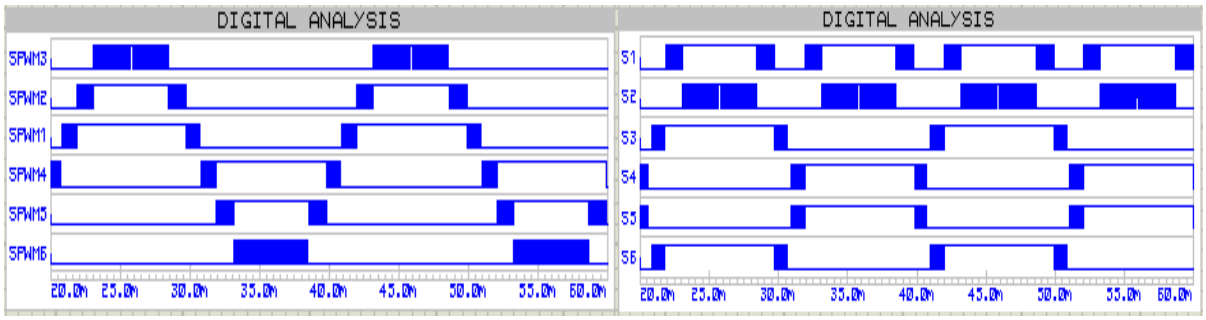


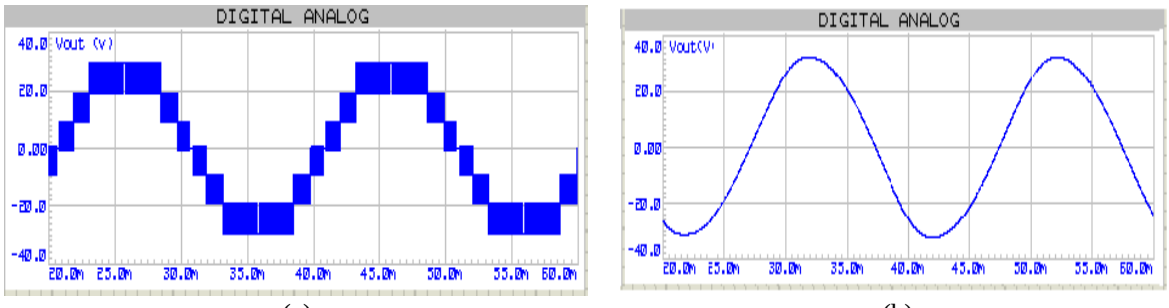
Figure 6. Over-all circuit diagram of the proposed 7-inverter

Six SPWM control signals of 16KHz frequency are generated at the Arduino output as shown in Figure 7 (a). Then, an extra logic circuit is used to generate the six gating pulses of the six switches as shown in Figure 7 (b). The generated output voltage without filter is a 7-level staircase output voltage which nearly identifies itself with sine wave as shown in Figure 8 (a). Figure 8 (b) shows the filtered output voltage which is pure sinusoidal waveform with 50Hz frequency and a peak voltage of 30V.



(a) (b)

Figure 7. These figures are; (a) SPWM control signals and (b) Gating pulses for the six switches



(a) (b)

Figure 8. Inverter output voltage; (a) without filter and (b) with filter

Harmonic content or total harmonic distortion in the output voltage waveform is often used to characterize the signal quality of electric power system, it can also be used to evaluate the effectiveness of control strategies [25]. The THD value can be calculated using the following,

$$THD(\%) = 100\frac{\sqrt{V_2^2+V_3^2+V_4^2+\cdots+V_n^2}}{V_1} \quad (7)$$

where,
V_1 is r.m.s. voltage at the fundamental frequency
V_n is r.m.s voltage of umpteenth harmonic

For harmonic analyses, the percentage of total harmonic distortion (THD) is determined using Matlab Simulink as shown in Figure 9. The THD was first calculated with a purely resistive load of 50Ω then with resistive-inductive load (R=5OΩ, L=10mH). The simulation is done using two switching frequency (fc=10KHz and fc=16KHz) to analyzes the influence of switching frequency on the inverter performance in terms of THD. The simulation results for R load with and without filter is presented in Figure 10(a) and 10(b), the output voltage and current of the inverter for R-L load without filter is presented in Figure 11(a) and (b), with filter is presented in Figure 12. The Figures 13-15 show the corresponding voltage THD. As shown from the figures the THD value is significantly low for both loads, which complies with the IEEE standard of THD limits.

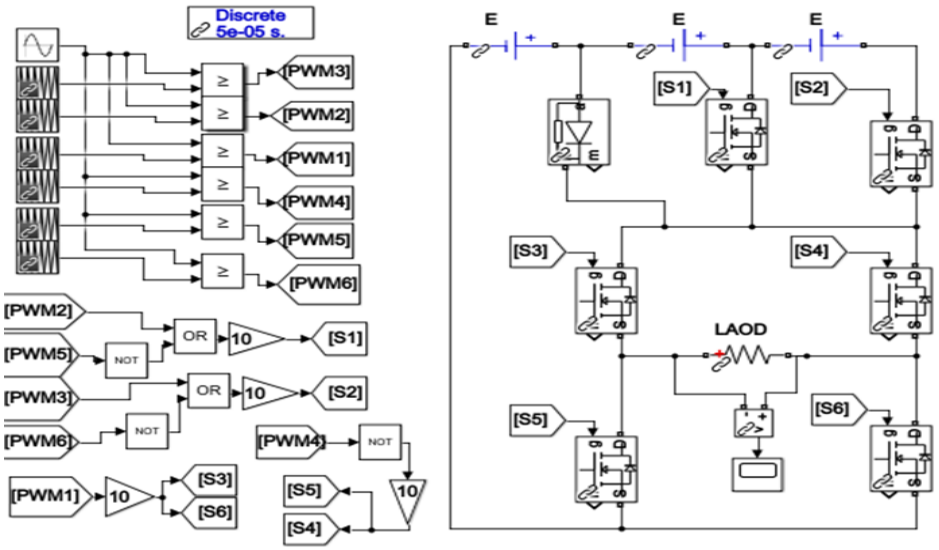


Figure 9. Matlab simulation model of the 7-level inverter

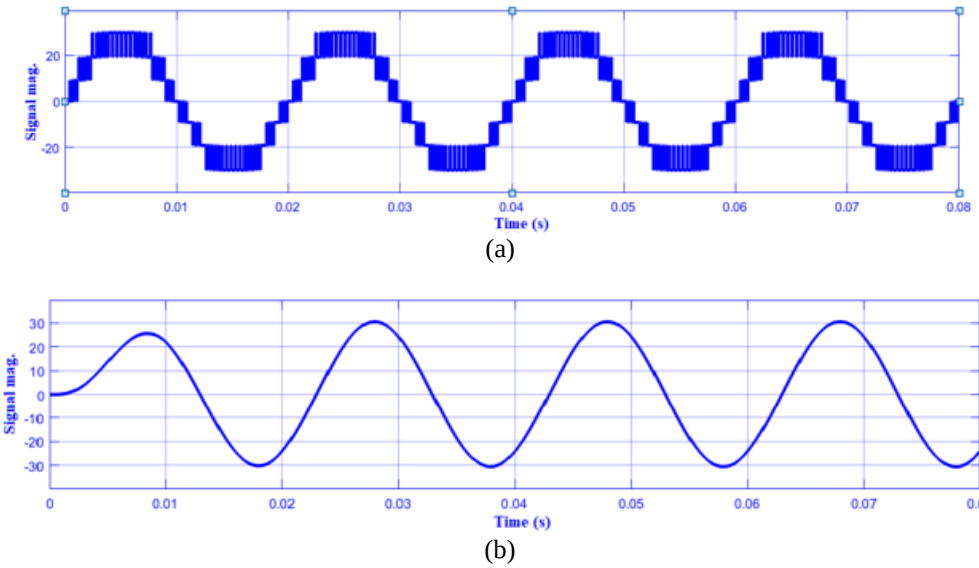


Figure 10. The 7-level inverter output voltage for resestive load; (a) before filtering and (b) after filtering

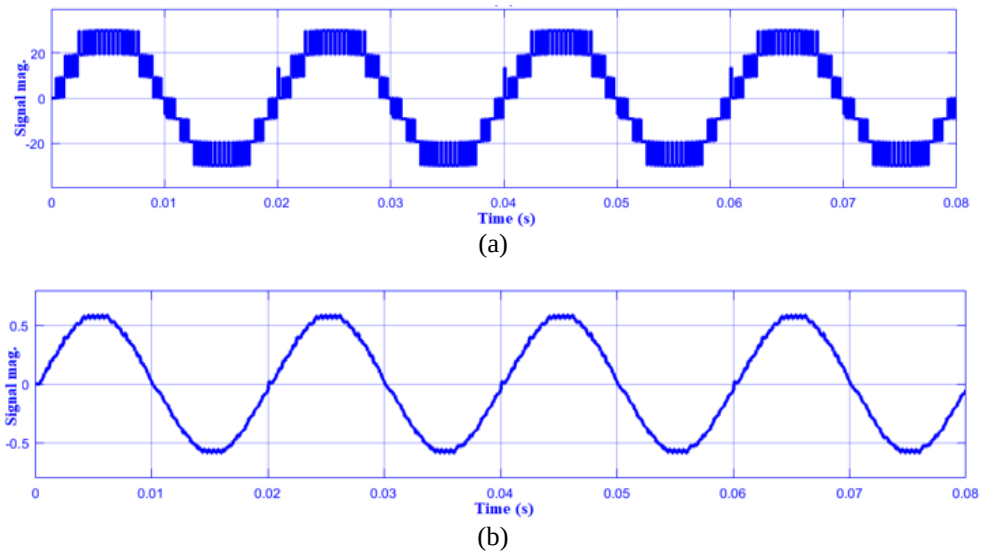


Figure 11. These figures are; (a). The inverter output voltage for R-L load before filtering and (b) the output current before filtering

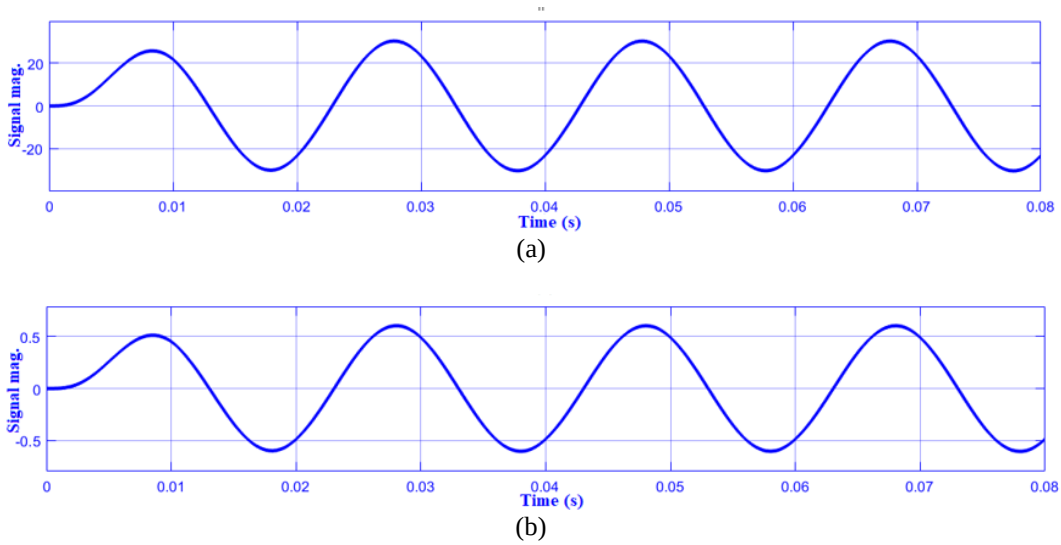


Figure 12. (a) The inverter output voltage for R-L load after filtering, (b) the output current after filtering

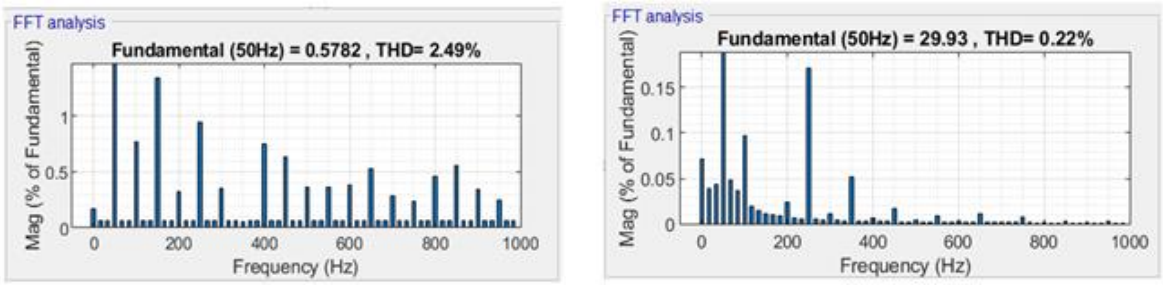
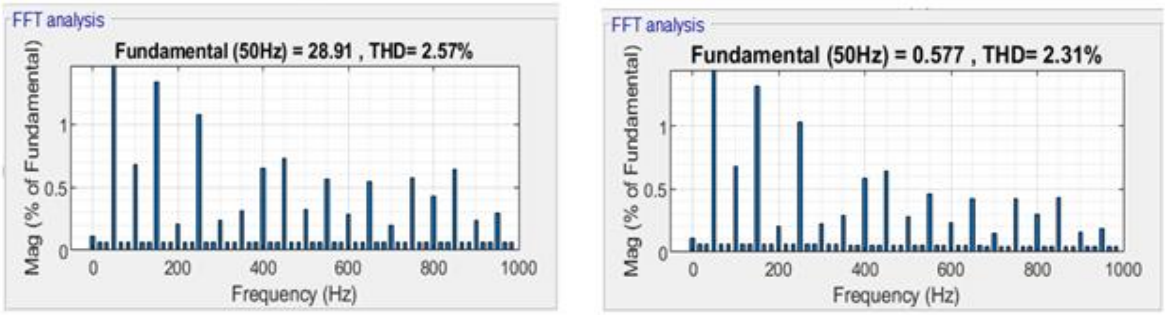
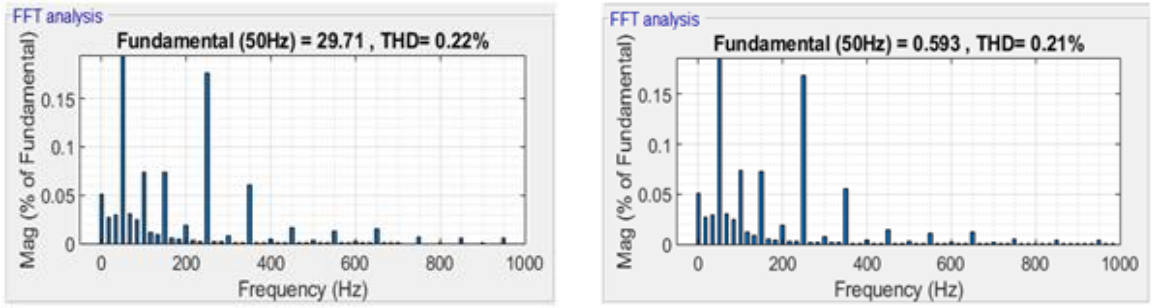


Figure 13. FFT analysis of the inverter output voltage for R load; (a) before filtering and (b) after filtering



(a) (b)

Figure 14. FFT analysis of the inverter for R-L load before filtering; (a) output voltage and (b) output current



(a) (b)

Figure 15. FFT analisis of the inverter for R-L load after filtering; (a) output voltage and (b) output current
FFT analisist after filtering

The THD value for both loads with and without filter using the two switching frequencies is presented in Table 3. The table clearly shows that the minimum value of the proposed inverter THD is obtained for resistive load at 16KHz switching frequency. Which means that by increasing the swwitching frequency, the harmonic in the output signal can be reduced, and it is observed that the THD value is reduced by more than 50 percent using filter.

Table 3. %THD comparison of the proposed 7-level inverter topology

	THD%			
	Without filter		With filter	
F(KHz)	10KHz	16KHz	10KHz	16KHz
R	3.70	2.49	0.50	0.22
R-L voltage	4	2.57	0.52	0.22
R-L curent	3.51	2.31	0.51	0.21

To prove the merits of the proposed inverter, a comparison of the proposed topology with the other existing topologies mentioned in the literature, based on the number of switches, total harmonic distortion (THD) and number of DC sources is presented in Table 4. As shown in the table, the new 7-level inverter architecture provides a pure sinusoidal voltage with very low THD using fewer components compared to conventional and others topologies.

Table 4. Comparison betwen the proposed 7-level inverter and other inverters

Topologies	Number of switches	Number of DC sources	THD%
Conventional cascaded 7-level inverter [7]	12	3	21.84
7-level MLI proposed in [15]	7	2	5
7-level MLI proposed in [16]	8	3	13.66
The new proposed 7-level inverter	6	3	2.49

4.2. Validation expiremental

To validate the workability of the proposed topology, an experimental prototype was implemented to confirm the simulation results as shown in Figure 16. The principal required components used to implement the proposed 7-level inverter are presented in Table 5. For the POD-SPWM generation, ARDUINO ATmega2560 was used to produce the SPWM control signals with a switching frequency of 16KHz as shown in Figure 17. As shown in Figure 18(a) and 18(b), the seven levels output voltage is successfully produced and the filtered output voltage is a pure sine wave with maximum voltage magnitude of 30V and 50Hz frequency. Figure 19 shows the harmonic spectrum for the output voltage of the inverter derived from the experimental prototype.As shown in the figure, the harmonic amplitudes are all below 1% of the fundamental amlitude, except the 3rd harmonic with an amplitude of 1%. The experimental results much with the simulation results, which confirm that the system is working as intended.

Table 5. Required components used to implement the proposed 7-level inverter

Compenent name	Spicification
Microcontroller	ARDUINO ATmega 2560
MOSFET swiches	MOSFET IRF 840: Power MOSFET (VDSS = 500V, RDS(on) = 0.85 ohm, ID =8.0A)
MOSFET driver	R 2110: high voltage, high speed driver
Optocoupler	6N137: High Speed Optocoupler, 10 Mbd
Diode	MUR 1560: Fast recovery diode, 15A, 600V, TO-220A
DC Source	Tree DC sources of 10V
Load	R=50Ω
LC Filter	L= 80 mH , C=47µF

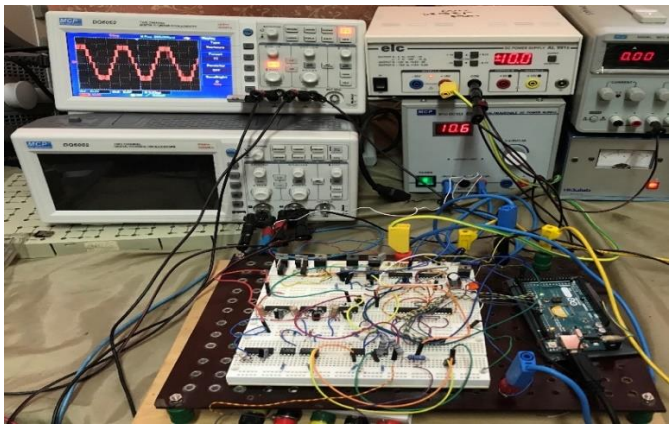


Figure 16. Laboratory setup of the proposed 7-level inverter

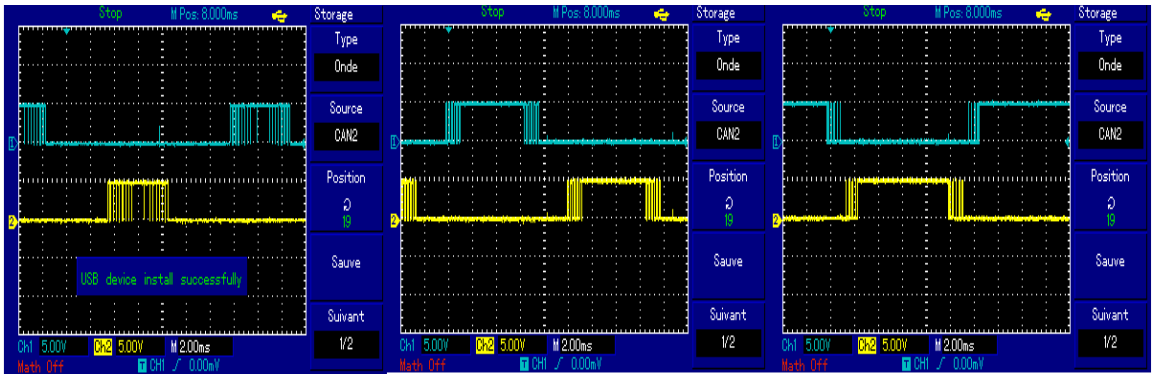
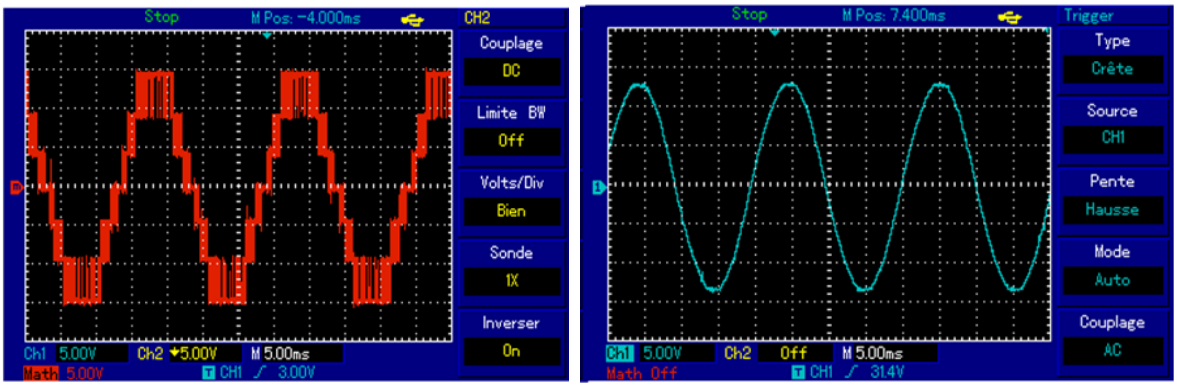


Figure 17. SPWM control signals



(a) (b)

Figure 18. Hardware output voltage of proposed 7-level inverter; (a) before filtering and (b) after filtering

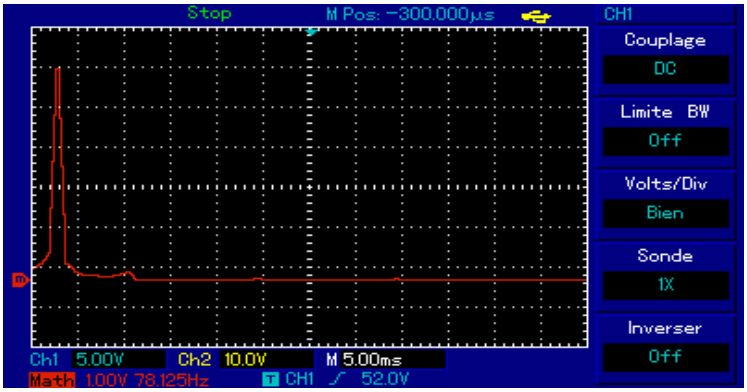


Figure 19. Spectrum analysis of the proposed inverter

5. CONCLUSION

This paper describes the design and real-time implementation of a new digital POD-SPWM based 7-level inverter architecture. The advantages of the proposed topology are emphasized with the reduction of power components. Therefore, the manufacturing cost, the size as well as the complexity of control strategy are greatly reduced. Digital POD-SPWM technique using ARDUINO microcontroller ATmega2560 has been used to enhance the performance of the inverter by reducing the total harmonic distortion and generating a high quality output voltage. The designed 7-level inverter is analyzed and simulated using Matlab Simulink and ISIS Proteus. The simulation is done using two switching frequency to analyzes the influence of the switching frequency on the inverter performance in terms of THD. In conclusion, by increasing the switching frequency, the harmonic in the output signal can be reduced. The inverter efficiently is experimentally confirmed by the simulation and the laboratory experimental results. The results show that the designed inverter total harmonics distortion (THD) is reduced as compared to the existing structures and a pure sine wave with a frequency of 50Hz and THD of 0.22% is obtained at the filter output, which complies with the IEEE standard.

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