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0.18μm CMOS Low Voltage Power Amplifier for WSN Application

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Abstract

This paper presents the design of a Class A/B power amplifier (PA) for 2.4-2.4835GHz Wireless Sensor Network (WSN) system in 0.18μm CMOS technology. The PA adopts the single-stage differential structure and the output power of the PA can be controlled by switching the sizes of transistors. Seven different level of output power can be obtained through a three-bit control code. The tested results shows that the proposed PA achieves power added efficiency (PAE) of 26.73% while delivering an output power of 6.35dBm at 1dB compression point. Its power gain is 15.87dB. With a low DC voltage supply of 1V, its power consumption is 15.3mW. The PA die size is 1070×610μm^2.

Keywords: *class AB, PA, WSN, PAE, low voltage*

1. Introduction

Wireless sensor network [1] (WSN) is a self-organizing network which consists of a large number of sensors using wireless communication technologies. Its purpose is to cooperatively perceive, collect and process information of target in the network area, and then the information is delivered to observer. It can be applied to various area of environmental and ecological control, medical, home automation, traffic control, etc. It is considered to be a huge impact in the 21st century technology. With the rapid development of wireless communications and micro-electronics technology, highly integrated, low power and low-cost the CMOS [2] wireless RF transceiver chip has been more and more applied in people's daily life and industrial production of electronic devices, the market potential is huge [3, 4].

As the core part of the wireless communication system in WSN, the transceiver (Figure 1) has been the focus of the research in recent years. Power amplifier located at the end part of transmitter is one of the key modules of the transmitter. It amplifies radio frequency (RF) signal from mixer, and delivers the signal to antenna for transmitting. Its function is to improve the ability of anti-interference of the RF signal. Therefore, the performance of PA is closely related with the communication quality of a communication system.

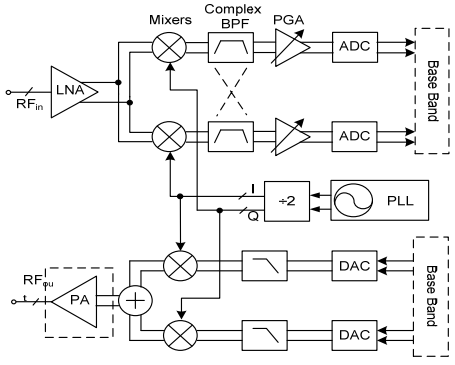

Figure 1. Block Diagram of the Transceiver

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This paper presents the design of a power amplifier (PA) for Wireless Sensor Network (WSN) system in TSMC 0.18μm RF CMOS technology. Because of the requirement of low power consumption for WSN system, this power amplifier doesn't need high power gain and output power. However, high efficiency [5] is the key target and power control is needed. After the tradeoff between efficiency, output power gain and, a fully differential single stage Class A/B [6] cascode structure is adopted and power control is realized by controlling the switch of transistors. The proposed PA has higher efficiency under a low DC voltage supply of 1V.

This paper is organized as follows. Section II discusses principles and the design of the proposed PA. Section III shows the microphotograph of the proposed PA and describes the experimental results of the proposed PA. Finally, conclusions are given in Section IV.

2. Power Amplifier Design

The proposed PA is shown in Figure 2. M_2, M_4, M_6, M_8, M_{10} and M_{12} are power transistors. M_1, M_3, M_5, M_7, M_9 and M_{11} are switch transistors. L_{d1} and L_{d2} are radio frequency choke (RFC), and they are load of the power transistors. R_1 and R_2 are stability adjusting resistors. C_{g1}, L_{g1} and C_{g2}, L_{g2} are input matching network. C_{g3}, L_{g3} and C_{g4}, L_{g4} are output matching network. R0 and M0 are composed of a bias circuit of the PA.

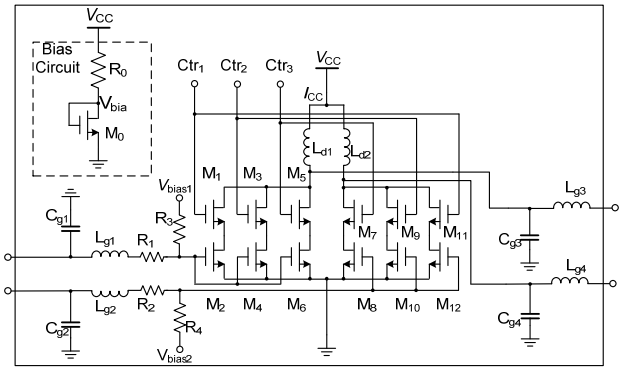

Figure 2. The Proposed Power Amplifier

2.1. Size and Bias of Power Transistor

The size of power transistor directly determines maximum output power of the proposed PA. The transistor can withstand a maximum voltage of breakdown voltage (V_{max}), while its minimum voltage is limited by the knee voltage (V_{knee}). V_{knee} defined as a value of V_{ds} when the drain current of the transistor reach to 95% of its maximum current. And V_{knee} divides work state of the transistor into the linear region and the saturation region. Under normal circumstances, V_{knee} compared to V_{max} is a very small value. It can be ignored in the design, i.e. can be considered $V_{knee} \approx 0$. However, this design is worked under 1V supply voltage and the power transistor need to work in saturation region, V_{knee} must therefore be considered. Through DC sweep curve, $V_{knee} \approx 0.5$V is estimated. The output power of the PA can be expressed as:

$$P_{out} = \frac{(V_{CC} - V_{knee}) I_{CC}}{2} \quad (1)$$

Where V_{cc} is power supply voltage and I_{cc} is drain current of the power transistor. 5dBm (≈ 3.16mW) maximum output power is needed, so:

$$I_{CC} = \frac{2P_{out}}{V_{DD} - V_{knee}} = \frac{2 \times 3.16}{1 - 0.5} = 12.64\text{mA} \quad (2)$$

According to I_{cc} and above requirement, width to length ratio and bias voltage of power transistor can be probably selected. Considering the existence of various non-ideality factors, the actual output power will certainly be less than the expected value, and therefore the size of the transistor and the bias voltage must leave some margin.

2.2. Radio Frequency Choke Inductor

TSMC 0.18μm RF CMOS process provides a variety of on-chip spiral inductors. The on-chip inductor is not a simple inductor, but contains complex parasitic parameters of a circuit. Nine-parameter equivalent circuit of the inductor is shown in Figure 3. Where R_{sub1} and R_{sub2} are substrate parasitic resistance, and C_{sub1} and C_{sub2} are substrate parasitic capacitance, and C_{ox1} and C_{ox2} are the parasitic capacitance between the inductor and the substrate surface, and C_s is the parasitic capacitance between the main coil of the inductance and the lead line. These parasitic parameters make the poor performance of the on-chip spiral inductors. The Q value is low, generally less than 10. Usually the higher the frequency, the Q value is lower, mainly because the top-level metal line of the inductor exists skin effect. The higher the frequency, the greater the parasitic resistance, and thus the Q value is lower.

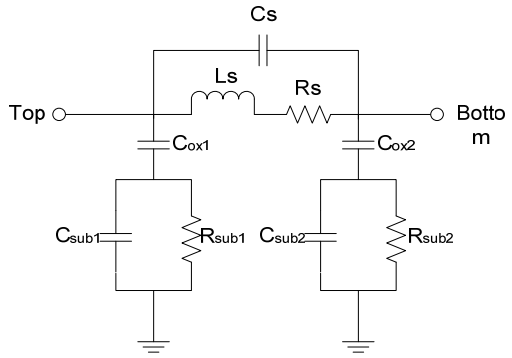

Figure 3. Nine-parameter Equivalent Circuit of the Inductor

Q value, the maximum allowed current, accuracy of the model, output matching, loss, and many other factors are needed to be taken into account, when choosing the choke inductor. The inductor must have a larger Q value near 2.44GHz. Wider metal width of the inductor can increase Q value and the maximum allowed current. Since the drain inductance is part of the output matching circuit, this inductor should be selected to simplify matching network. Adopting the inductor with accuracy model will cause the simulation results more reliable.

2.3. Output Power Control

Wireless sensor network nodes placed randomness (often spreading through the aircraft), which resulted in wireless communication distance is not fixed. In order to the save power consumption and extend battery life, PA needs to be adjusted the strength of the output power according to the length of the distance of the wireless communication.

In this design, power transistor is divided into three parts and controlled by Signal Ctr_1, Ctr_2 and Ctr_3, which is shown in Figure 2. When the signal is in high level, it can enable one part of the transistor. And when the signal is in low level, it can disable one part of the transistor. The three bits control signal can enable 7 levels (001-111) of output power of the PA, and shut down the PA when it is 000 [7].

2.4. Differential Cascode Structure

Differential structure has many advantages for the PA. It can suppress common mode noise; increase output voltage swing of the PA. It can offset the parasitic inductance of the power transistor source at encapsulation. And it also can suppress second harmonic and improve the linearity.

In cascode structure of this design [8], the common-source transistor (power transistor) uses the thin gate transistor, which can provide higher gain. The common-gate transistor (switch transistor) uses the thick gate transistor, which ensures its breakdown voltage affordability.

2.5. Stability Control

Stability must be considered when design a PA. The conditions of PA stability is K>1. Where:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} \quad (3)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (4)$$

Series connecting a resistor with the input terminal or parallel connecting a resistor with the output terminal of the PA can make the PA unconditionally stable work [9]. In this design, a low resistance resistor is selected to series connect with the input terminal.

2.6. Load Pull

One of the power amplifier design targets is to obtain the max output power and efficiency. In the design process, load pull [10] simulation is adopted to determine the output matching network. Assuming that output load of the PA is a variable, changing this variable once and gaining an output power every time, and as much as possible the value of this variable is mapped to entire Smith Chart, a series equal power circle and equal efficiency circle can be obtained. In the center of these circles, the maximum output power point and the maximum efficiency point can be determined. Compromising between these two points, the best output load is select. Figure 4 shows one of the simulation results of load pull.

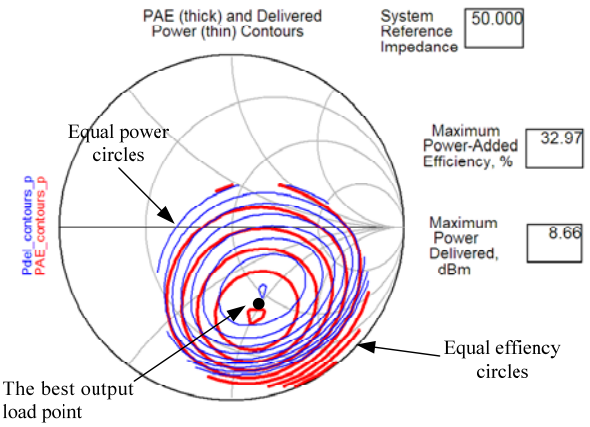

Figure 4. Simulation Result of Load Pull

2.7. Bias Circuit

The bias circuit used to generate the voltage V_{bias}, which is shown in Figure 2. Simulation found that, under conditions of different process corners have a different threshold value voltage V_{th} of the power transistor. V_{th} was small in the FF process, while V_{th} was large in the SS process. If a constant voltage of V_{bias} is maintained, process corner difference will be more obvious. The bias circuit is designed to reduce the differences in different process corners. It outputs a varying voltage of V_{bias}. In FF process corner, it outputs a lower voltage of V_{bias} to adapt V_{th} reduction. And In SS process corner, it output a higher voltage of V_{bias} to adapt V_{th} increase. The simulation results of voltages mentioned above in different corner process are shown in Table 1.

Table 1. Simulation Results of Voltages in PA

Process corner	Vth(V)	Vgs/ Vbias (V)	Vgs-Vth(mV)
TT	0.516	0.55	34
FF	0.463	0.498	35
SS	0.564	0.598	34

3. Experimental Results

Figure 5 shows the microphotograph of the proposed PA. The PA die area is 1070×610μm^2 including bonding pads. The radio frequency choke inductors and the pads determine the area of the PA. The two inductors occupy most of the area and set on the two sides of the layout. And the other parts of the proposed PA use a compact area to set in the center of the die.

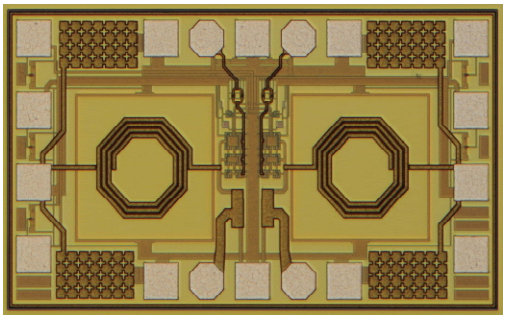

Figure 5. Microphotograph of the Proposed PA

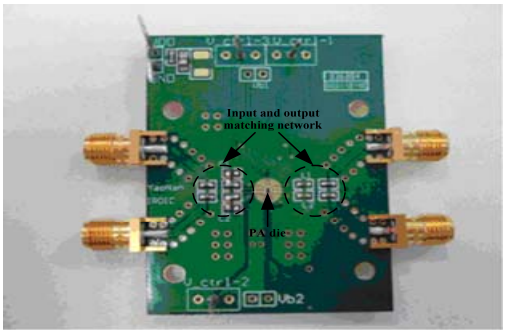

Figure 6. Photograph of the Printed Circuit Board

Bonding test was adopted to measure the proposed PA. The photograph of the printed circuit board is shown in Figure 6. The part of input and output matching network is composed by patch inductors and capacitors, which can be seen on the printed circuit board.

Figure 7 shows the S-parameter measured results of the PA. The tested conditions were set as follows: input power was -30dBm, input frequency was 2.44GHz, and power control code was 111. Then the control code was changed gradually, and measured the S-parameter at every step. And all the S-parameter measured results are summarized in Table 2.

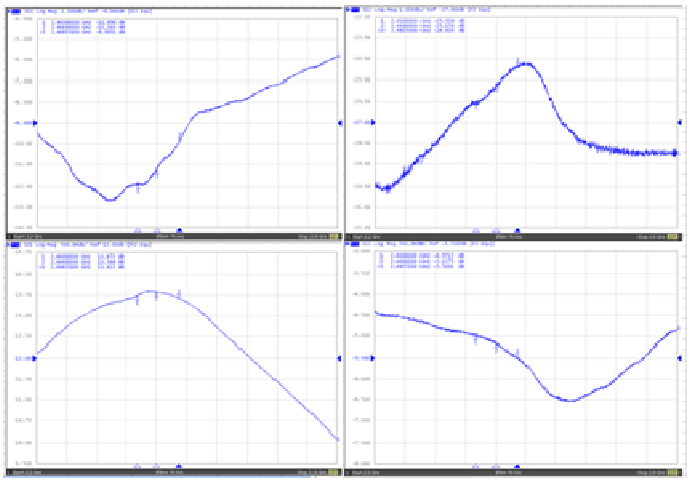

Figure 7. S-parameter Measured Results

Table 2. S-parameter Summary at 2.44GHz

Control code	S11(dB)	S21(dB)	S12(dB)	S22(dB)
111	-11.16	13.57	-25.16	-5.16
110	-11.13	12.44	-25.64	-5.03
101	-11.23	10.91	-26.71	-4.99
100	-10.87	9.12	-26.44	-4.74
011	-10.96	6.59	-25.92	-4.68
010	-10.02	3.22	-26.18	-4.28
001	-9.94	-2.95	-26.67	-4.09

The output power, power gain and work current measured results are shown in Table 3. The tested conditions were set as follows: input frequency was 2.44GHz, and power control code was 111, and change input power from -30dBm to -8dBm. From Table 3, the measured power gain of the PA decreases from 16.88dB to 15.87dB, when input power increases from -30dBm to -9.63dBm. So the input 1dB referred compression point of the PA is -9.63dBm, and the PA's power gain is 15.87dB, when it consumes 15.3mA current. The 1dB compression point is shown in Figure 7. So the PAE of the 1dB compression point is:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \approx \frac{4.2\text{mW} - 0.11\text{mW}}{15.3\text{mW}} \approx 26.73\% \quad (5)$$

Table 3. Output Power, Power Gain and Work Current Measured Results

Input power (dBm)	Output power (dBm)	Power gain(dB)	Work current (mA)
-30	-13.12	16.88	6.9
-20	-3.33	16.67	7.4
-15	1.29	16.29	8.3
-13	3.04	16.04	10.4
-11	4.99	15.99	14.4
-9.63	6.24	15.87	15.3
-8	6.35	14.35	16.9

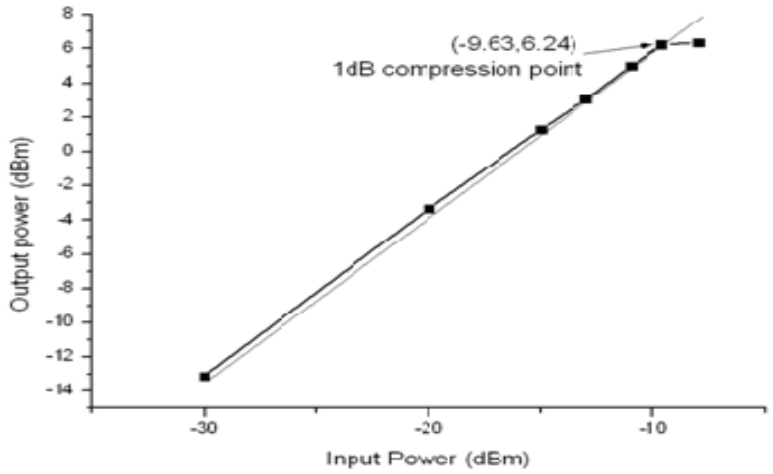

Figure 7. 1dB Compression Point of the PA

The measured results of proposed PA and their comparison to that of other Class A/B PAs are summarized in the Table 4. From Table 4, this work has higher PAE than others PA, and it consumes less power.

Table 4. Peformance Comparison of Class A/B

Parameter	This work	[11]	[12]	[13]
Work frequency (GHz)	2.4-2.4835	2.4-2.4835	2.4-2.480	1.92
Supply voltage (V)	1	1.2	1.8	1.2
Power consumption (mW)	15.3	22	24.25	NA
Output power (dBm)	6.24	7.92	6.4	4
PAE (%)	26.73	25.34	18	26

4. Conclusion

A low voltage of 1V class A/B power amplifier for WSN application was presented in this paper. After the measurement, it achieves 26.73% PAE at 6.24dBm output power. And it only consumes 15.3mW. This work can be applied in the transceiver for WSN system. And it also can be the reference of the further research on low voltage and low power for WSN transceiver.

Acknowledgments

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