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The Study and Achieving of High-precision Data-acquisition Based on ΔΣADC

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Abstract

ΔΣ ADC is used more and more widely, and it is favored for the important reason of high precision. In this paper, working principle and characteristics of ΔΣ modulator and digital filter have been analyzed, and then oversampling, noise shaping and digital filtering characteristics are discussed. Finally, a practical application is illustrated and its basic structure of acquisition circuit is given, the design ideas of single-ended-to-differential driver circuit and front RC filter circuit is highlighted, and the choosing of connection method of multiple channel system is argued.

Keywords: *ΔΣADC, oversampling, noise-shaping, digital filter, high-precision*

1. Introductions

In the field of modern testing, medical treatment, automotive electronics, audio electronics, the requirements of data acquisition is getting higher and higher, a miniaturized, low-cost, high-precision analog-to-digital conversion system is being looked for, and the acquisition system meeting these requirements can be achieved by using ΔΣ analog-to-digital converter [1]. Traditional analog-to-digital converter has analog internal structure which is usually complex and occupies space, and samples signal with Nyquist sampling rate, and the precision is ordinary too. However the analog structure of ΔΣ analog-to-digital converter is small, and most of its parts are digital structure which is easy implemented and controlled. Otherwise its characters, such as unique oversampling mechanism [2], noise-shaping and digital filter, enable it to effectively improve the signal-to-noise ratio and to eliminate high-frequency noise confounded to useful signal, and improve conversion accuracy, and make ΔΣADC very suitable for high-precision applications.

2. Improving Accuracy by Using Delta-sigma Converter

Unlike traditional analog-to-digital converters, a typical internal structure of ΔΣADC is shown in Figure 1. It integrates ΔΣ modulator and digital decimation filter inside, the ΔΣ modulator's responsibility is to oversampling input signal and outputting high-speed low-resolution data stream to the digital decimation filter, and the digital decimation filter's responsibility is to filter and decimate this high-speed data stream, and makes it becoming a low-speed high-resolution multi-bit data values, then outputs the data.

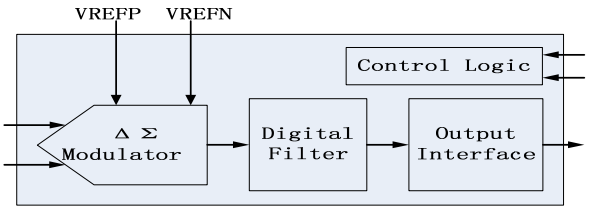

Figure 1. Typical Block Diagram of ΔΣADC

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2.1. ΔΣ Modulator Improving the Signal-to-noise Ratio

The improvement of accuracy is inseparable from improvement of signal-to-noise ratio (SNR), and ΔΣ modulator improves SNR with its working mechanism. Its internal structure is shown in Figure 2.

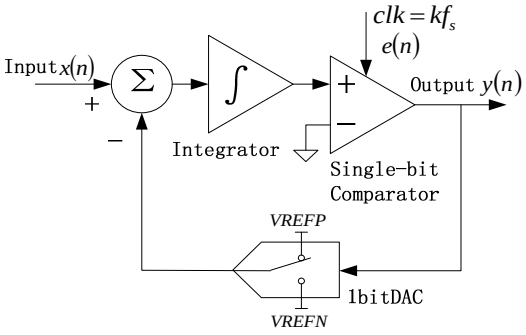


Figure 2. The Internal Structure of ΔΣ Modulator

Inside ΔΣ modulator, input signal is first compared with the feedback, second passed into the integrator for integration operation, and then oversampling quantized in the single-bit comparator, finally the quantized output is fed back to the input by a 1-bit DAC to participate the next conversion and at the same time output to digital decimation filter. Clearly, during conversion the signal quantized is not the input data value, but the difference between the input value and the last quantized value [3]. And the function of 1-bit DAC in the feedback loop is equivalent to a switch, which outputs forward reference voltage when the quantized value is 1 or the negative reference voltage when the quantized value is 0.

How the SNR is improved can be separated to two steps, oversampling and noise shaping. First one is oversampling. Oversampling means sampling with a frequency far higher than the Nyquist sampling rate. And between the Nyquist sampling and the oversampling, the different distribution of quantization noise is shown in Figure 3. The quantization noise after Nyquist sampling is uniformly distributed on the [0,f_s/2] band, and that after oversampling is broadened to [0,kf_s/2]. As the quantization noise power is unconcerned with sampling rate, so when the other conversion conditions is identical, the total quantization noise power in Nyquist sampling and oversampling is equal [4]. With the broadening of noise distribution range, the power density of noise within the useful band is decreased, and then the noise power within the signal band is decreased too, therefore oversampling has improved the signal-to-noise ratio. Assuming oversampling ratio is K, then the quantization noise power within the useful signal frequency band after oversampling is 1/*k* of it after ordinary sampling. So the signal-to-noise ratio is increased with (10lg*k*) *dB*.

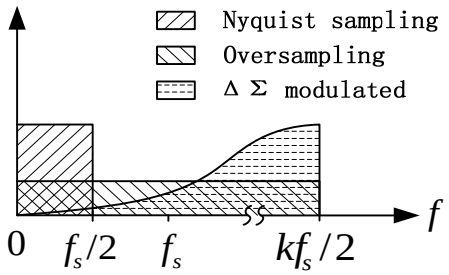


Figure 3. Quantization Noise Distribution Diagram

The second step improving signal-to-noise ratio is quantization noise shaping. Due to the above signal transmission process in ΔΣ modulator, the Z-domain equivalent model of ΔΣ modulator can be obtained as shown in Figure 4.

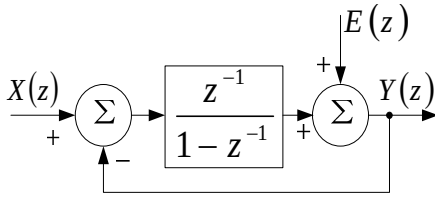


Figure 4. Z-domain Model Diagram of ΔΣ Modulator

Analyzing Figure 4, we get the following equation between input and output.

$$[X(z) - Y(z)] \bullet \frac{z^{-1}}{1 - z^{-1}} + E(z) = Y(z) \quad (1)$$

Simplifying Equuation 1, get the transmission characteristics of ΔΣ modulator.

$$Y(z) = z^{-1} \bullet X(z) + (1 - z^{-1}) \bullet E(z) \quad (2)$$

So the input signal transfer function is z^{-1}, and the quantization noise transfer function is (1-z-1). It is said that in the transmission process, input signal is delayed by one cycle, and quantization noise is transmitted by first-order differential form which is equivalent to high-pass filter and lead to that, shown in Figure 3, after ΔΣ modulating, most quantization noise is transferred to outside the useful band, and noise power on band [0,fs/2] is greatly reduced. The signal-to-noise ratio is substantially increased again after over-sampling [5]. If the integral and summing portion in ΔΣ modulator is second-order or higher order, the quantization noise shaping will be better, the improvement of the signal-to-noise ratio will be more remarkable and the conversion accuracy will be higher.

2.2. Digital Decimation Filter Reducing Noise Aliasing

In order to achieving higher accuracy, the noise after shaping must be effectively filtered. A digital decimation filter is integrated inside ΔΣ ADC, which can filter out the quantization noise shaped by modulator, reduce the demands of anti-aliasing filter circuit, otherwise reduce the frequency of modulator's high-speed output data stream and extract it. As shown in Figure 5, the internal structure of digital decimation filter is formed by the series connection of cascaded comb filter, compensation filter and half-band filter [6].

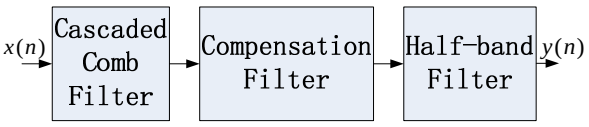
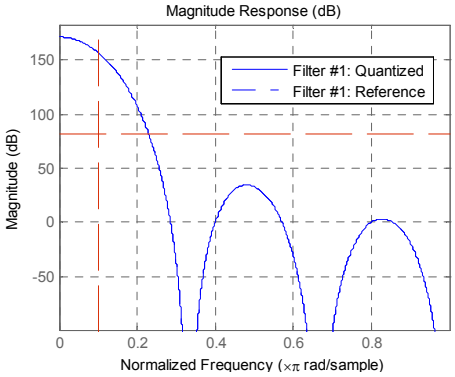
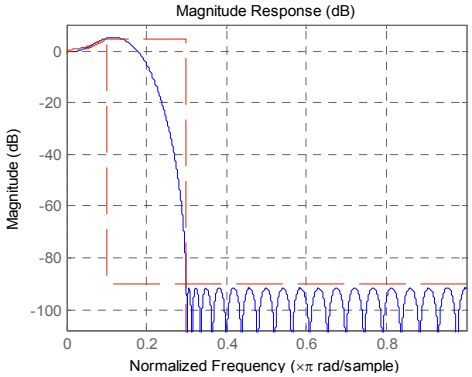


Figure 5. Digital Decimation Filter Block Diagram

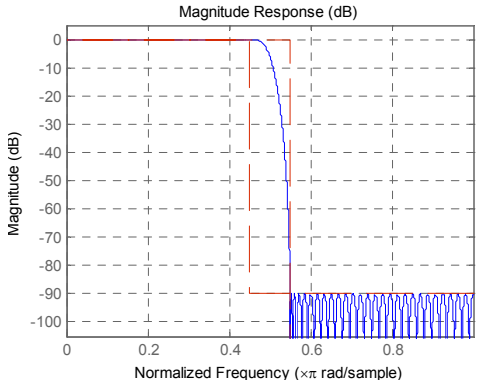
Use MATLAB Filter Design Toolbox to simulate each of the three filters frequency response characteristics, and obtain the result shown as Figure 6(a), (b), (c). The frequency response of cascaded comb filter has a fast pass-band edge roll-off, leading to the unconspicuous boundary between pass-band and stop-band and increasing the noise in pass band. But the frequency response of compensation filter has a heave which can just compensates for the pass band attenuation of front filter [7]. Plus that the half-band filter can accelerate the stop band attenuation, this three filters together make the entire digital decimation filter has a good low-pass filtering effect, and can effectively eliminates the quantization noise shaped by ΔΣ modulator [8]. So the digital decimation filter plays a role same to anti-aliasing filter circuit and reduces the need for additional anti-aliasing demand.



(a) Frequency response of cascaded comb filter



(b) Frequency response of compensation filter



(c) Frequency response of half-band filter

Figure 6. Frequency Response Diagrams of each Grade of Digital Decimation Filter

However except filtering, reducing frequency and extraction is the other two functions of digital decimation filter, which can convert high-speed data stream to low-speed and high-resolution multi-bit data output of ADC [9]. This extraction is periodic and makes the output spectrum of the digital decimation filter cyclical distribute, as shown in Figure 7. Although the digital decimation filter can substantially filter the noise in $[kF_{ms}+f_b,(k+1)F_{ms}-f_b]$, but can not distinguish the frequency components near $kFms$ (k = 1,2, ...), therefore the high frequency aliasing noise in $[kF_{ms}-f_b,kF_{ms}+f_b]$ should be filtered out by external anti-aliasing filter circuit.

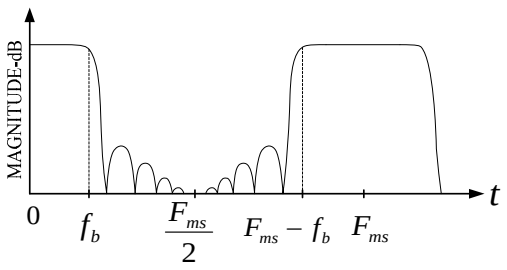


Figure 7. Frequency Response of Digital Decimation Filter

3. Application Examples

Use TI's ADS1271 to constitute a 16 channel synchronous acquisition circuit system which all channels can sample at the same time, single-channel circuit structure is shown in Figure 8. ADS1271 is the heart of converting, which is typical ΔΣ analog-to-digital converter, 24-

bit resolution, and differential input whose range is ±2.5V can efficiently suppress common mode interference [10]. In this application, the input signal is single-end and amplitude range is 0~5V, and it is subtracted by 2.5V in subtracting circuit, and then converted fully-differential signal by the fully-differential amplifier to meet the input range requirements of ADS1271. In addition, RC filter is used to filter out high frequency noise that ADC can not filter out, and use FPGA to control ADC to convert and to provide conversion clock [11]. The highest single-channel sampling rate is optional 50KHz, the conversion data is real-time uploaded or save to the file.

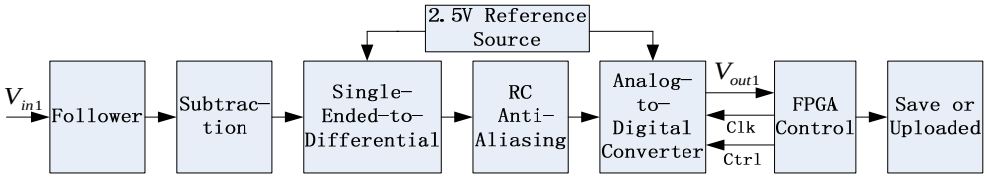


Figure 8. Diagram of Single-channel Acquisition Circuit

3.1. Single-ended-to-differential Circuit

In this applications, single-ended-to-differential circuit is structured with fully-differential op amp OPA1632, whose significant difference with ordinary op amp is enable to output differential signal and has a common-mode voltage input-end. The differential input, output and voltage supply enable it to excellently suppress outside common-mode interference and less susceptible to the outside noise. The single-ended-to-differential circuit driving ADC is shown in Figure 9.

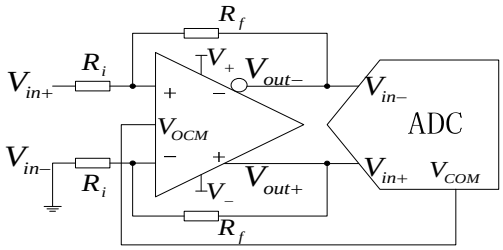


Figure 9. Simplified Diagram of Single-ended-to-differential Circuit Driving ADCs

Differential input and differential output in above circuit are:

$$V_{id} = V_{in+} - V_{in-}$$
$$V_{od} = V_{out+} - V_{out-} \quad (3)$$

The relationship of output and input is:

$$V_{od} = AV_{id} = \frac{R_f}{R_i} \bullet V_{id} \quad (4)$$

Voltage gain can be changed by changing the value of R_f and R_i, so that the output to meet the application requirements. V_{OCM} is the common-mode voltage input, and has the following relationship with differential output.

$$V_{OCM} = \frac{V_{out+} + V_{out-}}{2} \quad (5)$$

This common-mode voltage input and the reference voltage input of the ADS1271 are parallel connected to +2.5 V reference voltage source, so that OPA1632 differential output and ADS1271 differential inputs use the same common-mode voltage reference value to ensure the correctness of voltage conversion. In addition, OPA1632 also have the advantages of large gain bandwidth, high slew rate, small input noise, very low distortion, and good driving ability, which ensure the maximization of signal-to-noise ratio and dynamic range.

3.2. Single-pole RC Filter Circuit

As it is mentioned in the end of 2.2, although the digital decimation filter of ΔΣ ADC can filter out most of the high-frequency noise, but also be helpless to noise in [kF_{ms}-f_b,kF_{ms}+f_b], therefore an external anti-aliasing filter circuit is also needed. And this low-pass filter circuit is required that its transition band falls in the range of [f_b,F_{ms}-f_b] and has a low pass band attenuation. In this application, use single-pole RC filter to achieve. Set the target bandwidth is 10 kHz, and require the pass-band attenuation ratio α>0.99. On the basis of attenuation ratio formula of a single-pole filter.

$$\alpha = \frac{1}{\sqrt{1+(2\pi f_b RC)^2}} > 0.99 \tag{6}$$

Substitution with the application parameters into the above equation, so:

$$RC < \sqrt{\frac{1-\alpha^2}{(2\pi f_b \alpha)^2}} \approx 2.27 \times 10^{-6} s \tag{7}$$

Take RC 2us, so the cut-off frequency is:

$$f_b = \frac{1}{2\pi RC} \approx 79.6 kHz \tag{8}$$

On the foundation of meeting requires of pass band attenuation of useful signal, examine how the RC attenuates aliasing noise in the band [kF_{ms}-f_b,kF_{ms}+f_b]. ADS1271 is operated in high-resolution mode and oversampling rate is 128, when signal channel sampling rate is maximum 50kHz, so the oversampling speed of modulator is Fms=128×50k=6.4MHz, and the signal attenuation ratio α_1 of this RC in first band [6.4±0.01] is:

$$\begin{aligned}\alpha_1 &= \frac{1}{\sqrt{1+(2\pi f_b RC)^2}} \\ &= \frac{1}{\sqrt{1+(2\pi \times 6.4 \times 2)^2}} \approx 0.012\end{aligned} \tag{9}$$

It is equal to -38.42dB. In the same way, the signal attenuation ratio α_2 on second band [12.8±0.01] is 0.006, that is -44.13dB.

It is shown that the noise attenuation of first two aliasing bands is very ideal, and supperadd that the bandwidth limitations of the analog-to-digital converter itself can inhibit the noise of high order frequency band, this RC filter can meet the application requirements.

3.3. Selection of Transmission Mode

To acquisition application using multi-ADS1271, company TI comes up with a called daisy-chaining connection mode, as shown in Figure 10. Multiple ADS1271s are sequentially cascaded together through connecting the DOUT of one ADS1271 to the DIN of next ADS1271. For synchronization, a single serial clock SCLK is used for all ADS1271s, and connect all the synchronize input $\overline{SYNC}$ together when using SPI format.

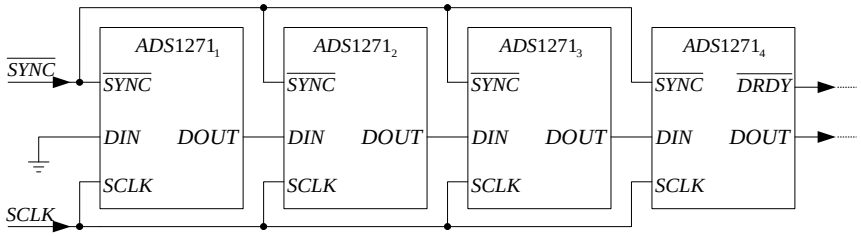


Figure 10. Diagram of Daisy Chaining for Multiple ADS1271s System

This kind of connection can simplify the serial interface connection and save circuit space, but the ADS1271 number is limited which connected in the chain. In the chain, the data at DIN pin and DOUT is transferred at falling edge SCLK clock, one falling edge come, then 1-bit binary data output. So it will take 24 SCLK clocks to output all the data produced by one conversion of ADS1271. So if having n ADS1271s in the system, to ensure all data not be lost, it will takes 24n SCLK clocks at lest. So the SCLK frequency affects the number of ADS1271 in the chain, which is relevant with the interface style and the operation mode. The interface mode can be set to SPI or Frame Sync Serial Interface and the operation mode can be High-Speed, High-Resolution and Low-Power. In this application, take Frame Sync Serial Interface and high-precision mode, so requires:

$$\frac{f_{CLK}}{f_{FRAME}} = 512 \quad \text{and} \quad f_{SCLK} = 128\, f_{FRAME}\ , \tag{10}$$

Here f_{FRAME} is the frequency of framing, the reciprocal of frame period. Therefore, on the condition that single-channel ADS1271 operates at the highest sampling rate 52.734ksps, then input clock is f_{CLK}=27*MHz*, so the serial clock frequency f_{SCLK}=0.25f_{CLK}=6.75*MHz*. Therefore the maximum number of ADS1271 can be daisy-chained is:

$$\frac{6.75\,MHz}{24 \times 52.734\,ksps} \approx 5.3 \tag{11}$$

That is 5, which can not meet the requirements of 16-channel simultaneous sampling. Consequently, use independent parallel connection between channels to achieve the acquisition in this application.

4. Conclusion

In this article, we analyze the internal structure and characteristics of ΔΣ ADC modulator and digital decimation filter, state ΔΣADC oversampling, noise shaping and filter extracting characteristics, and expound the principle of ΔΣADC high SNR and easy anti-aliasing for ΔΣADC. In the end taking a practical application as example, analyze single-ended-to-differential circuit, RC anti-aliasing circuit and the selection of work mode of ΔΣADC, and provide a basis for high-precision data acquisition using ΔΣADC.

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