Indonesian Journal of Electrical Engineering and Computer Science
Vol. 25, No. 1, January 2022, pp. 138~143
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v25.i1.pp138-143

Characterization of silicon tunnel field effect transistor based on charge plasma

Firas Natheer Abdul-kadir, Faris Hassan Taha
Department of Electrical Engineering, College of Engineering, University of Mosul, Mosul, Iraq

Article Info

Article history:

Received Jun 25, 2021
Revised Oct 26, 2021
Accepted Nov 26, 2021

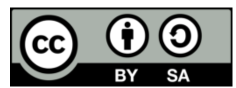
Keywords:

Biosensor
Charge plasma
MOSET
TCAD
TFET

ABSTRACT

The aim of the proposed paper is an analytical model and realization of the characteristics for tunnel field-effect transistor (TFET) based on charge plasma (CP). One of the most applications of the TFET device which operates based on CP technique is the biosensor. CP-TFET is to be used as an effective device to detect the uncharged molecules of the bio-sample solution. Charge plasma is one of some techniques that recently invited to induce charge carriers inside the devices. In this proposed paper we use a high work function in the source (ϕ=5.93 eV) to induce hole charges and we use a lower work function in drain (ϕ=3.90 eV) to induce electron charges. Many electrical characterizations in this paper are considered to study the performance of this device like a current drain (ID) versus voltage gate (Vgs), I_{ON}/I_{OFF} ratio, threshold voltage (VT) transconductance (gm), and sub-threshold swing (SS). The signification of this paper comes into view enhancement the performance of the device. Results show that high dielectric (K=12), oxide thickness (Tox=1 nm), channel length (Lch=42 nm), and higher work function for the gate (ϕ=4.5 eV) tend to best charge plasma silicon tunnel field-effect transistor characterization.

This is an open access article under the CC BY-SA license.



Corresponding Author:

Firas Natheer Abdul-kadir
Department of Electrical Engineering, College of Engineering, University of Mosul
Mosul, Iraq
Email: firas_nadheer@uomosul.edu.iq

1. INTRODUCTION

Charge plasma and electrostatic techniques are recently devised techniques to provocation the virtual doping inside the device [1], [2]. In the charge plasma technique, the charge carriers are motivated within the materials by employing different work functions on the drain and source regions, whereas in the electrostatic technique, the charge carriers are motivated within the materials by employing external bias [3], [4]. The tunnel field-effect transistor (TFET) device is vastly studied within the containing the virtual doping techniques [5]-[7]. TFET can be regarded as a promising alternative device of metal-oxide-semiconductors field effect transistor (MOSFET) to overcome the imperfection of short channel effects and betterment the characteristics of the device such as high I_{ON}/I_{OFF} ratio, low OFF-current state lower subthreshold slope and minimize the power consumption [8]-[11]. The operating mechanism of TFET is based on the band-to-band tunneling phenomenon, while in MOSFET, the operating mechanism is based on the thermionic emission technique [12]-[14]. Besides all these advantages, but TFET is still suffering from some problems and facing challenges like low ON-current state, ambipolar behavior (conduction of current when the gate bias is negative), and higher parasitic capacitances [15]-[18].

One of the most applications of the charge plasma tunnel field-effect transistor (CP-TFET) is the biosensor device which operates based on charge plasma technique [19]. There are other types of biosensors

device that depends on the ion-sensitive field-effect transistor (ISFET) [20]. ISFET operates on fundament the presence of ions in the bio-sample solution below the dielectric gate, but ISFET cannot detect the uncharged molecules for any bio-sample, so this can be considered as limiters of ISFET [19]. While CP-TFET has been verified to be used as an effective device to detect the uncharged molecules of the bio-sample solution [21], [22]. Also, another type of FET biosensor is the dielectric modulated device has named DM-FET biosensor and DM-TFET which have higher sensitivity for bio-sample [23], [24].

This paper overcomes the problem of the detect uncharged molecules and precision of the sensitivity, by collecting all the beneficial features of the dielectric modulated (DM) biosensor, charge plasma conception and TFET device, the DM CP-TFET biosensor has been an ongoing device and its better performance as compared with other types of biosensor [25]-[27]. So, this proposed paper aims to realize and study the characteristics of TFET device that depend on the CP technique, and the signification of the work comes into view enhancement the performance of the device (sub threshold slop and I_{ON}/I_{OFF} ratio) which used as a biosensor applications.

2. DEVICE STRUCTURE AND PARAMETERS

The substructure of the device, siliconcharge plasma tunnel field-effect transistor (CP-TFET) is shown as in Figure 1. The source and drain regions are established on the intrinsic body by prober metal work function. “P+” source is implanted by (ϕS=5.93 eV) and “N+” drain is implanted by (ϕD =3.9 eV). The gate regions are established on SiO2 by different metal work functions. Gate1 and Gate2 are implanted by (ϕ =3.9 eV), Gate3, and Gate4 (ϕ =4.0 eV). The structure of the device is making the concentrations distribution electron and hole are available regular at source and drain electrode, which make better control and a great ON current-state [28]-[30]. The concentration of substrate region (body) is 1×10^{15} cm^{-3} which represents the silicon intrinsic and the length of the channel is 43 nm. Oxide layer thickness (SiO2) under the gate is 3 nm and the length of the gate under lap region (dielectric) or space length is 7 nm, and the applied voltage on the drain terminal (Vd) is 0.5 V.

In this article, we study and investigate the important electrical parameter (performance) for the device such as I_{ON}, I_{ON}/I_{OFF} ratio, sub-threshold slope (SS), the threshold voltage (VT) and transconductance (gm). The performance of the device was observed by varying many factors for the device such as different dielectric constant (under lap region(K)), oxide layer thickness (T_{OX}), and channel length (LCh) [31], [32].

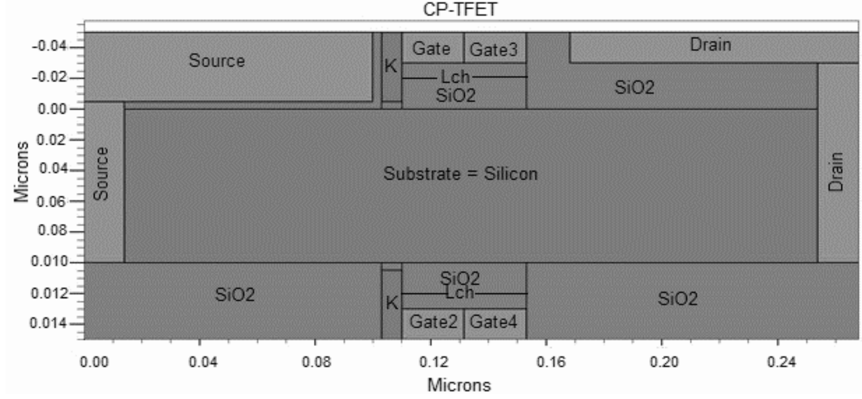


Figure 1. Schematic structure of a CP-TFET

3. RESULTS AND DISCUSSION

The simulation results are taken by using the Technology Computer Aided Design (TCAD) tool. The gate voltage (V_{GS}) is plotted against both drain current (I_{ON}) and transconductance (gm) in Figure 2 and Figure 3 at K=1,2,4,8, and 12). In Figure 2 is the effect of dielectric constant in drain current, wherein the (ION) increases when (K) increases and so on in Figure 3 of the (gm).

The relation between dielectric constant (k) versus the ratio of (I_{ON}/I_{OFF}) and subthreshold slope (SS) are plotted in Figure 4, which shows the increase of (K) led to an increase in the I_{ON}/I_{OFF}, while the opposite occurs in (SS), where increasing of (K), result in (SS) will decrease. Also, can be found the intersection point between them in about 5.2 of (K). The drain current and transconductance are plotted against voltage gate with a different thickness of T_{OX} = (1,2,3, and 4) as shown in Figures 5 and 6 respectively. The plots validate the performance of the device, at decreasing of the (T_{OX}), the I_D current and gm will be increasing. That’s mean the proportional is reverse between (I_D and gm) with (T_{OX}).

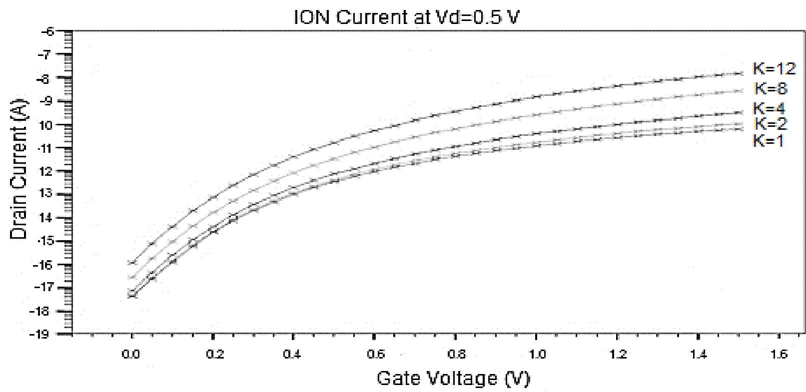


Figure 2. I_D=(I_{ON}) versus voltage gate (V_{GS}) at varying (K)

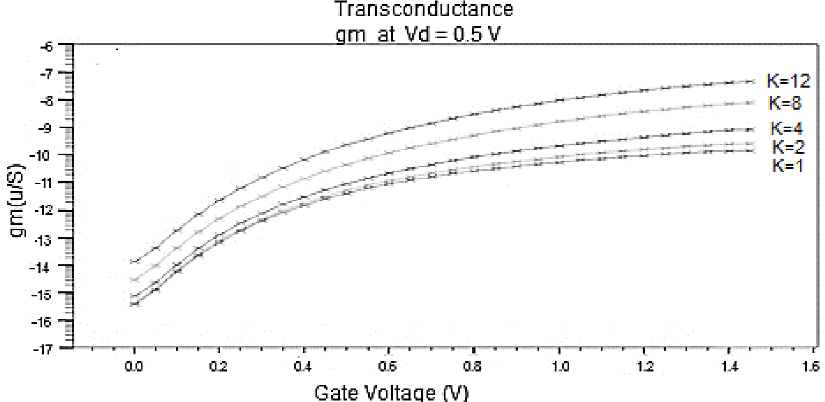


Figure 3. Transconductance (gm) versus voltage gate at varying (K)

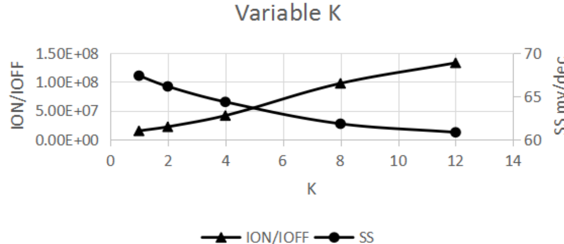


Figure 4. I_{ON}/I_{OFF} ration and (SS) versus different dielectric constant of (k)

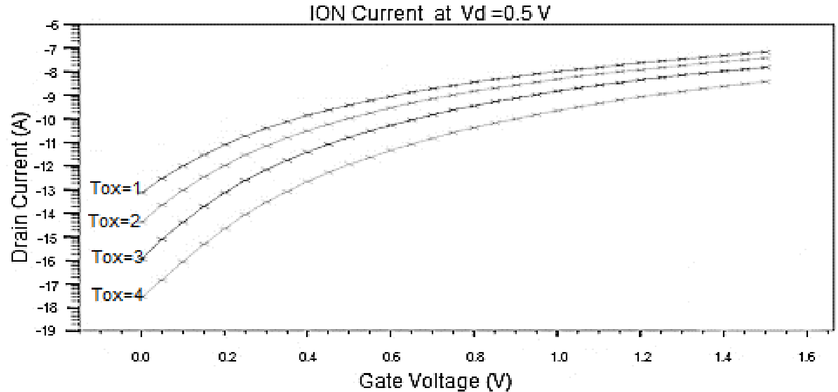


Figure 5. I_D (I_{ON}) versus voltage gate (V_{GS}) at varying (T_{OX})

The relation between thickness material (T_{OX}) of (SiO2) versus the ratio of I_{ON}/I_{OFF} and (SS) are plotted in Figure 7, which shows the minimum value of I_{ON}/I_{OFF} ratio (1.1×10^{6}) with VD= 0.5 V was gotten at T_{OX}=(1 and 2) nm, but at T_{OX}=3 nm, the I_{ON}/I_{OFF} ratio began increasing until reached to a maximum value (1.3×10^{9}) at T_{OX}=4 nm. While occurs opposite in (SS), where the minimum value of T_{OX}= 1 nm at the same value of VD=0.5 V, we obtained the worse case of SS characteristics (84.19 mV/dec), but after that, when the value of T_{OX} began increasing, the value of SS became decreasing until reached to the best value of SS characteristics (63.26 mV/dec). Also, we can find the intersection point between them in about 3.7 of (T_{OX}).

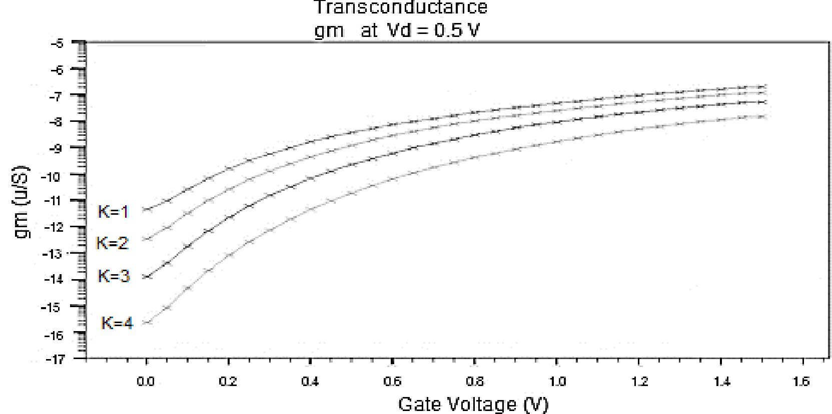


Figure 6. Transconductance (gm) versus voltage gate at varying (T_{OX})

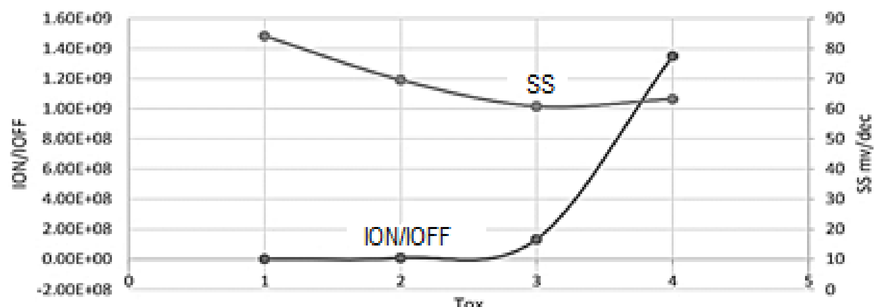


Figure 7. I_{ON}/I_{OFF} ration and (SS) versus different thickness constant of (T_{OX})

The three parameters (work function, channel length and oxide thickness) are taken to investigation the characteristics of the charge plasma tunnel field-effect transistor (CP-TFET) device, like threshold voltage (Vt), I_{ON} current, I_{OFF} current, I_{ON}/I_{OFF} ratio, subthreshold slop (SS) and transconductance (gm). We set the work function of (gate1 and gate2) at fixed value (3.9 ev), channel length at fixed value (43 nm) and oxide thickness at fixed value (3 nm). While the work function of (gate3 and gate4) are set at variable value (4.5, 4.3, 4.1, and 3.9) ev. All the electrical characteristic of the device was obtained at Vd= 0.5V, dielectric constant (K) =12 and temperature degree of device at 300 K as shown as in Table 1.

The relation between channel length (Lch) versus the ratio of (I_{ON}/I_{OFF}) and subthreshold slope (SS) are plotted in Figure 8, which shows the increase of (Lch) led to decreasing in the I_{ON}/I_{OFF}, while the opposite occurs in (SS), where increasing of (Lch), will result of decreasing in (SS).

Table 1. Electrical characteristic of CP-TFET (k=12 and Vd=0.5V)

Work Function (Gate3+Gate4) (ev)	Channel Length (nm)	T_{OX} (nm)	Vt (V)	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	SS mmmV/dec	Gm u/S	Work Function (Gate1+Gate2) (ev)
4.5	43	3	0.954	1.52×10^{-8}	3. 43×10-^{18}	$4.4\times10^{+9}$	33.84	0.050	3.9
4.3	43	3	0.954	1.53×10^{-8}	2. 07×10-^{17}	$7.4\times10^{+8}$	50.75	0.051	3.9
4.1	43	3	0.954	1.54×10^{-8}	3.9.87×10-^{17}	$1.5\times10^{+8}$	59.90	0.052	3.9

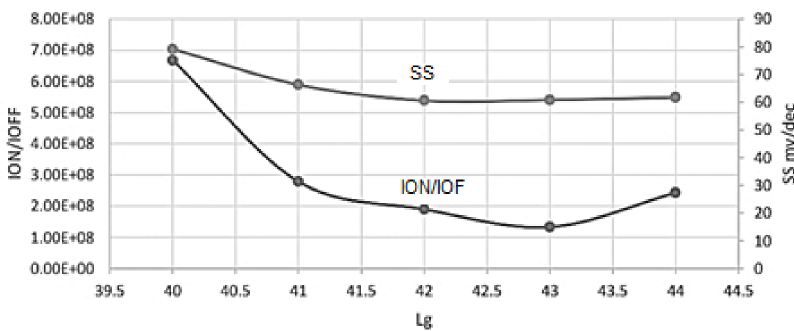


Figure 8. I_{ON}/I_{OFF} ration and (SS) versus different thickness constant of (Lch)

4. CONCLUSION

In this article, we have been taken many factors to study and analyze the characteristics of silicon tunnel field-effect transistors based on charge plasma. The performance of the charge plasma tunnel field-effect transistor (CP-TFET) device studies and investigated through this paper. By using plasma technique concept based on TFET structure. A dual-gate metal structure and gate under lap region is proposed to enhancement the characteristic of the device. By simulation study, the CP-TFET device shows making better performance for I_{ON} =1.5×10^{-8}A at (K=12, Lch=43 nm and Tox=3 nm), I_{ON}/I_{OFF}=1.3×10^{+9} at (K=12, Lch=43 nm and Tox=4 nm), and sub threshold slop SS=33.84 mv/dec at (K=12, work function for gate3 and gate4=4.5 ev).

ACKNOWLEDGEMENTS

The authors would like to thank the University of Mosul for scientific support.

REFERENCES

[1] C. Duvvury, "A guide to short-channel effects in MOSFETs," in *IEEE Circuits and Devices Magazine*, vol. 2, no. 6, pp. 6-10, Nov. 1986, doi: 10.1109/MCD.1986.6311897.

[2] Q. Chen, B. Agrawal, and J. D. Meindl, "A comprehensive analytical subthreshold swing (S) model for double-gate MOSFETs," in *IEEE Transactions on Electron Devices*, vol. 49, no. 6, pp. 1086-1090, June 2002, doi: 10.1109/TED.2002.1003757.

[3] K. Boucart and A. M. Ionescu, "Double-Gate Tunnel FET With High-k Gate Dielectric," in *IEEE Transactions on Electron Devices*, vol.54, no. 7, pp. 1725-1733, July 2007, doi: 10.1109/TED.2007.899389.

[4] A. Sunny and R. K. Sarin, "Gate misalignment effects on analog/RF performance of charge plasma-based doping-less tunnel FET," in *Applied Physics A*, vol. 123, no. 6, pp. 413, May 2017, doi:10.1007/s00339-017-1029-8.

[5] M. J. Kumar and K. Nadda, "Bipolar Charge-Plasma Transistor: A Novel Three Terminal Device," in *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 962-967, April 2012, doi: 10.1109/TED.2012.2184763.

[6] N. Kumar and A. Raman, "Design and Analysis of Novel Charge-Plasma Based Dopingless U-Shaped FET," *2019 6th International Conference on Signal Processing and Integrated Networks (SPIN)*, 2019, pp. 200-202, doi: 10.1109/SPIN.2019.8711739.

[7] F. N. Abdul-kadir, K.K. Mohammad, and Y. Hashim, "Investigation and design of ion-implanted MOSFET based on (18 nm) channel length", *TELKOMNIKA Telecommunication, Computing, Electronics and Control*, vol. 18, no. 5, pp. 2635-2641, Oct. 2020, doi: 10.12928/TELKOMNIKA.v18i5.15958.

[8] H. W. Kim and D. Kwon, "Low-Power Vertical Tunnel Field-Effect Transistor Ternary Inverter," in *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 286-294, 2021, doi: 10.1109/JEDS.2021.3057456.

[9] F. N. Abdul-kadir, Y. Hashim, and W. A. Shaif, "Temperature characteristics of Gate all around nanowire channel Si-TFET," *Journal of Physics: Conference Series, 5th International Conference on Electronic Design (ICED) 2020*, Aug. 2020, vol. 1755 doi:10.1088/1742-6596/1755/1/012045.

[10] W. Y. Choi, B. Park, J. D. Lee, and T. K. Liu, "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec," in *IEEE Electron Device Letters*, vol. 28, no. 8, pp. 743-745, Aug. 2007, doi: 10.1109/LED.2007.901273.

[11] S. Sahoo, S. Dash, and G. P. Mishra, "An Accurate Drain Current Model for Symmetric Dual Gate Tunnel FET Using Effective Tunneling Length," *Nanoscience & Nanotechnology-Asia*, vol. 9, no. 1, pp. 85-91, Jan. 2019, doi: 10.2174/2210681207666170612081017

[12] V. Vijayvargiya, B. S. Reniwal, P. Singh, and S. K. Vishvakarma, "Analogue/RF performance attributes of underlap tunnel field effect transistor for low power applications," *Electron. Letters*, vol. 52, no. 7, pp. 559-560, 2016, doi: 10.1049/el.2015.3797.

[13] G. Wadhwa and B. Raj "An Analytical Modeling of Charge Plasma based Tunnel Field Effect Transistor with Impacts of Gate underlap Region," *Superlattices and Microstructures*, vol. 142, no. 106512, 2020, doi:10.1016/j.spmi.2020.106512.

[14] F. Natheer, Y. Hashim, and M. N. Shakib, "Review of Nanosheet Transistor Technology," *Tikrit Journal of Engineering science (TJES)*, vol. 1, no. 28, pp. 40-48, 2021, doi: 10.25 30/tjes.28.1.05.

[15] B. Jena, K. Bhol, U. Nanda, S. Tayal, and S. R. Routray, "Performance Analysis of Ferroelectric GAA MOSFET with Metal Grain Work Function Variability," *Silicon*, April 2021, doi: 10.1007/s12633-021-01031-5.

[16] Hraziia, A. Vladimirescu, A. Amara, and C. Anghel, "An analysis on the ambipolar current in Si double-gate tunnel FETs," *Solid-State Electron*, vol. 70, pp. 67-72, Apr. 2012, doi: 10.1016/j.sse.2011.11.009.

[17] V. Vijayvargiya and S. K. Vishvakarma, "Effect of Drain Doping Profile on Double-Gate Tunnel Field-Effect Transistor and its Influence on Device RF Performance," in *IEEE Transactions on Nanotechnology*, vol. 13, no. 5, pp. 974-981, Sept. 2014, doi: 10.1109/TNANO.2014.2336812.
[18] A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," in *Proceedings of the IEEE*, Dec. 2010, vol. 98, no. 12, pp. 2095-2110, doi: 10.1109/JPROC.2010.2070470.
[19] N. Shafi, C. Sahu, C. Periasamy, and J. Singh, "SiGe Source Charge Plasma TFET for Biosensing Applications," *2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2017, pp. 93-98, doi: 10.1109/iNIS.2017.29.
[20] S. Tayal, G. Vibhu, S. Meena, and R. Gupta, "Optimization of Device Dimensions of High-k Gate Dielectric Based DG-TFET for Improved Analog/RF Performance", *Silicon*, May 2021, doi: 10.1007/s12633-021-01127.
[21] R. Narang, K. V. S. Reddy, M. Saxena, R. S. Gupta, and M. Gupta, "A Dielectric-Modulated Tunnel-FET-Based Biosensor for Label-Free Detection: Analytical Modeling Study and Sensitivity Analysis," in *IEEE Transactions on Electron Devices*, vol. 59, no. 10, pp. 2809-2817, Oct. 2012, doi: 10.1109/TED.2012.2208115.
[22] M. J. Kumar and S. Janardhanan, "Doping-Less Tunnel Field Effect Transistor: Design and Investigation," in *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3285-3290, Oct. 2013, doi: 10.1109/TED.2013.2276888.
[23] S. Kanungo, S. Chattopadhyay, P. S. Gupta and H. Rahaman, "Comparative Performance Analysis of the Dielectrically Modulated Full- Gate and Short-Gate Tunnel FET-Based Biosensors," in *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 994-1001, March 2015, doi: 10.1109/TED.2015.2390774.
[24] R. Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Dielectric Modulated Tunnel Field-Effect Transistor—A Biomolecule Sensor," in *IEEE Electron Device Letters*, vol. 33, no. 2, pp. 266-268, Feb. 2012, doi: 10.1109/LED.2011.2174024.
[25] S. Sahoo, S. Dash, and G. P. Mishra, "Work-function modulated hetero gate charge plasma TFET to enhance the device performance," *2019 Devices for Integrated Circuit (DevIC)*, 2019, pp. 461-464, doi: 10.1109/DEVIC.2019.8783943.
[26] A. Bhattacharyya, M. Chanda, and D. De, "GaAs0.5Sb0.5/ In0.53Ga0.47As heterojunction dopingless charge plasma-based tunnel FET for analog/digital performance improvement," *Superlattices and Microstructures*, vol. 142, no. 106522, 2020, doi: 10.1016/j.spmi.2020.106522.
[27] N. Kumar and A. Raman, "Performance Assessment of the Charge-Plasma-Based Cylindrical GAA Vertical Nanowire TFET With Impact of Interface Trap Charges," in *IEEE Transactions on Electron Devices*, vol. 66, no. 10, pp. 4453-4460, Oct. 2019, doi: 10.1109/TED.2019.2935342.
[28] S. Anand, S. I. Amin, and R. K. Sarin, "Performance analysis of charge plasma-based dual electrode tunnel FET," *Journal of Semiconductors*, vol. 37, no. 5, pp.054003, Feb 2019, doi:10.1088/1674-4926/37/5/054003.
[29] N. Parmar, D. S. Yadav, S. Kumar, R. Sharma, S. Saraswat, and A. Kumar, "Performance Analysis of a Novel Dual Metal Strip Charge Plasma Tunnel FET," *2020 IEEE International Students' Conference on Electrical,Electronics and Computer Science (SCEECS)*, 2020, pp. 1-5, doi: 10.1109/SCEECS48394.2020.112.
[30] F. N. Abdul-kadir, Y. Hashim, M. N. Shakib, and F. H. Taha, "Electrical characterization of si nanowire GAA-TFET based on dimensions downscaling," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 11, no. 1, pp. 780-787, 2021, doi: 10.11591/ijece.v11i1.pp780-787.
[31] M. J. Carra, H. Tacc, and J. Lipovetzky, "Performance evaluation of GaN and Si based driver circuits for a SiC MOSFET power switch," *International Journal of Power Electronics and Drive Systems(IJPEDS)*, vol. 12, no. 3, pp. 1293-1303, Sep. 2021, doi: 10.11591/ijpeds.v12.i3.pp1293-1303.
[32] S. Tayal, P. Samrat, V. Keerthi, B. Vandana, and S. Gupta, "Channel thickness dependency of high-k gate dielectric based double-gate CMOS inverter," *International Journal of Nano Dimension*, vol. 11 Issue 3, pp. 215-221, 2020.

BIOGRAPHIES OF AUTHORS

Firas Natheer Abdul-kadir Was received the B.Sc. in Medical Instruments Engineering from Mosul Technical College and Master of Engineering in Electronics and Communications Engineering from the University of Mosul, Mosul, Iraq, in 1998 and 2013 respectively. He is currently an Assistant Lecturer in the Department of Electrical Engineering, College of Engineering, Mosul University, Mosul, Iraq. His research interests include Microelectronics and Nano electronic, MOSFET nano-structure. He can be contacted at email: firas_nadheer@uomosul.edu.iq.

Faris Hassan Taha Was received the MSc degree in Electronic and communication from the University of Mosul, Mosul, Iraq, in 1995 and received PhD degree in 2013 in Solid State Electronics from University of Mosul, Mosul, Iraq. His research interests include Microelectronics and Nanoelectronics. He can be contacted at email: f.h.aldabbagh@uomosul.edu.iq.