# Implementation three-step algorithm based on signed digit number system by using neural network 

Qabeela Q. Thabit ${ }^{1}$, Alyaa Ibrahim Dawood ${ }^{2}$, Bayadir A. Issa ${ }^{3}$<br>${ }^{1}$ Basrah Education Directorate, Ministry of Education, Basrah, Iraq<br>${ }^{2}$ Engineering Technical College, Southern Technical University, Basrah, Iraq<br>${ }^{3}$ Management Technical College, Southern Technical University, Basrah, Iraq

## Article Info

## Article history:

Received Mar 8, 2021
Revised Nov 2, 2021
Accepted Nov 4, 2021

## Keywords:

Addition operation
Artificial neural network
Basic arithmetic neural network unit
Binary modified signed digit number
Three-step algorithm


#### Abstract

The need for a simple and effective system that works with high efficiency features such as high processing speed, the ability to solve problems by learning method and accomplish the largest amount of data processing accurately and in little time produces that system, which attracted the efforts of the researcher to employ neural networks in computing away from the complexities that burden traditional computers. We presented a model for the design of the arithmetic circuit for the process of addition the sign digit numbers in a new way to deal with the arithmetic operations, which employment of the use of neural networks, this model includes a theoretical and practical simulation of them. The model relied on the implementation of the addition process based on a three-step algorithm adopted by the signed systems. Which is characterized by the possibility of execution in a parallel way, and therefore it provides the advantage of completion of arithmetic operation regardless of the length of their operands, or in other words, whatever the number of bits in the operands. The simulation of the model is done by entering operands for 6 addition operations (each one has operands are 15 -bit length) to be executed simultaneously.


This is an open access article under the CC BY-SA license.


## Corresponding Author:

Qabeela Q. Thabit
Basrah Education Directorate, Ministry of Education
Basrah, Iraq
Email: qabelh2010@gmail.com

## 1. INTRODUCTION

Many applications and processes are utilized in conjunction with algorithms to complete the calculations. DNA was used in the computations in the recent past [1]. The very high speed integrated circuit (VHSIC) hardware description language (VHDL) is another technique utilized in this domain [2], [3]. Today one of the most important techniques of soft computing is artificial neural networks, which have been researched, studied and applied on a large scale during the last two decades. In recent times, the neural network has been widely used in all fields, especially engineering, medical, economic and, others [4]-[6], because the neural network is characterized by parallel processing of data regardless of its size, meaning that it provides high speed and capacity for processing in addition to being mimics the way of thinking in the human mind [7]. Research continued in the field of designing logic gates using the neural network, and the most important of which is what Yellamraju et al. [8], presented in achieving many basic logic gates. Also, the basic logic gates (AND, OR, XOR) were presented with a systematic study to choose the threshold values and weights for the implementation of any complex network, where truth tables were used to verify the completion of logic circuits using neural networks in an easier way [9]. The neural network has entered into a
wide range of prediction applications industrial process control, sales forecasting, risk management, and customer research data validation. Also, in the field of different management applications [10], artificial intelligence in different fields as medicine, all types of modern technologies with soft computing [11]-[15], business applications [16] and recognition research which including as example, recognition of network speakers, facial recognition, handwritten word recognition and three-dimensional recognition [17].

In designing various arithmetic circuits, researchers used many digital systems, including but not limited to the binary system [18], the residual number [19], the redundant number [20], multivalued radix number [21], and signed digit number system which gives two advantages, first allows to performing arithmetic operation in parallel manner and reduced number of carry propagation steps [22]-[24]. while designing logic circuits using neural networks, it was mostly using binary systems [25]-[27], a few papers dealt with the design in a neural network using sign digit number system as construct counters by Cotofana and Vassiliadis [28]. In comparison to analog computing, digital computing approaches have already generated enormous gains in speed, accuracy, and adaptability. However, due to the "Von Neumann bottleneck problem," digital electronic computers are unable to process vast amounts of data at a high rate. To overcome this problem, we suggest this paper as one of the solutions, the propose model has been established using the parallel algorithm in order to perform the arithmetic operations such as one step, two-step, and three-step algorithm. In this work, two arithmetic circuits designed for addition signed digit number system depending on this algorithm using neural networks, in a new way that gave an efficient system include choosing suitable algorithm and mathematical function that perform its rules in an artificial neural network.

## 2. BACKGROUND

### 2.1. Artificial neural network principle

The first simulating model to the work of a biological neuron presented by the scientist McCulloch and Pitts in 1943, as computational model for a binary-threshold unit represents an artificial nerve cell operating in separate time by integrating mathematical logic and neurophysiology [29]. The output of the neuron is equals one when the input of the activation function is more than or equivalent to threshold term otherwise the output is equal to -1 . The simplest form of an artificial neural network is made up of the following components: the input layer, which includes the group of entries that are summed into the summation function, and then the processing takes place in the activation function that represents the output layer as shown in Figure 1, the simpler form for the multi-layer artificial network, which is a more complex level than the simple network, consists of an input layer, hidden layer, and the output layer shown in the Figure 1 [11].


Figure 1. Structure of an artificial neuron and a multilayered neural network [11]: (a) artificial neuron and (b) multi layer artificial network

Rosenblatt, an American psychologist, proposed the perceptron as a computer model for neurons in 1958. The introduction of digital connectivity weights was the most significant breakthrough. The model of a perceptron a neuron contains three fundamental components as shown in Figure 2 [7], [11], [27], [30].

- Synapses: which are determined by the weights' power.
- An adder is being used to add the input signals together.
- The output range is controlled using a non - linear activation.


Figure 2. Typical perceptron structure [23]

### 2.2. Binary signed digit number system

One of the number representation systems is the binary modified signed-digit (BMSD) number system. BMSD displays boundary load generation to one place on the left through the addition and subtraction operations of digital computers. The binary signed digit numbers allow the completion of the addition and subtraction operations simultaneously, regardless of the length of the numerical operands, which provides the advantage of parallelism with one execution time. In BMSD number form, the decimal number is expressed as [31], [32]:

$$
\begin{equation*}
\text { Dceimal }=\sum_{i=0}^{n-1} X_{i} r^{i} \tag{1}
\end{equation*}
$$

Where;
Dceimal: The numeral in decimal form.
$X_{i}$ : is the BMSD number's $i$-th digit serial, where $\left\{X_{i} \in\{\alpha, \ldots-1,0,1, \ldots, \alpha\}: \alpha \leq r-1\right\}$.
$r$ : is the form of BMSD number system's radix value, and in a BMSD number, $n$ is the number of digits.

### 2.3. Details three-step form algorithm

Depending on the number of steps there are three types of algorithms: one-step algorithm [33], two-step algorithm [34], and three-step algorithm [35], algorithms consisting of one and two steps have a small number of steps, but the difficulty of implementation is increased due to their dependence on previous values. The three-step algorithm is easy to implement. Assume that augends X and addend Y have BMSD representations.

$$
\begin{aligned}
& X_{\text {BMSD }}=X_{n-1},---, X_{i},---, X_{0} . \\
& Y_{\text {BMSD }}=Y_{n-1},---, Y_{i},---, Y_{0} .
\end{aligned}
$$

The following three step of summation rules as explained in Table 1, performed according to the (2), (3), and (4):

| Step-one: Calculate | $\mathrm{X}_{\mathrm{i}}+\mathrm{Y}_{\mathrm{i}}=2 \mathrm{~T}_{\mathrm{i}+1}+\mathrm{W}_{\mathrm{i}}$ | $(\mathrm{i}=0,---, \mathrm{n}-1)$ |
| :--- | :---: | :---: |
| Step-two: Compute | $\mathrm{T}_{\mathrm{i}}+\mathrm{W}_{\mathrm{i}}=2 \mathrm{~T}^{\prime}{ }_{\mathrm{i}+1}+\mathrm{W}^{\prime}{ }_{\mathrm{i}}$ | $(\mathrm{i}=0,---, \mathrm{n}-1)$ |
| Finally, Step-three: Calculate | $\mathrm{S}_{\mathrm{i}}=\mathrm{T}^{\prime}{ }_{i}+\mathrm{W}^{\prime}{ }_{\mathrm{i}}$ | $(\mathrm{i}=0,---, \mathrm{n}-1)$ |

Finally, Step-three: Calculate $\quad \mathrm{S}_{\mathrm{i}}=\mathrm{T}^{\prime}{ }_{\mathrm{i}}+\mathrm{W}^{\prime}{ }_{\mathrm{i}} \quad(\mathrm{i}=0,---, \mathrm{n}-1)$

Table 1. Three-step algorithm rules

| Inputs |  | Step one rule |  | Step two rule |  | Step three rule |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| X | Y | T (Carry) | W (Sum) | $\mathrm{T}^{\prime}$ (Carry) | $\mathrm{W}^{\prime}$ (Sum) | Final Sum (T) |
| -1 | -1 | -1 | 0 | -1 | 0 | -1 |
| -1 | 0 | -1 | 1 | 0 | -1 | -1 |
| -1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | -1 | -1 | 1 | 0 | -1 | -1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | -1 | 0 | 1 | 1 |
| 1 | -1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | -1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |

## 3. THE OFFERED ADDITION ALGORITHM STRUCTURE

### 3.1. Step one rule/T-carry transformation

The first rule is, T- carry transformation the output equal to 1 in three cases $(1+1),(1+0)$, and $(0+1)$ while it results a $(-1)$ in the following three cases $(-1+-1),(-1+0)$, and $(0+-1)$ as explained in Table 1 , those are designed by using two functions (summation and T-transformation) as shown in Figure 3. Where Fun. 1 indicates to function 1 which represent the output of T-transformation as (5).

$$
\text { Fun. } 1=\left\{\begin{array}{c}
-1, S<0  \tag{5}\\
1, S>0
\end{array}\right.
$$



Figure 3. T-transformation function

### 3.2. Step one rule/ $\mathbf{W}$-sum transformation

The first rule is / W-sum transformation the output equal to -1 in two cases $(1+0)$, and $(0+1)$ while its results a (1) in two cases $(-1+0)$, and ( $0+-1$ ) as explained in Table 1 , those are designed by using a combination of summation and delta function as shown in Figure 4. Where Fun. 2 indicates to function 2 which represent the output of W-transformation as (6).

$$
\begin{equation*}
\text { Fun. } 2=-\delta(\mathrm{S}-1)+\delta(\mathrm{S}+1) \tag{6}
\end{equation*}
$$



Figure 4. W-transformation function

### 3.3. Step two rule/T'- carry transformation

In step-two rule/T'- carry transformation the output equal to 1 in one case $(1+1)$ while its results a $(-1)$ in one case $(-1+-1)$ as explained in Table 1, those are performed by using summation and threshold function as shown in Figure 5. Where Fun. 3 indicates to function 3 which represent the output of $\mathrm{T}^{\prime \prime}$-transformation as (7).

$$
\text { Fun. } 3=\delta(S-2)+-\delta(S+2)=\left\{\begin{array}{c}
-1, S=-2  \tag{7}\\
1, S=2
\end{array}\right.
$$



Figure 5. T'-transformation function

### 3.4. Step-two rule /W'-sum transformation

In step-two rule / W'- sum transformation the output equal to 1 if two cases $(1+0)$, or $(0+1)$ while its results a ( -1 ) if the following two cases $(-1+0)$, or $(0+-1)$ as explained in Table 1, those are designed using a combination of summation and delta function as shown in Figure 6. Where Fun. 4 indicates to function 4 which represent the output of ${ }^{W}$ '-transformation as (8).

$$
\begin{equation*}
\text { Fun. } 4=\delta(\mathrm{S}-1)+-\delta(\mathrm{S}+1) \tag{8}
\end{equation*}
$$



Figure 6. W'-transformation function

### 3.5. Step-three

It includes only T-transformation that represents the final sum results. Only the difference is that its two inputs are $\mathrm{T}^{\prime}$ and $\mathrm{W}^{\prime}$ instead of X and Y . The collection of the above functions for all steps represents one basic arithmetic neural network unit (BANNU) to perform the operation of addition for one-bit of each operand X and Y , as given in Figure 7.


Figure 7. Basic arithmetic neural network unit

## 4. SIMULATION OF THREE-STEP ADDER

At the same time, the addition operations are conducted simultaneously for a set of number pairs. As a result, all processes are implemented at the same time, increasing system productivity. For simulation, we take example as the following addition operation. We consider 6 operations, each operation has two operands of 15 bits' length, the execution of operations is shown in Tables 2, 3, and 4 . The simulation for the Tables 2, 3 , and 4 three step results (step one, step two, and step three) is implemented by using visual language programming as shown in Figures 8, 9, and 10 respectively.

Table 2. Execution step one for 6 operations

| Operation no. |  | Inputs | T-transformation | W-transformation |
| :---: | :---: | :---: | :---: | :---: |
| Op. 1 | $\mathrm{a}_{1}$ | $(100-1-11010-101-10-1)_{\text {BMSD }}=(13923)_{10}$ | 0100-10111-1-10-10-10 | 00-10010-10-1110001 |
|  | $\mathrm{b}_{1}$ | $(-11010-11110-1-1-100)_{\text {BMSD }}==(-6236)_{10}$ |  |  |
| Op. 2 | $\mathrm{a}_{2}$ | $(1111111111111111)_{\text {BMSD }}=(32767)_{10}$ | 11111111111111110 | 0000000000000000000 |
|  | $\mathrm{b}_{2}$ | $(1111111111111111)_{\text {вмSD }}=(32767)_{10}$ |  |  |
| Op. 3 | $\mathrm{a}_{3}$ | $(-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1)_{\text {BMSD }}=(-32767)_{10}$ | -1-1-1-1-1-1-1-1-1-1-1-1-1- | 0000000000000000000 |
|  | $\mathrm{b}_{3}$ | $(-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1)_{\text {BMSD }}=(-32767)_{10}$ | 1-1-10 |  |
| Op. 4 | $\mathrm{a}_{4}$ | $(1111100-1-1-100111)_{\text {BMSD }}=(31527)_{10}$ | 1111111-1-1-1-1-10000 | 000000-1-111111000 |
|  | $\mathrm{b}_{4}$ | $(1111111000-1-1-1-1-1)_{\text {BMSD }}=(32481)_{10}$ |  |  |
| Op. 5 | $\mathrm{a}_{5}$ | $(11111111111111111)_{\text {BMSD }}=(32767)_{10}$ | 11111111111111110 | 0-1-1-1-1-1-1-1-1-1-1-1-1- |
|  | $\mathrm{b}_{5}$ | $(0000000000000000)_{\text {BMSD }}=(0)_{10}$ |  | 1-1-1 |
| Op. 6 | $\mathrm{a}_{6}$ | $(-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1)_{\text {BMSD }}=(-32767)_{10}$ | -1-1-1-1-1-1-1-1-1-1-1-1-1- | 0111111111111111111 |
|  | $\mathrm{b}_{6}$ | $(0000000000000000)_{\text {BMSD }}=(0)_{10}$ | 1-10 |  |

Table 3. Execution step two for 6 operations

| Operation no. | Inputs |  |  |  |
| :---: | :---: | :--- | :---: | :--- |
| 1 | $\mathrm{~T}_{1}=$ | $0100-10111-1-10-10-10$ | $\mathrm{~T}^{\prime}$-transformation | $\mathrm{W}^{\prime}$-transformation |
| 2 | $\mathrm{~W}_{1}=$ | $00-10010-10-1110001$ |  |  |
|  | $\mathrm{~T}_{2}=$ | 1111111111111110 | 000000000000000000000 | $01-10-11101001-10-11$ |
| 3 | $\mathrm{~W}_{2}=$ | 0000000000000000000 |  |  |
|  | $\mathrm{~T}_{3}=$ | $-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-10$ | 0000000000000000000 | $-1-1-1-1-1-1-1-1-1-1-1-1-1-1-10$ |
| 4 | $\mathrm{~W}_{3}=$ | 000000000000000000 |  |  |
|  | $\mathrm{~T}_{4}=$ | $1111111-1-1-1-1-10000$ | 0000000000000000000 | 111111000000100 |
| 5 | $\mathrm{~W}_{4}=$ | $000000-1-111111000$ |  |  |
|  | $\mathrm{~T}_{5}=$ | 111111111111110 | 0000000000000000000 | $1000000000000000-1$ |
| 6 | $\mathrm{~W}_{5}=$ | $0-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1$ |  |  |
|  | $\mathrm{~T}_{6}=$ | $-1-1-1-1-1-1-1-1-1-1-1-1-1-1-10$ | 0000000000000000000 | -1000000000000001 |
|  | $\mathrm{~W}_{6}=$ | 01111111111111111 |  |  |

Table 4. Execution step three for 6 operations

| Operation no. |  | Inputs | Final sum |
| :---: | :---: | :---: | :---: |
| 1 | $\mathrm{T}_{1}=$ | 0000000000000000000 | $(01-10-11100001-10-11)_{\text {BMSD }}=(7687)_{10}$ |
|  | $\mathrm{W}^{\prime}{ }_{1}=$ | 01-10-11101001-10-11 |  |
| 2 | $\mathrm{T}_{2}=$ | 0000000000000000000 | $(1111111111111110)_{\text {BMSD }}=(65534)_{10}$ |
|  | $\mathrm{W}^{\prime}{ }_{2}=$ | 11111111111111110 |  |
| 3 | $\mathrm{T}_{3}=$ | 0000000000000000000 | $(-1-1-1-1-1-1-1-1-1-1-1-1-1-1-10)_{\text {BMSD }}=(-65534)_{10}$ |
|  | $\mathrm{W}_{3}=$ | 1-1-1-1-1-1-1-1-1-1-1-1-1-1-10 |  |
| 4 | $\mathrm{T}_{4}{ }^{\prime}=$ | 0000000000000000000 | $(111111-1000001000)_{\text {BMSD }}=(64008)_{10}$ |
|  | $\mathrm{W}^{\prime}{ }_{4}=$ | 111111000000100 |  |
| 5 | $\mathrm{T}_{5}{ }^{\prime}=$ | 0000000000000000000 | $(1000000000000000-1)_{\text {BMSD }}=(32767)_{10}$ |
|  | $\mathrm{W}^{\prime}{ }_{5}=$ | 100000000000000-1 |  |
| 6 | $\mathrm{T}_{6}{ }^{\prime}=$ | 0000000000000000000 | $(-10000000000000001)_{\text {BMSD }}=(-32767)_{10}$ |
|  | $\mathrm{W}_{6}{ }^{\prime}=$ | -1000000000000001 |  |


| Step one(T) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Step one(W) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 1 | 0 | 0 | -1 | 0 | 1 | 1 | 1 | -1 | -1 | 0 | -1 | 0 | -1 | 0 | 0 | 0 | -1 | 0 | 0 | 1 | 0 | -1 | 0 | -1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | -1 | -1 | -1 | -1 | -1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -1 | -1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 |
| -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Figure 8. Simulation of step one

| Step two(T') |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Step two(W') |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -1 | 0 | -1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | -1 | 0 | -1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | -1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | -1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Figure 9. Simulation of step two


Figure 10. Simulation of step three

## 5. CONCLUSION

The application of computing in the way of using neural networks provides the advantage of parallel execution of the largest amount of data, regardless of the number of bits in each parameter for which the calculation is performed (word length), and this consumes time and gives more simplicity to the designed system and establishes a new type of computation in signed-digit number systems, from the mechism of the neural network that inspired us to perform arithmetic operations. For example, an addition where we implemented in this research a three-step algorithm, to combine two numbers using neural networks, in a new way that gave an effective system that includes choosing a suitable algorithm and a mathematical function that performs its rules in the artificial neural network. It is worth noting that in the near future, other algorithms can be implemented, one step and two steps algorithm as examples, and we can also save using trinary or quaternary numerical systems or otherwise.

## REFERENCES

[1] A. A. Al-Saffar and Q. Q. Thabit, "Simulation of Nanoscale Optical Signed Digit Addition Based on DNA-Strands," proc. of 2018 International Conference on Advanced Science and Engineering (ICOASE), 2018, Duhok, Iraq, doi: 10.1109/ICOASE.2018.8548926.
[2] B. A. Issa and I. Sabri, "High Precision Binary Coded Decimal (BCD) unit for 128-bit addition," Proc. of the 2nd International Conference on Electrical, Communication and Computer Engineering (ICECCE), 12-13 June 2020, Istanbul, Turkey, doi: 10.1109/ICECCE49384.2020.9179331.
[3] B. A. Issa, I. S. A. AL-Forati, M. A. Al-Ibadi, H. M. Amer, A. Turky Rashid, and O. T. Rashid, "Design of High Precision Radix-8 MAF Unit with Reduced Latency," 2020 International Congress on Human-Computer Interaction, Optimization and Robotic Applications (HORA), 2020, pp. 1-6, doi: 10.1109/HORA49412.2020.9152924.
[4] I. K. Kapageridis and A. G. Triantafyllou, "LavaNet-Neural network development environment in a general mine planning package, " Computers \& Geosciences, vol. 37, no. 4, pp. 634-644, April 2011, doi: 10.1016/j.cageo.2010.10.017.
[5] Y. Luo, "Recurrent neural networks for classifying relations in clinical notes," Journal of Biomedical Informatics, vol. 72, pp. 85-95, 2017, doi: 10.1016/j.jbi.2017.07.006.
[6] N. M. Ahmed and A. O. Hamdeen, "Predicting Electric Power Energy, Using Recurrent Neural Network Forecasting model," Journal of University of Human Development (JUHD), vol. 4, no. 2, pp. 53-60, 2018, doi: 10.21928/juhd.v4n2y2018.
[7] M. Forssell, "Hardware Implementation of Artificial Neural Networks," Hardware Implementation of Artificial Neural Networks, pp. 1-4, 2014, [Online]. Available: http://users.ece.cmu.edu/~pgrover/teaching/files/NeuromorphicComputing.pdf
[8] S. Yellamraju, S. Kumari, S. Girolkar, S. Chourasia, and A. D. Tete, "Design of various logic gates in neural networks," 2013 Annual IEEE India Conference (INDICON), 2013, pp. 1-5, doi: 10.1109/INDCON.2013.6725879.
[9] P. Ramesh and N. Yadaiah, "Methodology for Designing Logic Gates \& Circuits Using Mcculloch Pitts Neuron," International Journal of Electronics Engineers, vol. 8, no. 2, pp. 204-213, 2016.
[10] A. Sharma and A. Chopra, "Artificial Neural Networks: Applications in Management," IOSR Journal of Business and Management (IOSR-JBM), vol. 12, no. 5, pp. 32-40, 2013, doi: 10.9790/487X-1253240.
[11] K. Kumar and G. S. M. Thakur, "Advanced Applications of Neural Networks and Artificial Intelligence: A Review," International Journal of Information Technology and Computer Science (IJITCS), vol. 6, no. 6, pp. 57-68, 2012, doi: 10.5815/ijitcs.2012.06.08.
[12] M. Morgan, C. Blank, and R. Seetan, "Plant disease prediction using classification algorithms," IAES International Journal of Artificial Intelligence (IJ-AI), vol. 10, no. 1, pp. 257-264, March 2021, doi: 10.11591/ijai.v10.i1.pp257-264.
[13] K. Lenin, "Minimization of real power loss by enhanced teaching learning based optimization algorithm," International Journal of Robotics and Automation (IJRA), vol. 9, no. 1, pp. 1-5, March 2020, doi: 10.11591/ijra.v9i1.pp1-5.
[14] K. Kumar et al., "Soft computing and IoT based solar tracker," International Journal of Power Electronics and Drive Systems (IJPEDS), vol. 12, no. 3, pp. 1880-1889, September 2021, doi: 10.11591/ijpeds.v12.i3.pp1880-1889.
[15] A. Kurniawan and E. Shintaku, "Two-step artificial neural network to estimate the solar radiation at Java Island," International Journal of Electrical and Computer Engineering (IJECE), vol. 11, no. 4, pp. 3559-3566, August 2021, doi: 10.11591/ijece.v11i4.pp3559-3566.
[16] K. A. Smith and J. N. D. Gupta, "Neural networks in business: techniques and applications for the operations researcher," Computers \& Operations Research, vol. 27, no. 11-12, pp. 1023-1044, 2000, doi: 10.1016/S0305-0548(99)00141-0.
[17] O. Awodele and O. Jegede, "Neural Networks and Its Application in Engineering," Proceedings of Informing Science \& IT Education Conference (InSITE), 2009.
[18] R. Yang et al., "CNN-LSTM deep learning architecture for computer vision-based modal frequency detection," MechanicalSystem and Signal Processing, vol. 144, Oct. 2020, doi: 10.1016/j.ymssp.2020.106885.
[19] C. Jiang and S. Wei, "Residue-Weighted Number Conversion with Moduli Set $\left\{2^{\mathrm{p}}-1,2^{\mathrm{p}}+1,2^{2 \mathrm{p}}+1,2^{\mathrm{p}}\right\}$ Using Signed-Digit Number Arithmetic," 2010 Ninth International Symposium on Distributed Computing and Application to Business, Engineering and Science, 2010, pp. 629-633, doi: 10.1109/dcabes.2010.132.
[20] Q. A. A. Haiha, Y. Al-Zahouri, and M. Ahmed, "Efficient New design and Verification of Sign-Digit Adder for Two Symmetric Redundant Radix-4 Numbers," International Journal on Computer Science and Engineering, vol. 2, no. 4, pp. 972-978, 2010.
[21] V. Patel and K. S. Gurumurthy, "Arithmatic Operations in Multi-Valued Logic," International Journal of VLSI Design \& Communication Systems (VLSICS), vol. 1, no. 1, pp. 21-32, 2010, doi: 10.5121/vlsic.2010.1103.
[22] A. K. Cherri and H. A. Kamal, "Parallel High-Radix Negabinary Signed-Digit Arithmetic Operations: One-Step Trinary and One-Step Quaternary Addition Algorithms," Proceedings of SPIE - The International Society for Optical Engineering 2004, doi: 10.1117/12.568845.
[23] R. Rani, N. Sharma, and L. K. Singh, "Fast computing using signed digit number system," 2009 International Conference on Control, Automation, Communication and Energy Conservation, 2009, pp. 1-4.
[24] Q. Q. Thabit and A. A. Al-Saffar, "DNA-strand molecular beacon optical processor," Heliyon, vol. 5, no. 9, 2019, doi: 10.1016/j.heliyon.2019.e02389.
[25] A. M. Haidar, "A novel neural network half adder," Proceedings. 2004 International Conference on Information and Communication Technologies: From Theory to Applications, 2004, pp. 427-428, doi: 10.1109/ICTTA.2004.1307814.
[26] S. A. Alzaeemi, M. A. Mansor, M. Shareduwan, M. Kasihmuddin, S. Sathasivam, and M. Mamat, "Radial basis function neural network for 2 satisfiability programming," Indonesian Journal of Electrical Engineering and Computer Science, vol. 18, no. 1, pp. 459-469, April 2020, doi: 10.11591/ijeecs.v18.i1.pp459-469.
[27] E. S. I. and A. W. A., "Artificial Neuron Network Implementation of Boolean Logic Gates by Perceptron and Threshold Element as Neuron Output Function," International Journal of Science and Research (IJSR), vol. 4, no. 9, pp. 637-641, 2015, [Online]. Available: https://www.ijsr.net/archive/v4i9/SUB157580.pdf.
[28] S. Cotofana and S. Vassiliadis, "Signed Digit Counters with Neural Networks," CiteSeer, 1997.
[29] A. P. O. da Silva, C. R. M. Leite, L. McMillan, C. A. Paz de Araujo, M. A. C. Fernandes, and A. M. G. Guerreiro, "Adaptive Boolean Logic Using Ferroelectrics Capacitors as Basic Units of Artificial Neurons," Integrated Ferroelectrics, vol. 159, no. 1, pp. 23-33, 2015, doi: 10.1080/10584587.2015.1029408.
[30] S. Ray, M. Haque, T. Ahmed, and T. T. Nahin, "Comparison of artificial neural network (ANN) and response surface methodology (RSM) in predicting the compressive and splitting tensile strength of concrete prepared with glass waste and tin (Sn) can fiber," Journal of King Saud University-Engineering Sciences, 2021, doi: 10.1016/j.jksues.2021.03.006.
[31] R. S. Fyath, A. A. W. Alsaffar, and M. S. Alam, "Nonrecorded trinary signed-digit multiplication based on digit grouping and pixel assignment," Optics Communications (Elsevier), vol. 230, no. 1-3, pp. 35-44, 2004, doi: 10.1016/j.optcom.2003.11.038.
[32] M. S. Alam, K. Jamil, and M. A. Karim, "Optical Higher-Order Quaternary Signed-Digit Arithmetic," Optical Engineering, vol. 33, no. 10, pp. 3419-3426, 1994, doi: 10.1364/AO.31.005614
[33] M. S. Alam, "Parallel Optical Computing Using Recoded Trinary Signed-Digit Numbers," Applied Optics, vol. 33, no. 20, pp. 4392-4397, 1994, doi: 10.1364/AO.33.004392.
[34] M. S. Alam, "Efficient Trinary Signed-Digit Symbolic Arithmetic," Optics Letters, vol. 19, no. 5, pp. 353-355, 1994, doi: 10.1364/ol.19.000353.
[35] A. Awwal, M. N. Islam, and M. A. Karim, "Modified Signed-Digit Trinary Arithmetic by Using Optical Symbolic Substitution," Applied Optics, vol. 31, no. 11, pp. 1687-1694, 1992, doi: 10.1364/AO.31.001687.

