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Novel ripple reduction method using three-level inverters with unipolar PWM

Paiboon Kiatsookkanatorn[1], Napat Watjanatepin[2]
[1]Department of Electrical Engineering, Rajamangala University of Technology Suvarnabhumi, Thailand
[2]Solar Energy Research and Technology Transfer Center (SERTTC),
Rajamangala University of Technology Suvarnabhumi, Thailand

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ABSTRACT

This paper proposes a novel method to reduce voltage and current ripple for the inverters by using three-level inverters with unipolar pulse width modulation (PWM) (3LFB-2U). A simple technique of switching signal generation by using carrier-based dipolar modulation of three-phase three-level inverters is extended to single-phase inverters that can be done by generating all possible switching patterns of the single-phase three-level inverters. Moreover, the concept of carrier-based dipolar modulation and the construction of reference voltages from desired output voltage and added zero voltage to control unipolar switching is also shown. The research results reveal that the proposed method can reduce the voltage and current ripple. Furthermore, the voltage and current harmonics can reduce by 27.77% and 1.79%, respectively less than two-level inverters without a loss of a simple modulation to generate the switching signals.

Corresponding Author:

Napat Watjanatepin
Solar Energy Research and Technology Transfer Center (SERTTC)
Rajamangala University of Technology Suvarnabhumi
7/1 Nonthaburi-1, Nonthaburi, 11000, Thailand
Email: napat.w@rmutsb.ac.th

1. INTRODUCTION

Single-phase inverters have been widely applied to grid -connected inverters for low voltage and low power [1], [2]. These inverters have many requirements for grid codes [3]. The current harmonic is one of the important and interesting grid requirements. This harmonic is related directly to pulse width modulation (PWM) strategies [4]. For two-level full-bridge inverters [5], bipolar modulation is one of the modulation methods that produce the signal to drive the switch easily. However, the ripple of the voltage and current are normaly high, which causes a high harmonic voltage and a harmonic current as shown relationship in [6]. To reduce the ripple, unipolar modulation needs to be used instead. The unipolar modulation also makes the switch a unipolar switching, which reduces the ripple voltage, current, and the harmonic. However, the switching losses are high. R. Lai and K. D. T. Ngo [7], hybrid modulation is proposed to reduce switching losses but the ripple and the harmonic values remain high. Therefore, if the ripple and harmonic values are to be lowered, a large filter circuit will be required [8], [9]. This type of circuit suffers a high loss [10], [11] and the effect of inductance saturation [12].

Regarding three-level inverters, they are utilized to solve problems of two-level inverters, such as the switch voltage stress, the harmonic value, and the switching losses. The input voltage of three-level inverters stems from the capacitors connected in a series to divide the direct current (DC) bus voltage [13]-[16]. Then, the voltage drop of capacitors is only about half of the DC bus voltage. Therefore, if the switching patterns of

three-level full-bridge inverters are controlled by using unipolar switching that is no direct voltage transition from positive bus voltage to negative bus voltage, the voltage level transition of output is only half of the DC bus voltage. As a result of the decrease in the ripple output, the harmonic components will be reduced as well.

However, the modulation of three-level inverters cannot be done by directly using the modulation of two-level inverters. For this reason, recent research by [17]-[24] has developed modulation methods to single-phase three-level inverters. Several space-vector modulation (SVM) methods are presented [17]-[21] by expanding the concept of the SVM of two-level inverters with more complexity and a more sophisticated calculation. On the other hand, the carrier-based modulation methods [22]-[24] for less calculation have been proposed. The discontinuous PWM (DPWM) [22], [23] to reduce the number of switching is presented by controlling one leg is not switched as a hybrid modulation of a two-level inverter [7]. The switching losses can be reduced but the current THD is increased. To control the current THD and efficiency, a novel DPWM method [24] is proposed by combining the unipolar PWM and DPWM. However, this research is clearly shown that the current ripple and current THD during DPWM are more than unipolar PWM.

In the above sense, this paper proposes a novel method to reduce voltage and current ripple using three-level full-bridge inverters with unipolar PWM. The main contributions of this paper are as follows. First, the simple carrier-based dipolar modulation [25] with few calculations and procedures is extended to the proposed method and all possible switching patterns of three-level inverters are also shown. Then, a concept of reference voltage generation from command output voltage and added zero voltage is also applied to unipolar modulation. Finally, the performance of two-level inverters and three-level inverters are compared.

2. THE PROPOSED METHOD

2.1. Structure and basic equations of carrier-based dipolar modulation

Three-level inverters are similar to two-level inverters in that they require a direct current supply. However, three-level inverters use three-levels of direct voltage from two capacitors that are connected in a series to divide half of the bus voltage. The equivalent circuits of three-level inverters are shown in Figure 1, where the three-level input bus voltage is obtained from the positive bus voltage v_P, the center bus voltage v_0, and the negative bus voltage v_N. The relationships between the voltages of the input and output sides for half-bridge inverters can be described by (1) and (2).

$$v_o = v_o^* + v_Z = [m_{11} \quad m_{12} \quad m_{13}] \begin{bmatrix} v_P \\ v_0 \\ v_N \end{bmatrix} \tag{1}$$

$$m_{11} + m_{12} + m_{13} = 1 \tag{2}$$

Where, v_o^* and v_o are command and output voltage respectively. v_Z is zero-sequence voltage. m_{11} and m_{12} are duty cycles of three-level half-bridge inverters.

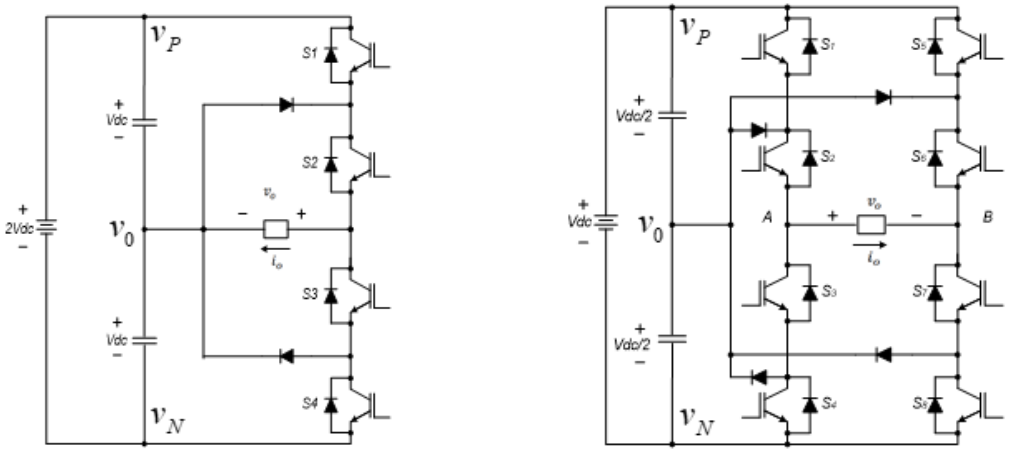


Figure 1. Structure of single-phase three-level inverter; (a) half-bridge and (b) full-bridge

Figure 1 (a) shows a single-phase three-level half-bridge inverter scheme of which the output voltage is directly related to the current flow of the four switches. If switches S_1 and S_2conduct the current, the output voltage will connect to the input positive bus voltage v_P. Then, if switches S_2 or S_3 conduct the current, the output voltage will connect to the center bus voltage v_0. Finally, if switches S_3 and S_4 conduct the current, the output voltage will connect to the input negative bus voltage v_N. A relationship between the output voltage and switching states is shown in Table 1.

Table 1. A relationship between output voltages and switching states for half-bridge inverters

DC bus voltage	Output voltage v_o	S_1	S_2	S_3	S_4	i_o
v_P	+Vdc	On	On	Off	Off	>0
v_0	0	Off	On	Off	Off	>0
v_0	0	Off	Off	On	Off	<0
v_N	-Vdc	Off	Off	On	On	<0

2.2. Concept of carrier-based dipolar modulation

According to Figure 1, the scheme of the single-phase three-level inverters can be easily rewritten, as shown in Figure 2, which now has three-level t-type neutral point clamped (3L-TNPC) switches that support the configuration in [26]. The carrier-based modulation technique of three-level inverters is different from that of two-level inverters at which two sets of the carrier wave and reference voltage are compared [27] and is called carrier-based dipolar modulation. The concept of this modulation is extended to generate the switching signals for three-phase three-level inverters [28]-[30].

Although the modulation method to generate a signal that drives the switches for three-level inverters is more complex than that of two-level inverters, using a carrier-based dipolar modulation can reduce the complexity. This modulation technique that generates the signal to drive the switches infers the relationship in generating the reference voltages u_P^*, u_N^* from command voltage v_o^* , which can be shown in (3).

$$v_o^* = u_P^* + u_N^* \tag{3}$$

$$v_Z = v_{ZP} + v_{ZN} = 0 \tag{4}$$

$$v_o = v_o^* + v_Z = \underbrace{(u_P^* + v_{ZP})}_{u_P} + \underbrace{(u_N^* + v_{ZN})}_{u_N} \tag{5}$$

Where, u_P^*, u_N^* are positive and negative command voltages, u_P, u_N are positive and negative references and v_{ZP}, v_{ZN} are positive and negative zero-sequence voltages. Generally, the carrier wave and the reference signal are equal to one unit. In this paper, on the other hand, the maximum and minimum values of carrier wave used to describe the modulation concept depend on the input voltage or DC bus voltage and the value of reference signal is upon the desired output voltage, as demonstrated in Figure 3.

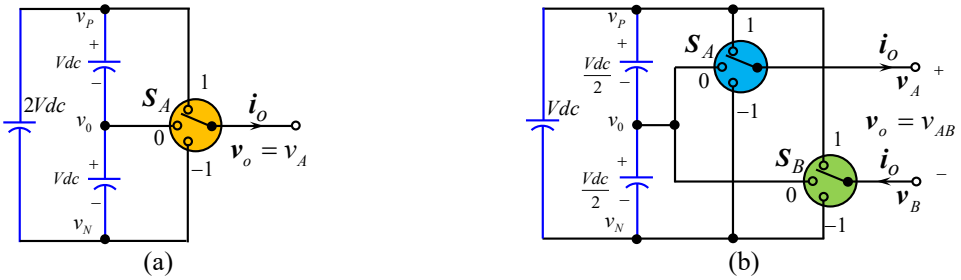


Figure 2. Simplified structure of single-phase three-level inverter; (a) half-bridge and (b) full-bridge

Research [25] proposed the concept of carrier-based dipolar modulation from the commanded voltage for three-phase three-level inverters. This can be applied to single-phase inverters. The steps are as follows. First, the commanded output voltage, as shown in Figure 3 (a), is divided into two parts: positive voltage command u_P^* , which is built from the positive bus, and the negative voltage command u_N^*, which is built from the negative bus, as shown in Figure 3 (b). Then, the positive zero-sequence voltage v_{ZP} and positive voltage command u_P^* are added and the positive reference voltage u_P is moved up or down to the desired position.

Besides, the negative voltage command u_N^* and the appropriate positive zero-sequence voltage v_{ZN}, are added at which the values are independent and the reference voltage u_N is moved to the desired position. However, in the case of a half-bridge scheme, v_{ZP} and v_{ZN} are directly related. If v_{ZP} is decreased, the v_{ZN} is also decreased and v_Z must be equal to zero, as shown in Figure 3 (c) or Figure 3 (d). After that, the reference voltages u_P and u_N in Figure 3 (d) are normalized. Then U_P, U_N which are used to compare to the carrier-based dipolar, can be obtained as shown in Figure 3 (e). Finally, the different modulation schemes on U_P, U_N as shown in Figure 4.

Figure 4 describes the carrier-based dipolar modulation for three-level inverters. As seen in the above figure, the different addition of zero voltage v_{ZP}, v_{ZN} gives PWM mode for each leg as follows: dipolar switching (d), unipolar switching (u), bipolar switching (b), and non-switching (n) that cover all possible switching patterns of three-level inverters. Here, an integer and letters "d" "u" "b" or "n" are used to represent a PWM mode. For example, <1u1d> PWM means that one leg is in unipolar mode and one leg is in dipolar mode.

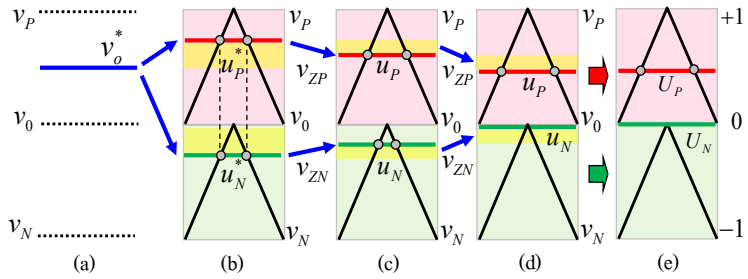


Figure 3. Concept of carrier-based dipolar modulation; (a) commanded voltage, (b) positive and negative voltage commands, (c) reference voltages, (d) reference voltages for unipolar mode, and (e) reference signals

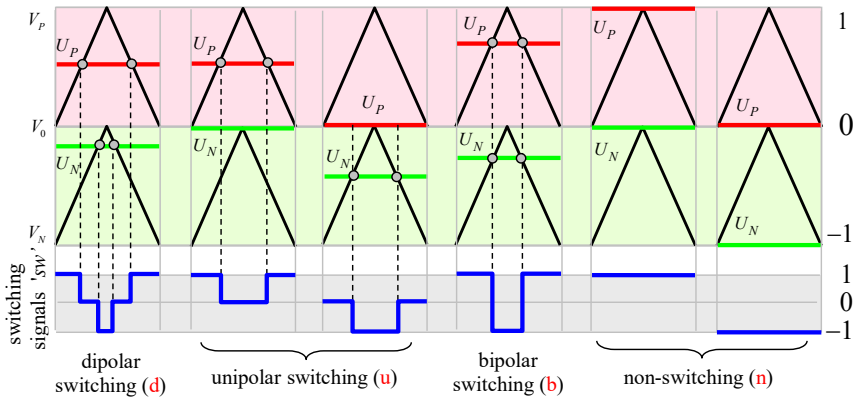


Figure 4. PWM mode for three-level inverters [25]

3. THE RESEARCH METHOD

From Figure 2 (b), the relationship between the output voltage and switching states is shown in Table 2. And the relationship between the output voltage and input voltage can be described by (6) and (7).

$$\begin{bmatrix} v_A \\ v_B \end{bmatrix} = \begin{bmatrix} v_A^* + v_Z \\ v_B^* + v_Z \end{bmatrix} = \underbrace{\begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \end{bmatrix}}_{M} \begin{bmatrix} v_P \\ v_0 \\ v_N \end{bmatrix} \tag{6}$$

$$0 \le m_{ij} \le 1, \; i = \{1,2\}, j = \{1,2,3\} \; \textstyle\sum_{j=1}^{3} m_{ij} = 1, \tag{7}$$

The carrier-based modulation method for full-bridge inverters differs from half-bridge inverters, as shown in Figures 2 (a) and (b) respectively, by adding zero voltage v_Z the same as the three-phase inverters because the output voltage of full-bridge inverters is different for A-leg and B-leg voltages, as shown in (8).

$$v_o^* = v_{AB}^* = v_A^* - v_B^* \tag{8}$$

Where,

$$v_A^* = -v_B^*$$

and

$$v_o = v_{AB} = (v_A^* + v_z) - (v_B^* + v_z) \tag{9}$$

resulting in

$$\left.\begin{aligned} v_A^* + v_z &= (u_{AP}^* + v_{ZP}) + (u_{AN}^* + v_{ZN}) \\ v_B^* + v_z &= (u_{BP}^* + v_{ZP}) + (u_{BN}^* + v_{ZN}) \end{aligned}\right\} \tag{10}$$

Here, v_{AB}^*, v_{AB} are command and output voltage between A-leg and B-leg. v_A^*, v_A are command and output A-leg voltage and v_B^*, v_B are command and output B-leg voltage. u_{AP}^*, u_{BP}^* are positive output voltage commands A-leg and B-leg. u_{AN}^*, u_{BN}^* are negative output voltage commands A-leg and B-leg. $u_{AP,}u_{BP}$ and $u_{AN,}u_{BN}$ are positive and negative output voltages A-leg and B-leg, respectively.

Table 2. A relationship between output voltages and switching states for full-bridge inverters

Modes	1	2	3	4	5	6	7	8	9
S_A	1	1	1	0	0	0	-1	-1	-1
S_B	1	0	-1	1	0	-1	1	0	-1
v_{A0}	v_P	v_P	v_P	v_0	v_0	v_0	v_N	v_N	v_N
v_{B0}	v_P	v_0	v_N	v_P	v_0	v_N	v_P	v_0	v_N
v_{AB}	0	$V_{dc}/2$	V_{dc}	$-V_{dc}/2$	0	$V_{dc}/2$	$-V_{dc}$	$-V_{dc}/2$	0

Figure 5 shows carrier-based dipolar modulation for full-bridge three-level inverters. In this case, commanded voltages consist of A-leg voltage v_A^* and B-leg voltage v_B^* that are out of phase 180 degrees, as shown in Figure 5 (a). In the double carrier-based dipolar modulation, commanded voltages in each leg are divided into two parts: positive A-leg voltage command u_{AP}^* and negative A-leg voltage command u_{AN}^*. For the B-leg case they are the same as A-leg, as shown in Figure 5 (b). Then, these positive and negative voltage commands are added by the appropriate positive and negative zero voltages v_{ZP} and v_{ZN}. As a result, reference voltages u_P and u_N are moved to the desired position, as shown in Figure 5 (c) or Figure 5 (d). Figure 5 (c) is <1n1b> PWM while Figure 5 (d) is <2u> PWM. For full-bridge inverters, adding zero voltages v_{ZP} and v_{ZN} are independent and differ from half-bridge inverters. Finally, the reference signals $[U_P]$ and $[U_N]$ are obtained by normalizing u_P and u_N in Figure 5 (d) with DC bus voltage, as shown in Figure 5 (e). This concept is the novel carrier-based modulation method for single-phase three-level inverters.

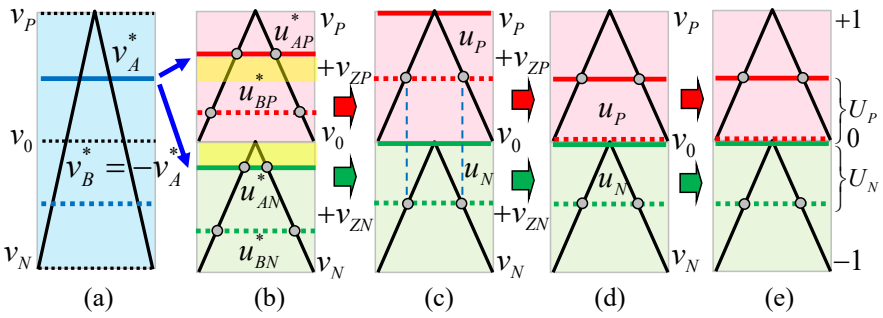


Figure 5. Carrier-based dipolar modulation for full-bridge three-level inverters; (a) commanded voltages, (b) <2d> PWM, (c) <1n1b> PWM, (d) <2u> PWM, and (e) reference signals for <2u> PWM

According to the general equation of modulation M for full-bridge inverters in (6), the function of zero voltage modulation can be separated as (11).

$$M = M' + M_0 = \underbrace{\begin{bmatrix} m'_{11} & m'_{12} & m'_{13} \\ m'_{21} & m'_{22} & m'_{23} \end{bmatrix}}_{[M']} + \underbrace{\begin{bmatrix} X & Y & Z \\ X & Y & Z \end{bmatrix}}_{[M_0]} \quad (11)$$

Where,

$$[M'] = \frac{1}{v_P^2 + v_0^2 + v_N^2} \begin{bmatrix} v_A^* \\ v_B^* \end{bmatrix} [v_P \quad v_0 \quad v_N]$$

when the general equation of modulation function M from (6) is replaced by another (11). In this case, (6) then becomes (12).

$$\begin{bmatrix} v_A \\ v_B \end{bmatrix} = \begin{bmatrix} v_A^* + v_Z \\ v_B^* + v_Z \end{bmatrix} = \begin{bmatrix} m'_{11} + X \\ m'_{21} + X \end{bmatrix} v_P + \begin{bmatrix} m'_{12} + Y \\ m'_{22} + Y \end{bmatrix} v_0 + \begin{bmatrix} m'_{13} + Z \\ m'_{23} + Z \end{bmatrix} v_N \quad (12)$$

The output voltage and input voltage are compared to the middle point of DC bus voltage and the results are shown as (13).

$$\begin{bmatrix} v_A - v_0 \\ v_B - v_0 \end{bmatrix} \triangleq \underbrace{\begin{bmatrix} m'_{11} + X \\ m'_{21} + X \end{bmatrix} (v_P - v_0)}_{u_P} + \underbrace{\begin{bmatrix} m'_{13} + Z \\ m'_{23} + Z \end{bmatrix} (v_N - v_0)}_{u_N} \quad (13)$$

and the zero voltage v_{ZP}, v_{ZN} in (10) is derived from

$$v_{ZP} = X[v_P - v_0], v_{ZN} = -Z[v_0 - v_N] \quad (14)$$

From (11) the allowable range of zero voltages M_0 are given by (15).

$$\left.\begin{array}{l} -min(m'_{11}, m'_{21}) \le X \le 1 - max(m'_{11}, m'_{21}) \\ -min(m'_{12}, m'_{22}) \le Y \le 1 - max(m'_{12}, m'_{22}) \\ -min(m'_{13}, m'_{23}) \le Z \le 1 - max(m'_{13}, m'_{23}) \\ X + Y + Z = 1 \end{array}\right\} \quad (15)$$

According to Figure 4, it can be seen that unipolar switching gives low voltage level transition. In this paper, the minimum values of X, Z are chosen to make a <2u>PWM true as represented in (16).

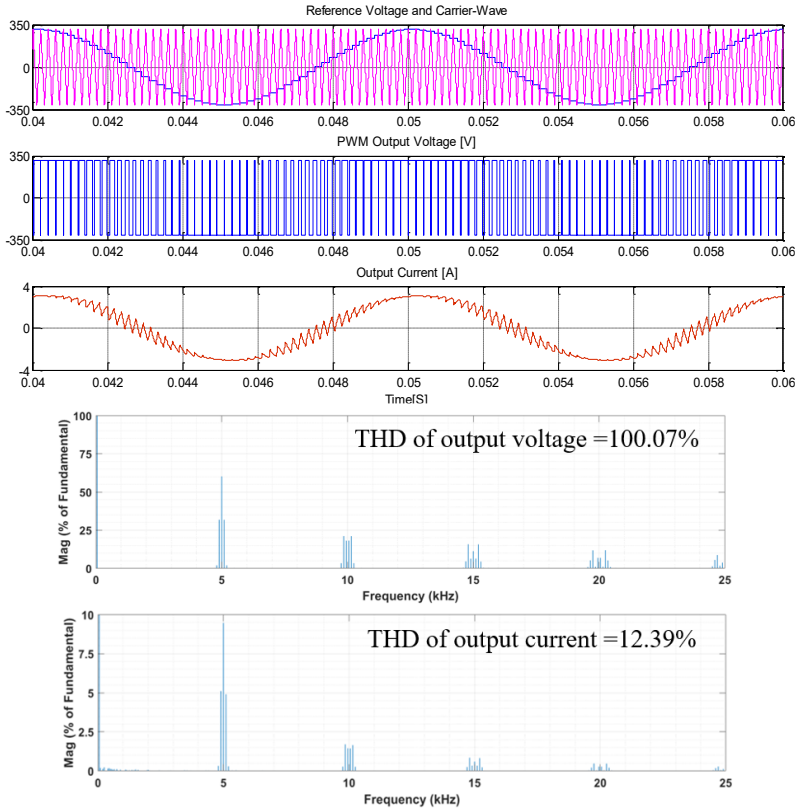
$$\left.\begin{array}{l} X = -min(m'_{11}, m'_{21}) \\ Z = -min(m'_{12}, m'_{22}) \end{array}\right\} \quad (16)$$

4. RESULTS AND DISCUSSION

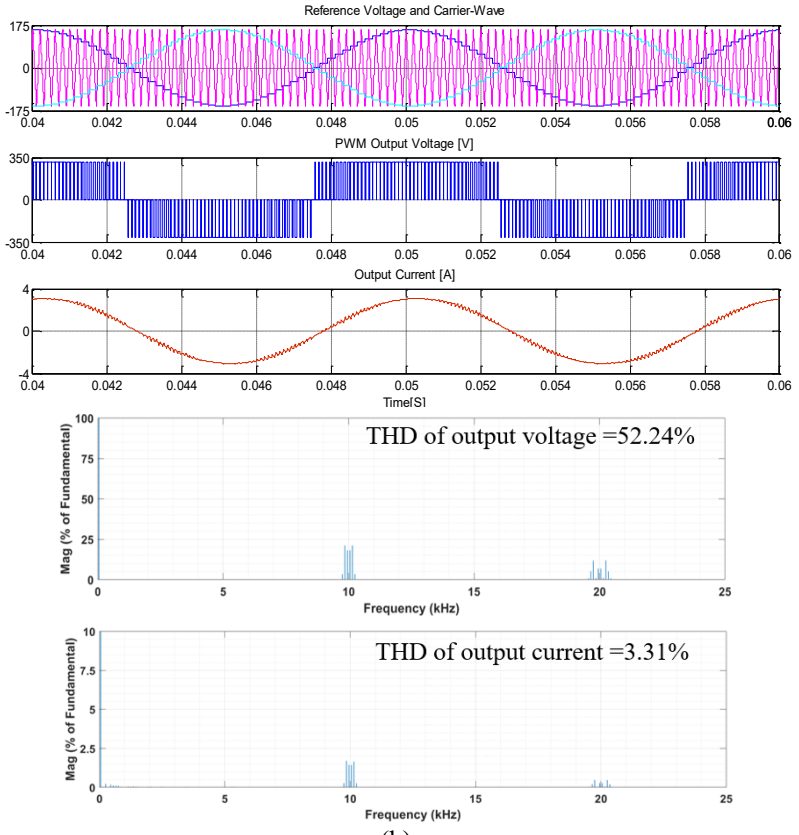
Simulation is carried out to compare and analyze the output current and voltage ripple for single-phase inverters. Simulation conditions are shown in Table 3. Figures 6 and 7 show the results of two-level inverters and Figures 8 and 9 show the results of three-level inverters by using the proposed carrier-based modulation. From the above three modulations, Figures 6 (a) and 6 (b) are bipolar and unipolar modulations, respectively that give THD of voltage according to [5] and Figure 6 (c) is hybrid modulation accoding to report of [7]. A comparison of the output current ripple of each modulation is shown in Figure 7. From Figure 7, it is indicated that the the two-level inverters have high values in both the ripple voltage and ripple current. Though the method of modulation is chosen appropriately, the two-level inverter scheme can only produce the lowest voltage to Vdc. Thus, to achieve a lower voltage than Vdc, the three-level inverter scheme needs to be implemented.

Table 3. Simulation conditions

Parameters	Value	Parameters	Value
DC Bus Voltage	$\sqrt{2}$*220 V	Load	$R = 100\Omega, L = 20mH$
Output Voltage	220V, 50Hz	Switching Frequency	5 kHz

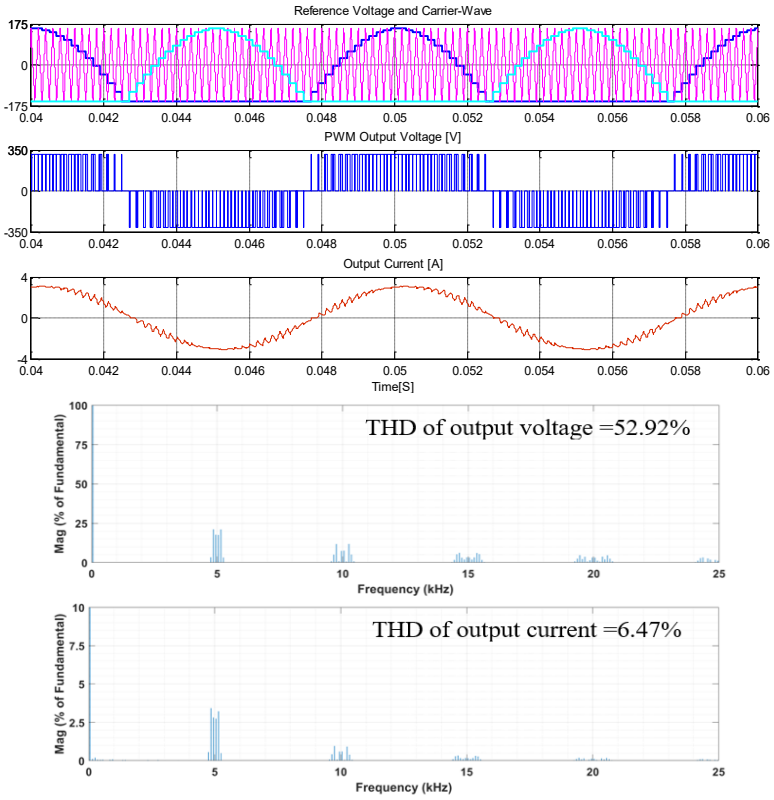


(a)



(b)

Figure 6. Voltage and current waveforms and spectrums for two-level full-bridge inverters; (a) bipolar modulation (2LFB-B) and (b) unipolar modulation (2LFB-U)



(c)

Figure 6. Voltage and current waveforms and spectrums for two-level full-bridge inverters; (c) hybrid modulation (2LFB-H) (continue)

Figure 8 (a) illustrates the unipolar modulation for a three-level half-bridge inverter. In this modulation, the positive voltage generates the positive bus while the negative voltage generates the negative bus, which has no direct transition from positive bus to negative bus. In addition, this modulation requires only two switching times <1u> PWM. Compared to Figure 7 (c), the output voltage and the current waveform, including the voltage spectrum, have similar characteristics. Therefore, this modulation can be used to replace a two-level inverter with a hybrid modulation. Figure 8 (b) describes the unipolar modulation of two legs (<2u> PWM) for a three-level full-bridge inverter and indicates the change of the output voltage level is minimized to Vdc/2 only. As a result, the changes of dv/dt are also minimized to half in the case of half-bridge configuration. Hence, the output ripple voltage that can be observed through the sine wave output is significantly reduced. The output current ripple can be compared with the case of a half-bridge, as shown in Figure 9.

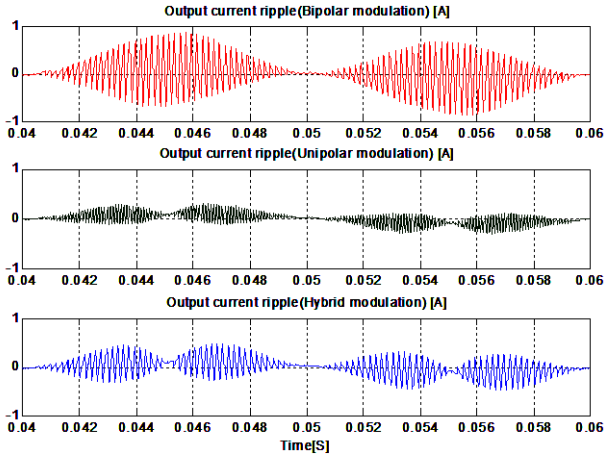
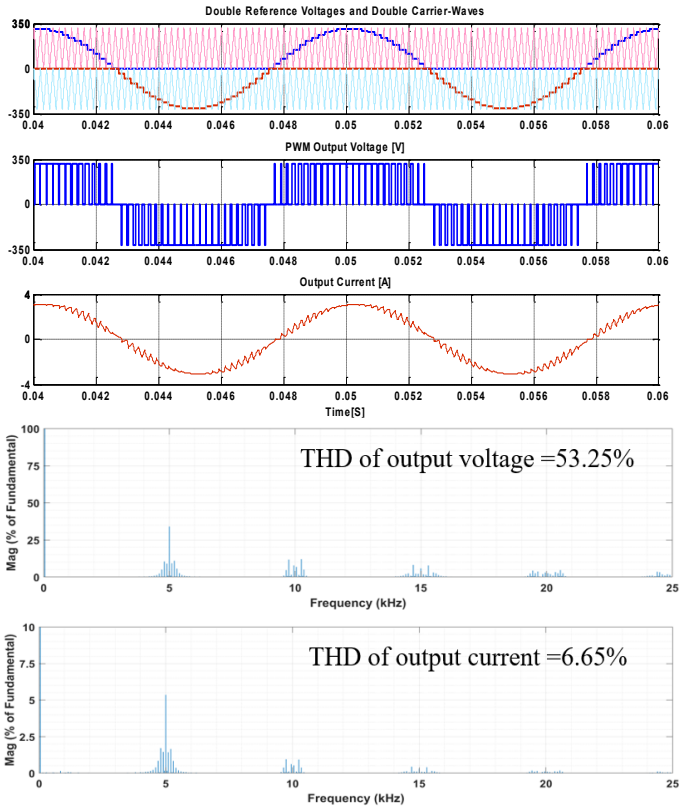
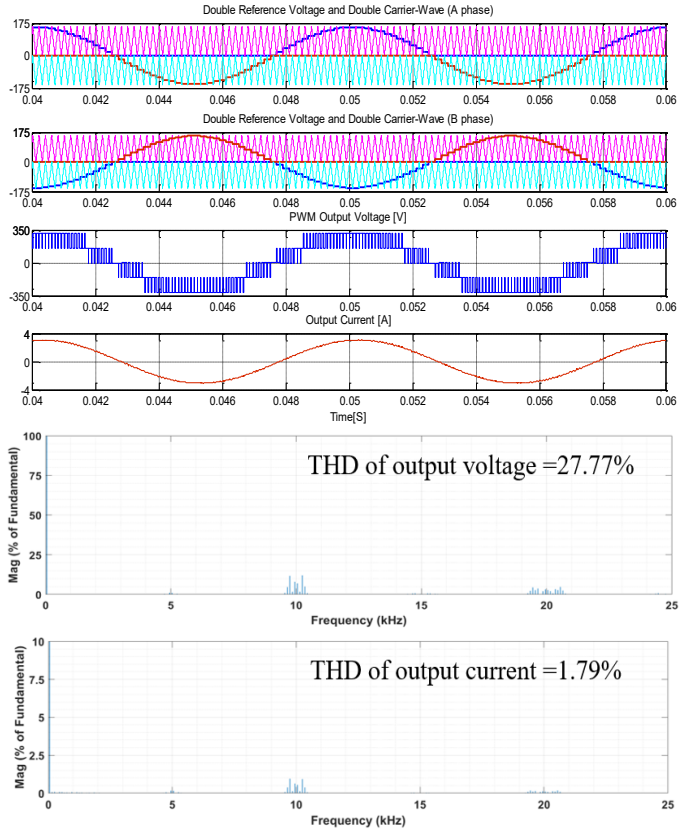


Figure 7. The output current ripple of two-level inverters



(a)



(b)

Figure 8. Voltage and current waveforms and spectrums for three-level inverter with a carrier-based dipolar modulation to unipolar switching; (a) half-bridge (3LHB-U) and (b) full-bridge (3LFB-2U)

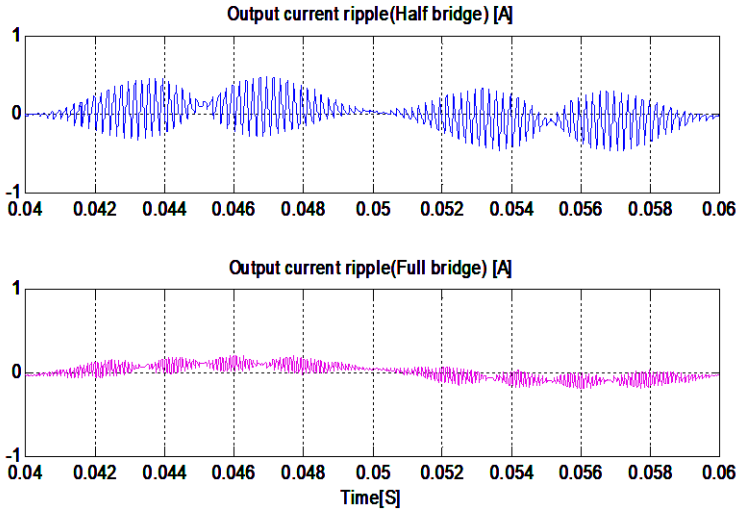


Figure 9. The output current ripple of three-level inverters

It is shown in Figure 9 that the output current ripple of three-level full-bridge inverters is very low. It is confirmed that the viewpoint of the proposed three-level inverter to reduce ripple is realized and using carrier-based dipolar modulation to generate the switching signals for the three-level inverter is simple. This is similar to the modulation process of the two-level inverters. Furthermore, this dipolar modulation technique can also generate bipolar and dipolar switchings. Hence, the switching patterns have freedom except for the unipolar switching. For this reason, future studies will use this modulation to reduce the current ripple in DC link capacitors too.

From the presented guidelines, the characteristics of single-phase inverters can be compared, as shown in Table 4. It is shown that the voltage level transition of a two-level inverter with bipolar modulation (2LFB-B) is high to 2Vdc and it can be reduced to Vdc when modulation is replaced by unipolar modulation (2LFB-U). The output voltage frequency of this modulation is increased twice the switching frequency. As the result, the current ripple is reduced but the switching losses are high. The switching losses can be decreased by using hybrid modulation (2LFB-H) because this modulation will give the output voltage frequency reducing to the switching frequency. However, the change of output voltage frequency makes the current ripple to be high. On the other hand, three-level inverter utilization to reduce the current ripple controlling the low voltage level transition by choosing the unipolar modulation but the characteristics in Table 3 indicated that three-level half-bridge inverters (3LHB-U) are like 2LFB-H. The voltage level transition of both is Vdc so if we want to have the only Vdc/2, the three-level inverter changes from half-bridge to full-bridge and still unipolar modulation (3LFB-2U). This modulation gives the output voltage frequency twice the switching frequency as 2LFB-U but the current ripple of 3LFB-2U is lower. Because of the low voltage level transition, the voltage stress of switches is low too. Although the number of switchings in a period is four, switching losses are still low. Furthermore, 3LFB-2U also gives low total harmonics distortion of voltage and current by 27.77% and 1.79%, respectively. Therefore, it can be confirmed that voltage level transition significantly affects the performance of inverters. The factors on low voltage level transition come from the inverter structure and proper PWM mode. Thus, it can be concluded that the proposed inverters have been a high performance that can be able to apply the grid-connected inverters for the photovoltaic system.

Table 4. Characteristics of two-level and three-level inverters

Features	2LFB-B[5]	2LFB-U[5]	2LFB-H[7]	3LHB-U	3LFB-2U
PWM mode	<2b>	<2b>	<1n1b>	<1u>	<2u>
Voltage level transition	2Vdc	Vdc	Vdc	Vdc	Vdc/2
Maximum of current ripple peak-to-peak value (A)	1.52	0.45	0.72	0.73	0.23
PWM output voltage	fs	2fs	fs	fs	2fs
Switching number / Ts	4	4	2	2	4
Switch voltage stress	Vdc	Vdc	Vdc	Vdc	Vdc/2
Switching losses	Fair	Fair	Low	Low	Low
%THDv	100.07	52.24	52.92	53.25	27.77
%THDi	12.39	3.31	6.47	6.65	1.79

5. CONCLUSION

This paper proposes a novel method to reduce output ripple for the single-phase inverters by using three-level inverters in combination with unipolar modulation. We applied a carrier-based dipolar modulation of three-phase inverters to single-phase inverters by expanding the concept of modulation command voltage as a reference voltage as the same as in two-level inverters. Thus, the generation of the switching signals can be simplified. The simulation results show that the three-level half-bridge inverters with unipolar modulation (3LHB-U) have the same performance at the same level as two-level full-bridge inverters with hybrid modulation (2LFB-H). Therefore, the concept of ripple reduction in single-phase inverters can be realized by using three-level full-bridge inverters (3LFB-2U), which provide very low levels of change in dv/dt. Hence, the change of voltage is not only minimized to Vdc/2, but the waveform is also closer to the sine wave. As a result, the harmonic voltages and the harmonic currents are at a lowered level and the stress voltage at the switch is minimized to Vdc/2. Moreover, the switching losses are also low because the voltage across power devices is half of the DC bus voltage. Comparing with unipolar modulation methods, this proposed modulation method can utilize the bipolar and dipolar switchings which are maybe necessary to reduce the current ripple in DC link capacitors.

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