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Prediction of a New Cascaded Hybrid Multilevel Inverter with Less Device Count

C.R.Balamurugan*, S.P.Natarajan, R.Bensraj
Arunai Engineering College, Tiruvannamalai, India
*Corresponding author, e-mail: crbalain2010@gmail.com

Abstract

Multilevel inverters have been opted for high power applications due to reduced harmonic distortion, less device voltage stress and modular structure. This work proposes new modified hybrid H-bridge multilevel inverter using auxiliary switch. This proposed inverter produces five levels output with five power devices and clamping diodes as a phase voltage and nine levels as a line voltage.The levels of the inverters are decided based on the phase voltage not on the line voltage. In this paper the performance of the proposed inverter are measured in terms of line voltage. However, by increase in the number of levels the proposed inverter with reduced number of switches produces low switching losses and improves the efficiency of the inverter. This method achieves the variation of Total Harmonic Distortion (THD) in the inverter and output voltage is observed for various modulation indices. Simulation is performed using MATLAB-SIMULINK for line to line output voltage. Variable Amplitude Phase Disposition (VAPD) strategy provides output with relatively low distortion for all the strategies. It is also seen that VAPOD is found to perform better for all strategies since it provides relatively higher fundamental RMS output voltage.

Keywords*: THD, PWM, CF, FF, Line voltage.*

1. Introduction

Multilevel converters offer a number of advantages when compared to the conventional two level converter counterpart. Gerardo Ceglia et al [1] have discussed a new multilevel inverter topology. Caballero et al [2] presented new a symmetrical hybrid multilevel voltage inverter. Khoucha et al [3] proposed a comparison of symmetrical and asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives. Roshankumar et al [4] described a five-level inverter topology with single-dc supply by cascading a flying capacitor inverter and an h-bridge. Bayat and Babaei [5] presented a new cascaded multilevel inverter with reduced number of switches. Topology for multilevel inverters to attain maximum number of levels from given dc sources have been discussed by Gupta and Jain [6]. Rahila et al [7] introduced a new 81 level inverter with reduced number of switches. Minimization applied directly on the line-to-line voltage of multilevel inverters proposed by Yousefpoor et al [8]. Chavarría et al [9] deals Energy-Balance Control of PV Cascaded Multilevel. Kangarlu and Babaei [10] have been proposed a generalized cascaded multilevel inverter using series connection of submultilevel inverters. Balamurugan et al [11] proposed a new modified H-bridge multilevel inverter using less number of switches. Younghoon Cho et al [12] developed a carrier-based neutral voltage modulation strategy for multilevel cascaded inverters under unbalanced dc sources. Murali et al [13] made a design and analysis of voltage source inverter for renewable energy applications. Jamaludin et al [14] proposed a multilevel voltage source inverter with optimized usage of bidirectional switches. Gabriel et al [15] introduced a five-level multiple-pole PWM AC – AC converters with reduced components count. Lim et al [16] suggested a modular-cell inverter employing reduced flying capacitors with hybrid phase-shifted. Rasilo et al [17] proposed a effect on multilevel inverter supply on core losses in magnetic materials and electrical machine. Reddy et al [18] developed a embedded control for a n -Level DC – DC – AC Inverter.

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2. Toplogy and Operation

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high frequency waveform in positive and negative polarities. The chosen five level modified cascaded Hybrid H-bridge multilevel inverter with less number of switches is shown in Figure 1. One switching element and four diodes added in the conventional full-bridge inverter are connected to the center-tap of dc power supply. Proper switching control of the auxiliary switch can generate half level of dc supply voltage. Table I shows the switching states and possible output voltages of the converter.

3. The Proposed Multilevel Inverter

This topology requires less number of components compared to conventional topologies. It is also more efficient which leads to simpler and more reliable control of the inverter. To provide a large number of output levels without increasing the number of bridges, a new modified cascaded hybrid H-bridge symmetrical multilevel converter is proposed in this paper. Table 1 shows the possible switching states of the proposed inverter. Table 2 displays the comparison between conventional and proposed multilevel inverter.

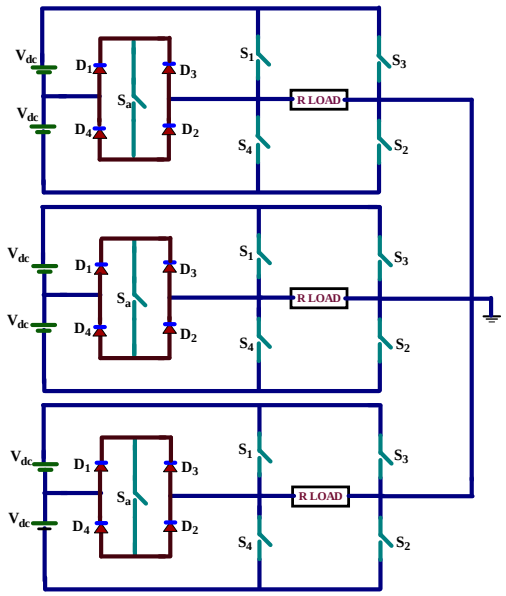

Figure 1. Schematic of chosen three phase, five level modified cascaded hybrid H-bridge inverter

Table 1. Voltage ouput and switching states

Vphase a	S_a	S_1	S_2	S_3	S_4
$2V_{dc}$	0	1	1	0	0
V_{dc}	1	0	0	0	0
0	0	0	0	0	1
$-V_{dc}$	1	0	1	0	0
$-2V_{dc}$	0	0	0	1	1

Table 2. Comparison between existing system and proposed system

Type	Conventional CMLI	Chosen hybrid H-bridge cascaded inverter
No. of switches	24	15
No. of clamping diodes	24	15
No. of DC sources	6	6

4. Modulation Schemes

The advent of the multilevel inverter topology has brought forth various Pulse Width Modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the inverter. More number of modulation strategies possible for multilevel inverters. The most efficient method is pulse width modulation schemes used to control the switching of the active devices in each of the multiple voltage levels in the inverter. In this method, a fixed D.C. input voltage is supplied to the inverter and a controlled A.C. output voltage is obtained by adjusting the on and–off periods of the inverter devices. Voltage-type PWM inverters have been applied widely to such fields as power supplies and motor drivers. This is because such inverters are well adapted to high-speed self turn-off switching devices that, as solid-state power converters, are provided with recently developed advanced circuits. The SPWM aims at generating a sinusoidal inverter output voltage without low-order harmonics. This is possible if the sampling frequency is high compared to the fundamental output frequency of the inverter. In this paper multicarrier modulation techniques with sine reference are presented. Number of triangular wave is compared with a controlled sinusoidal modulating signal. The number of carriers required to produce the m level output is m-1. Multiple degrees of freedom are available in carrier based multilevel PWM. The principle of the carrier based PWM strategy is to use m-1 carriers with a reference signal for a m level inverter. This paper focuses on six SPWM strategies. They are: PDPWM, VAPDPWM, PODPWM, VAPODPWM, VFPWM and VAVFPWM.

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4.1. Phase Disposition (PD)

In this method uses four carriers, all these carriers have the same amplitude, frequency, and phase. Since all carriers are selected with the same phase. All carriers are having amplitude as 1. The PD PWM signal generation for modulation index m_a = 0.8 is shown in Figure 2.

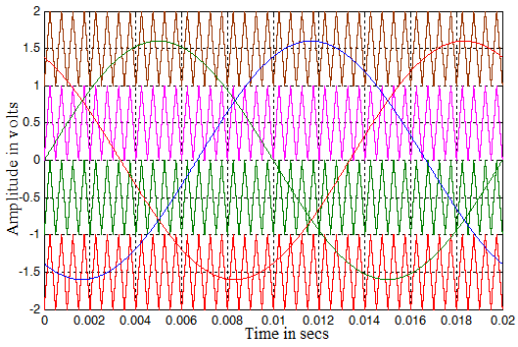

Figure 2. Modulating and carrier waveforms for PDPWM strategy (m_a = 0.8 and m_f = 40)

4.2. Variable Amplitude Phase Disposition (VAPD)

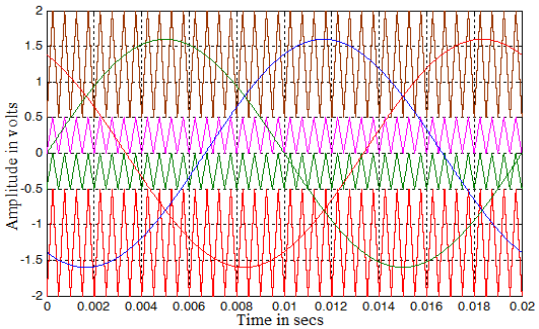

Figure 3. Modulating and carrier waveforms for PDPWM strategy (m_a = 0.8 and m_f = 40)

This method is same as PDPWM but amplitude arrangement is somewhat different. The sinusoidal reference wave is placed at the middle of the four carriers. The VAPD PWM signal generation for modulation index m_a = 0.8 is shown in Figure 3.

4.3. Phase Opposition Disposition (POD)

This method is same as PDPWM but carrier arrangement should be different. In this method uses two groups of carriers that is positive group and negative group carriers. In this type the two groups are opposite in phase with each other. It can generate five level output. The PODPWM signal generation for m_a = 0.8 is shown in Figure 4.

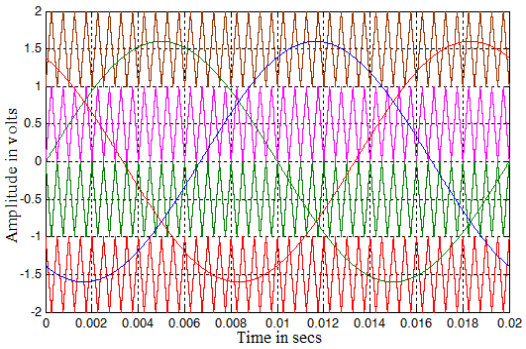

Figure 4. Modulating and carrier waveforms for PODPWM strategy (m_a = 0.8 and m_f = 40)

4.4. Variable Amplitude POD (VAPOD)

The VAPODPWM signal generation for m_a = 0.8 is shown in Figure 5. In this method all carriers phase shifted by 180 degree. All these carriers have the, frequency, and phase but different amplitude.

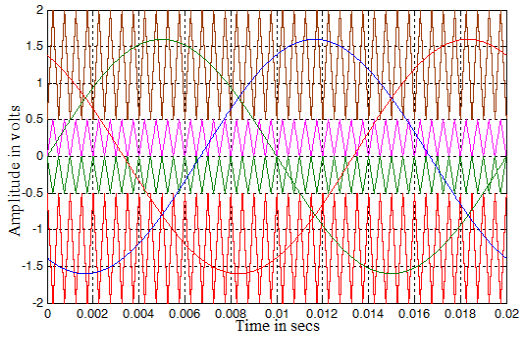

Figure 5. Modulating and carrier waveforms for VAPODPWM strategy (m_a = 0.8 and m_f = 40)

4.5. Variable Frequency (VF)

This method is one of the PWM techniques and it is same as PDPWM but intermittent carrier having different frequency compare to upper and lower carrier. The VFPWM signal generation for m_a = 0.8 is shown in Figure 6.

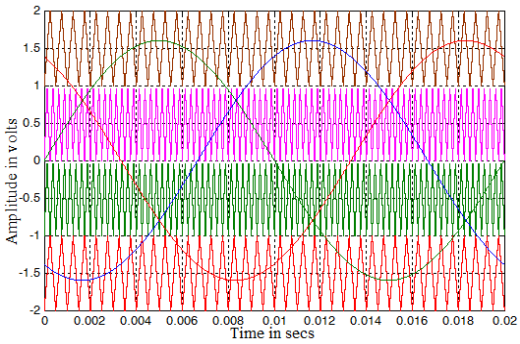

Figure 6. Modulating and carrier waveforms for VFPWM strategy
(m_a = 0.8 and m_f = 40 for lower and upper switches and m_a = 0.8 and m_f = 80 for intermediate switches)

4.6. Variable Amplitude VF (VAVF)

In this method similar to VF but carrier amplitude of carrier is different. It can generate five level output. Since all carriers are selected with the same phase, the method is known as VAVF strategy. The VAVFPWM signal generation for m_a = 0.8 is shown in Figure 7.

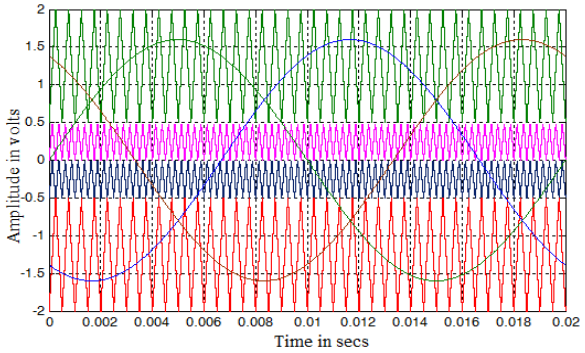

Figure 7. Modulating and carrier waveforms for VAVFPWM strategy (m_a = 0.8 and m_f = 40)

5. Simulation Results

The chosen five level inverter is modeled in MATLAB-SIMULINK to verify the proposed PWM strategies for chosen three phase Hybrid H- bridge type cascade five level inverter for various values of m_a ranging from 0.6 – 1 and corresponding %THD values line voltage are measured using FFT block and they are shown in Table 3. Table 4 shows the V_{RMS} of fundamental of inverter output for the same modulation indices. Table 5, 6 and 7 show form factor, crest factor and distortion factors. Figure 8-19 show the simulated output voltage of chosen hybrid H-bridge cascaded inverter and the corresponding FFT plots with different PWM strategies but only for one sample value of m_a=0.8 and m_f=40. Figure 8 shows the five level output voltage generated by PDPWM strategy and its FFT plot is shown in Figure 9. From Figure 9, it is observed that the PDPWM strategy produces significant 30th, 32nd and 38th harmonic energy. Figure 10 shows the five level output voltage generated by VAPDPWM strategy and its FFT plot is shown in Figure 11. From Figure 11, it is observed that the VAPDPWM strategy produces significant 5^{th,} 7th and 38th harmonic energy. Figure 12 shows the five level output voltage generated by PODPWM strategy and its FFT plot is shown in Figure 13 From Figure 13, it is observed that the PODPWM strategy produces significant 33rd, 35th and 39th harmonic energy. Figure 14 shows the five level output voltage generated by VAPODPWM strategy and its FFT plot is shown in Figure 15. From Figure 15, it is observed that the strategy produces significant 5th, 27th, 29th and 39th harmonic energy. Fig.16 shows the five level output voltage generated by VFPWM strategy and its FFT plot is shown in Figure 17. From Figure 17,

it is observed that the VFPWM strategy produces significant 5th, 33rd, 35th and 39th harmonic energy. Figure 18 shows the five level output voltage generated by VAVFPWM strategy and its FFT plot is shown in Figure 19. From Figure 19, it is observed that the VAVFPWM strategy produces significant 5th, 36th and 38th harmonic energy. The following parameter values are used for simulation: V_{dc} = 200V, f_c = 2000Hz, f_m = 50Hz and R (load) = 100 ohms.

5.1.Simulation of PDPWM Technique

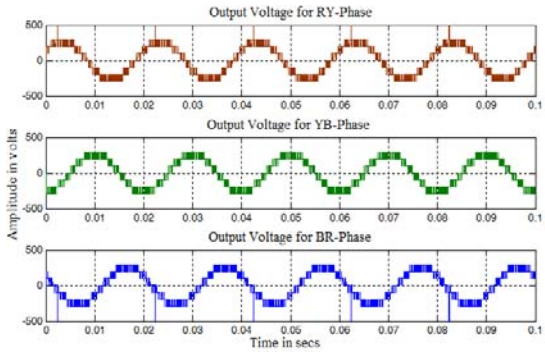

Figure 8. Simulated output voltage generated by PDPWM technique for R-load

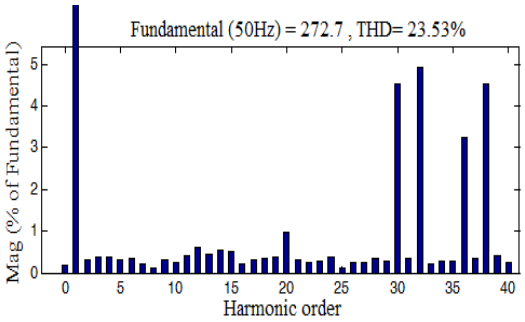

Figure 9. FFT spectrum for PDPWM technique

5.2. Simulation of VAPDPWM Technique

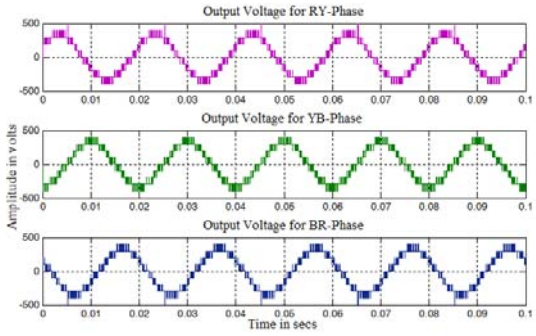

Figure10. Simulated output voltage generated by VAPDPWM technique for R-load

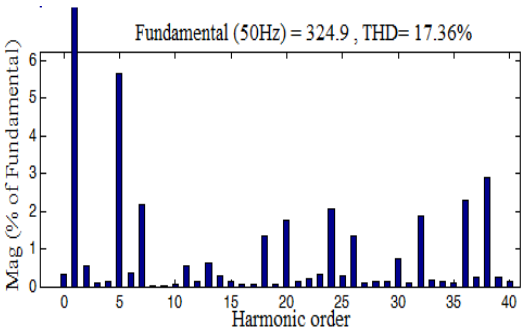

Figure 11. FFT spectrum for VAPDPWM technique

5.3. Simulation of PODPWM Technique

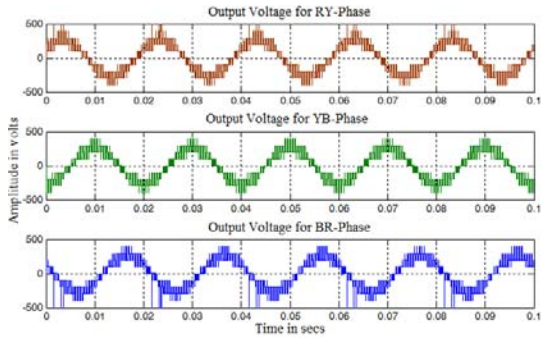

Figure 12. Simulated output voltage generated by PODPWM technique for R- load

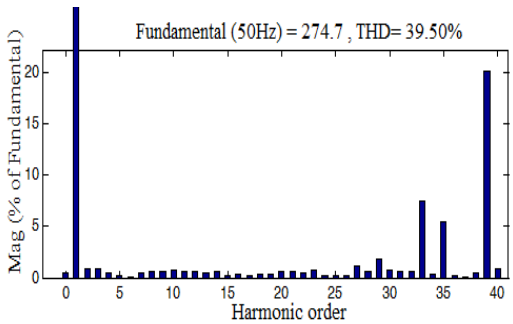

Figure 13. FFT spectrum for PODPWM technique

5.4. Simulation of VAPODPWM Technique

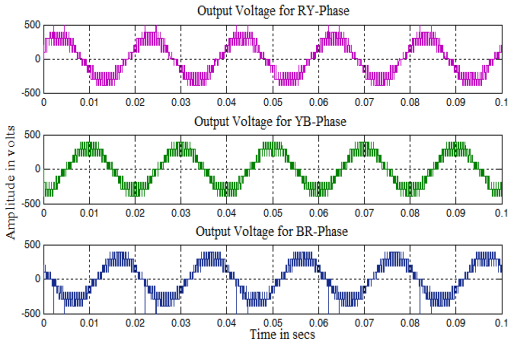

Figure 14. Simulated output voltage generated by VAPODPWM technique for R- load

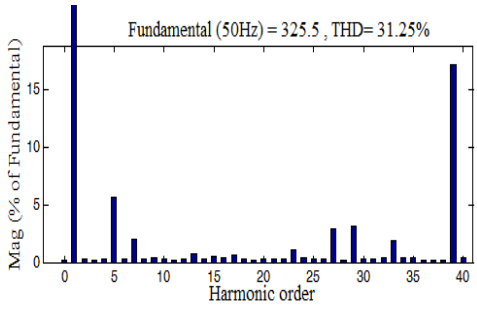

Figure 15. FFT spectrum for VAPODPWM technique

5.5. Simulation of VFPWM Technique

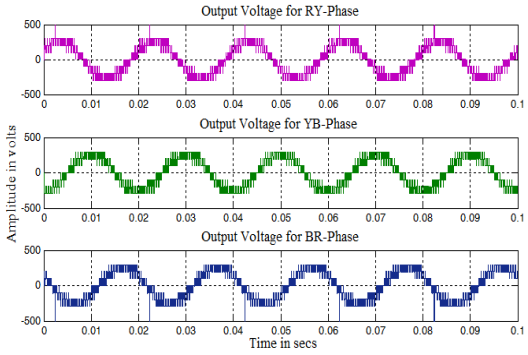

Figure16. Simulated output voltage generated by VFPWM technique for R-load

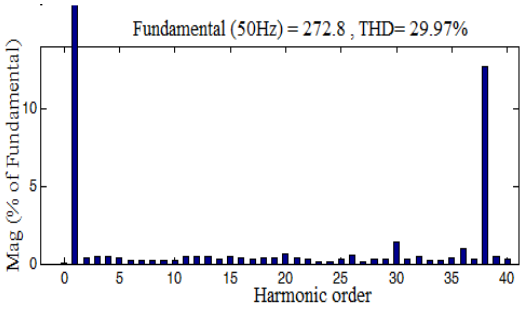

Figure 17. FFT spectrum for VFPWM technique

5.6. Simulation of VAVFPWM Technique

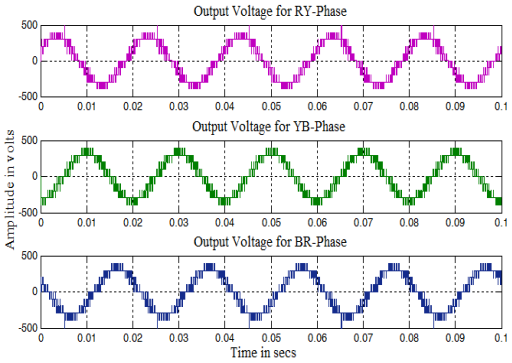

Figure 18. Simulated output voltage generated by VAVFPWM technique for R-load

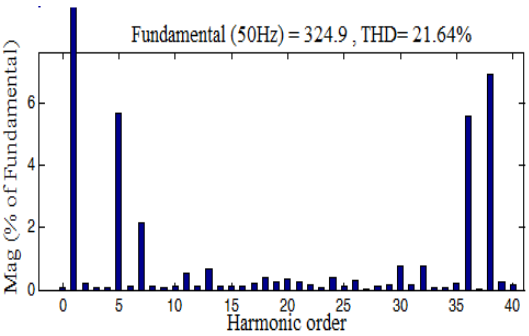

Figure 19. FFT spectrum for VAVFPWM technique

Table 3. % THD of output voltage of chosen hybrid H-bridge MLI for various values of modulating indices

m_a	PD	VAPD	POD	VAPOD	VF	VAVF
1	17.74	17.76	24.10	21.57	21.41	20.98
0.9	17.76	18.05	34.59	26.67	24.29	21.21
0.8	23.53	17.36	39.50	31.25	29.97	21.64
0.7	25.27	19.44	43.12	35.11	33.38	24.67
0.6	28.70	25.79	41.19	35.36	35.91	31.20

Table 4. V_{RMS} (Fundamental) of output voltage of chosen hybrid H-bridge MLI for various values of modulating indices

m_a	PD	VAPD	POD	VAPOD	VF	VAVF
1	241.7	262.5	242.1	263.5	241.8	249.5
0.9	216.8	246.4	218.7	246.6	216.7	246.4
0.8	192.9	229.8	194.2	230.1	192.9	229.7
0.7	168.2	212.5	169	212.9	168.1	212.7
0.6	143.7	196.1	143.2	195.3	143.9	196.1

Table 5. Form Factor of output voltage of chosen hybrid H-bridge MLI for various values of modulating indices

m_a	PD	VAPD	POD	VAPOD	VF	VAVF
1	5935	6447.5	25570	27450	3390.0	1355.7
0.9	413.46	2681.1	5920	26260	741.37	2674.4
0.8	881.81	1134.0	INF	2285.4	1211.8	INF
0.7	1430.0	3558.3	INF	725.45	4295.0	10705
0.6	433.23	104.85	1189.2	1245	369.5	2225.5

Table 6. Crest Factor of output voltage of chosen hybrid H-bridge MLI for various values of modulating indices

m_a	PD	VAPD	POD	VAPOD	VF	VAVF
1	1.4145	1.4140	1.4142	1.4144	1.4143	1.4140
0.9	1.4142	1.4143	1.4138	1.4140	1.4143	1.4143
0.8	1.4136	1.413	1.4145	1.4146	1.4142	1.4144
0.7	1.4143	1.4145	1.4142	1.4142	1.4140	1.4141
0.6	1.4140	1.4145	1.4141	1.4142	1.4141	1.4140

Table 7. Distortion Factor of output voltage of chosen hybrid H-bridge MLI for various values of modulating indices

m_a	PD	VAPD	POD	VAPOD	VF	VAVF
1	0.084	0.2362	0.1144	0.2538	0.0448	0.2453
0.9	0.0468	0.2399	0.1415	0.2346	0.0302	0.2487
0.8	0.0937	0.2674	0.2311	0.2437	0.1158	0.2384
0.7	0.0674	0.2224	0.1878	0.2374	0.0717	0.2252
0.6	0.1557	0.1687	0.1266	0.1656	0.1501	0.1747

6. Conclusion

The proposed modified hybrid H-bridge multilevel inverter has been simulated using MATLAB. The five level inverter can operate as a nine level inverter in three phase systems interms of line to line voltage. So compared to the phase voltage the line to line voltage performance are better. The important characteristic of the proposed system is able to be

extended to any number of output voltage levels with less number of switches. This system can overcome some of the limitations of the conventional $MLI_{S.}$ This method results harmonics decreases as the number of levels increase, less number of switches and cost of the converter. Performance indices like %THD, V_{RMS} (indicating the amount of DC bus utilization), CF, FF and DF related to power quality issues have been evaluated, presented and analyzed. Based on presented switching algorithm, the chosen multilevel inverter generates near sinusoidal output voltage and as a result, has relatively low harmonic content for the VAPDPWM strategy. It is also seen that VAPODPWM technique is found to perform better for all strategies since it provides relatively higher fundamental RMS output voltage. Table 3 and 4 shows the total harmonic distortion and RMS for all chosen modulating indices. Table 5 displays form factor for all modulating indices. Table 6 and 7 display the crest factor and distortion factor for all chosen modulating indices.

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