# Method for improving ripple reduction during phase shedding in multiphase buck converters for SCADA systems

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### Article Info ABSTRACT

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In the current digital environment, central processing unit (CPUs), field programmable gate array (FPGAs), application-specific integrated circuit (ASICs), as well as peripherals, are growing progressively complex. On motherboards in many areas of computing, from laptops and tablets to servers and Ethernet switches, multiphase phase buck regulators are seen to be more common nowadays, because of the higher power requirements. This study describes a four-stage buck converter with a phase shedding scheme that can be used to power processors in programmable logic controller (PLCs). The proposed power supply is designed to generate a regulated voltage with minimal ripple. Because of the suggested phase shedding method, this power supply also offers better light load efficiency. For this objective, a multiphase system with phase shedding is modeled in MATLAB SIMULINK, and the findings are validated.

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#### 1. **INTRODUCTION**

Buck converters have grown in popularity in recent years due to the increased need for speed and efficiency. Multiphase systems use an interleaving strategy to distribute processing functions, which is based on the parallel connection of conventional power sources. The benefits of this approach, such as rapid transient time and reduced ripple at the output voltage, make it suitable for voltage regulator module (VRM) [1]. The power needs are continually growing as multi-cores are incorporated into a single processor [2] and the voltage regulators that power these microprocessors are essential for improving system dynamic performance, reliability, and efficiency while saving money and increasing power density [3]. In these areas, buck converters excel. The transition strain is equally spread across the phases, allowing for more power to be delivered. If all phases are separated evenly, the output signal amplitude will be N times less than a single-phase one, removing the need for output filters [4]-[7]. In high-power cases that require high efficiency and minimal component stress, interleaved topologies increase converter efficiency by decreasing current pressure on switching devices. In addition, the interleaved design reduces source current and ripple voltage at the output [8]. Selected a four-stage buck converter for the intended application. The proposed multiphase buck regulator is designed especially for the programmable logic controller (PLC) power supply, which is a part of supervisory control and data acquisition (SCADA) systems. But in general, this is applicable to any kind of low voltage and high current systems. A PLC is a commercial computing system that is used to control production line procedures and other factory automation equipment that

requires a very highly reliable control approach as well as problem diagnosis. A PLC system consists of analog and digital input and output components, as well as a communication module, a central processing unit (CPU) component, a control component, and a power supply. Several integrated circuit sub-systems within the PLC system, such as an analog front-end (AFE), backplane communication, electronic processing microcontrollers, field programmable gate array (FPGAs), wires or cordless interfaces, clocking, memory, and user interfacing, all require power. PLCs are used in demanding, durable production environments and require extra attention when constructing a nonisolated point-of-load power solution.

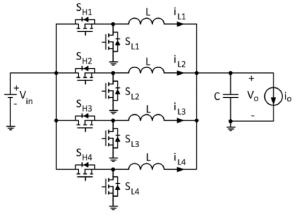
Servers, CPUs, laptops, and workstations are all powered by multi-phase voltage regulators. Recently, attempts have been made to improve the efficiency of such a regulator by constantly changing the number of active phases in addition to the rise in current consumed by the load. Indeed, analyzing the efficiency curve as a combination of load current and phase count reveals that, under low loads, reducing the number of active phases improves efficiency. Other than higher efficiency at light load, this technique also increases output voltage ripple [9]. The present work deals with the development of a new direct current-direct current (DC-DC) converter with lower voltage ripple and higher efficiency [10]. A phase-controlling technique is used to achieve an optimal performance curve by shutting off a defined number of phases as the electric demand decreases [11]. Losses in the switching converters play a major role in the converter efficiency. Single-phase buck converters have low efficiency at light loads in general [12]. Activating many phases simultaneously reduces effective on-resistance, which improves efficiency for larger load current. The number of active phases must be reduced to a minimum at lower load currents to decrease switching loss and enhance efficiency [13]. However, because the load is distributed over all modules, the percentage load experienced by individual modules varies as the number of active phases changes [14].

This thesis suggests a new technique, called the frequency control technique, to improve the ripple reduction in multiphase converters. The frequency control method suggests increasing frequency during light loads, to improve the reduction in ripple. This is done by reducing the duty cycle of the stage progressively to zero. In this job, an average model of the frequency control method is created as well as the required frequency during phase shedding is calculated on the basis of different specifications. The mathematical designs of these converters are critical for studying the system's dynamic behaviors [15]. The frequency control technique is also compared to other common ways presented in literature and it has been validated analytically as well as through simulation based on the MATLAB/Simulink model [16]. The remaining part of the paper is organized. The second part covers a four-stage buck converter and its efficiency under various loads. Section three provides simulation findings that demonstrate reduced output voltage ripple. Section four brings the paper to a completion.

### 2. BASIC SCHEME OF MULTIPHASE BUCK CONVERTER

Figure 1 illustrates the basic architecture of a four-stage DC-DC buck converter. The suggested multiple input structure's basic cell consists of two switches and a DC source. The switches are isolated from one another [17]. The converter is made up of four-unit cells, each of which includes a DC voltage source, a transistor as a switch, and a diode [18]. Limited the number of phases to four (N=4) as an illustration rather than a limitation, in order to keep the diagram simple and sufficiently discuss the paper's methodology in depth. Instead of all phases being engaged (switched ON) at the same time, the four-phase converter's switching pattern is normally staggered evenly in this design. In other words, in the case of N = 4, each pulse width modulation (PWM) signal has a phase shift of a multiple of 90°. Figure 2 compares the switching cycles of a single-phase and a four-phase converter. Among the other benefits described in the earlier section, such a multiphase converter reduces output ripple and lowers DC inductor current per phase [19].

Figure 3 compares the voltage ripple of single phase and four-phase converters, and Figure 4 shows the normalised input capacitance root mean square (RMS) current. As the various ripple currents for each phase cancel each other out, the input RMS current goes to zero. Multiphase interleaved buck VRM (MPVRM) permits low-voltage high-current operation while providing high power density, high conversion efficiency, and quick dynamic response [20]. Due to higher switching loss, interleaved DC/DC converters have lower efficiency at mild loads than their single stage counterparts. Several strategies have been developed to increase the light load efficiency of DC/DC converters. The recommended solution for enhancing the light load efficiency of higher power applications is phase shedding [21]. Over a large load range, the phase-shedding approach helps to improve the converter efficiency. When the load current is lowered, the number of running phases is reduced, and just one phase is gradually linked to the load system under mild loads [22]. However, under medium and light loads, removing a few stages from the converter tends to cause the amount of alternating current (AC) content at the existing input and output to increase. Furthermore, this may result in exceeding the maximum current and voltage surge requirements. This method also results in larger power losses, negating the benefit of phase-shedding during light loads.



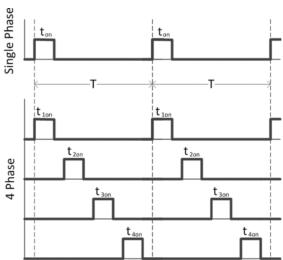


Figure 1. Four-phase dc-dc converter

Figure 2. Comparison in switching cycle of 4phase converter and single-phase converter

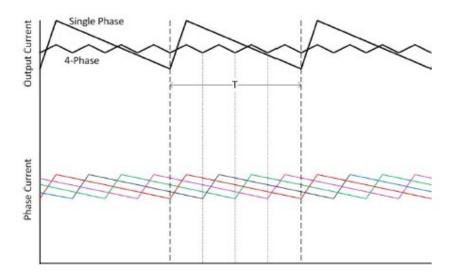
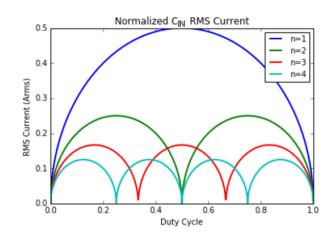
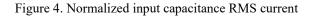


Figure 3. Single-phase vs. four-phase converter output voltage ripple





Several ways to minimize the impact of this issue have previously been presented in earlier research. The purpose of this study is to validate the performance of a multiphase converter [23] with variable frequency control during phase shedding. When the electric loads of the power supply system increase, the multiphase power converter attempts to adjust the frequency through the control loop by changing the switching frequency as the load changes. Throughout the load transient, this process continues. A greater increase in switching frequency is dependent on a considerably larger increase in the load transient. The innovative approach presented herein is based on the fact that a four-phase power converter fundamentally operates at a variable switching frequency. This approach works in such a way that when there is a light load, the number of stages automatically reduces due to the phase shedding management mechanism. As a result, the ripple content at the output voltage increases. During this step, the switching frequency raises and decreases the output voltage ripple automatically. This aids in the minimization of output voltage ripple. As a result of this suggested approach, reduced ripple and efficiency improvements at light load can be obtained. Table 1 shows the efficiency calculation for all the 4 phases as per load current variation. It is clear from the calculations that the light load efficiency is higher than the full load efficiency [24]. The light load efficiency for the 4th phase is 86% and the light load efficiency of the 2, 3 and 4 phases is 87%, 88% and 89% respectively. Figure 5 depicts a four-phase converter's efficiency curve graphically. In order to improve converter efficiency, one may switch on or off any combination of phases. For example, if the 4-phase buck converter's output current is just 50% of its peak value, two phases can be removed to obtain the same efficiency when all four phases are turned on [19].

Table 1. Output load current vs efficiency of all the 4 phases of converter				
Iout	Efficiency Phase4	Efficiency Phase3	Efficiency Phase2	Efficiency Phase1
1	86.67788312	87.04130397	88.68206969	89.91189102
2	90.23649923	90.09876649	90.81963178	91.00762911
3	91.45800732	91.12624925	91.49536835	91.26007955
4	92.05849212	91.61885682	91.79199318	91.2977642
5	92.40431381	91.89291832	91.93478608	91.2492298
6	92.62103318	92.05642589	92.0001046	91.15772715
7	92.76333007	92.15630231	92.02098839	91.04189006
8	92.85883425	92.21622222	92.01406158	90.91106651
9	92.92301144	92.24942327	91.98860113	90.77046115
10	92.96519364	92.2638866	91.95019185	90.62320114
11	92.9913456	92.26471026	91.90239687	90.47127802
12	93.0054579	92.25530328	91.84759646	90.31601978

Table1. Output load current vs efficiency of all the 4 phases of converter

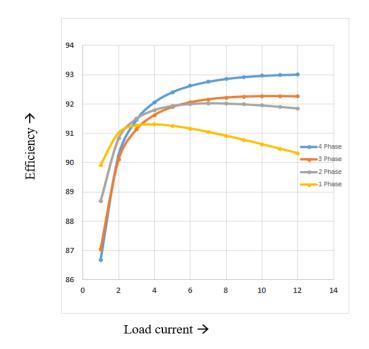


Figure 5. Efficiency of 4phase converter vs. load conditions

### 3. SIMULATION RESULTS AND DISCUSSION

A 108W, 30V/12V voltage regulator has been constructed and simulated using the approaches described above. The improvement in light load efficiency for a 4-stage structure with phase shedding mode is assessed [25]. Figure 6 presents the controlled voltage and current waveforms of a four-phase buck converter. With a load of 12A, the output voltage is controlled at 9V. Figure 7 displays the gate pulses to the four switches in the four-phase converter, as well as the load current against output ripple voltage. From the figure, it is evident that the output ripple voltage is approximately 8mV at a switching frequency of 200kHz.

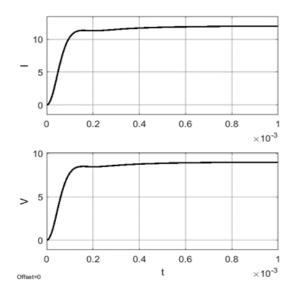


Figure 6. Regulated output volage and current from 4phase converter

Figure 8 shows the gate pulses for three switches of a four-phase converter, as well as the ripple in output voltage as a function of load current. The ripple voltage in this case is 1.8mV at 230Khz. Figure 9 illustrates gate pulses to two switches of a four-phase converter, as well as the load current vs output voltage ripple, which is 1.7mV at 240KHz. Figure 10 represents gate pulses to a single switch for a four-phase converter, as well as the load current vs output ripple voltage, which is 1.3mV at 270kHz.

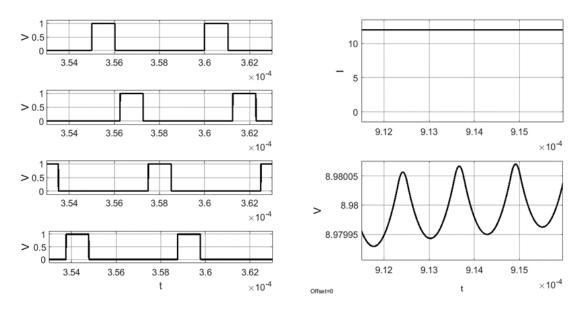


Figure 7. Gate pulses to the 4phase converter and load current vs output ripple voltage

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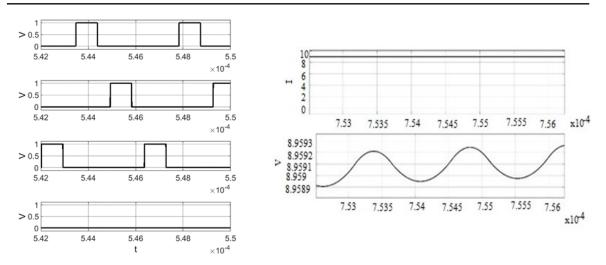


Figure 8. Switching pulses to the 3phase converter and load current vs ripple content at output voltage

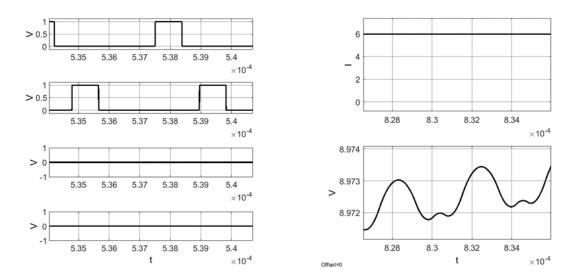


Figure 9. Switching pulses to the 2phase converter and load current vs ripple content at output voltage

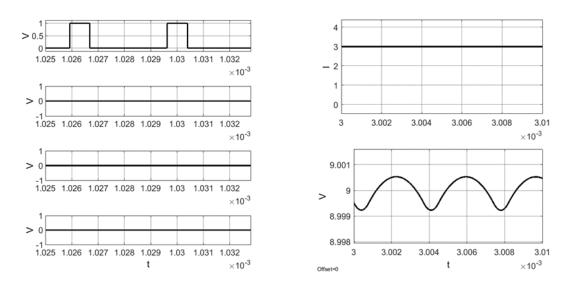


Figure 10. PWM pulses to the single-phase converter and load current vs output ripple voltage

### 4. CONCLUSION

This study presents a four-stage buck converter with a phase-shedding control scheme to enhance the efficiency of light load converters. The goal of this study was to show that output ripple voltage may be reduced without compromising converter light load efficiency. After incorporating the proposed method into a multiphase converter, it is evident that the ripple at the output voltage decreases over time as the phase reduction procedure progresses. Circuit simulation data is used to determine and evaluate light load efficiency enhancements. The ripple content at the output voltage has been reduced to 1.3mV under light load, and the efficiency has been improved to a higher extent, according to the simulated results. This ideal approach has been shown to be the best option for processors used in high-power applications.

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