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A Novel Unit Power Factor Rectifier Based on Three-phase Digital PLL

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Abstract

A novel three-phase phase-locked loop solution is proposed based on D-Q transformation aiming at the AC-DC rectifier with high efficiency and high power factor. The phase-locked loop is implemented digitally using the Xilinx blockset integrated with Matlab/Simulink. The three-phase digital phase-locked loop (TDPLL) is elaborately designed with the parameters defined in detail. The AC-DC converter (rectifier) model with the TDPLL is built and simulated in the high-speed VHS-ADC simulation platform from Canada. The simulation and test results show the TDPLL is locked right after the different three-phase voltage disturbances and very suitable for control of the rectifier with high parallelism through space vector pulse width modulation (SVPWM).

Keywords: *digital phase locked loop (DPLL), field-programmable gate array (FPGA), rectifier, space vector pulse width modulation (SVPWM), high power factor*

1. Introduction

The new energy sources such as solar energy and wind power have been paid more attention these years. More and more power and electronic devices are used with the large-scale grid-connected generation system. However these nonlinear devices and loads introduce much harmonics and induce low power factor, following which is the raise of the standard of connecting to the power grid [1-2]. To achieve high power quality and high efficiency, all kinds of circuit topologies and control methods are studied [3]. A novel single-stage high-power-factor AC-DC converter adopts a full-bridge resonant converter, which is integrated with two buck–boost-type power factor corrector (PFC) circuits [4]. An interleaved flyback topology is applied in a three-phase unity-power-factor single-stage ac–dc converter [5]. Both of the two topologies can improve the circuit efficiency, but the circuit structures are complex with more components used.

Another way to high efficiency converter is use of the control methods which can save the devices and components. The real-time phase synchronization with grid voltage is very important for switching of power devices, calculation of active and reactive power, and transformation between the different coordinates. The phase synchronization techniques are usually implemented based on the zero-crossing detector and the phase locked loop (PLL) in a power system. The zero-crossing detector calculates the phase according to the time of zero-cross points but it shows poor dynamical performance and is very vulnerable to the harmonics, DC offset and the other disturbances [6].

The PLL is commonly used for the phase synchronization and significant for the whole control system because it provides the accurate and real-time phase angles, and the reference for calculation. The synchronization of phase can be realized through hardware and software. The hardware PLL such as CD4046 is usually used for hardware synchronization by dynamically following the signal frequency deviation and changing the sampling frequency. The hardware synchronization is simple, fast and widely used in engineering practices but not reliable. The measurement error is larger in case of wave distortion. In addition the inherent error is serious resulting from complicated circuits, hardware delay and drift.

The software synchronization is implemented through software algorithms based on CPU, DSP or FPGA. The method is of simple circuitry, high precision and strong control of

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tracking time [7-11]. As the processing elements, CPU and DSP reduce the limitation of processor speed in parallel to some extent but the parallelism is limited. In such parallel mode the implemented tasks are not divided according to the degree of parallelism and complexity so the simulation step is commonly decades of microseconds. On the other hand, the real-time tracking will be improved to a great extent if the FPGA is preferred in the part of high parallelism, and the CPU in the part of high complexity [12-13].

It is unnecessary to know very well the hardware when using the FPGA as a central processor to design the signal processing system since Xilinx System Generator for DSP is applicable. Matlab/Simulink provides a versatile platform for the System Generator which translates directly the blocked algorithms into a bitstream file and then downloads it into the FPGA. In this paper a high-speed data-processing system VHS-ADC from Canada based on FPGA is used to design the three-phase PLL which is then applied to the three-phase voltage-source SVPWM rectifier. The discrete-domain models of the SVPWM rectifier based on the Xilinx blockset are built. The simulation results about the SVPWM rectifier show that the three-phase digital PLL is very useful to make a rectifier with high power factor (PF) if the power quality problems happen to the power source such as voltage sag and three-phase unbalance.

2. Model of SVPWM Rectifier

2.1. Structure of SVPWM Rectifier

The main circuit structure and control diagram of the three-phase voltage-source SVPWM rectifier are illustrated in Figure 1. The main circuit consists of three-phase AC voltage source, filter inductance and equivalent resistance in grid side, filter capacitance and load in DC side, and the three-phase full-bridge IGBT switch between the two sides. The all-digital control system is mainly composed of grid-side digital voltage filter and current filter, coordinate converter, forward-feed decoupling controller, three-phase digital PLL (TDPLL) and SVPWM pulse generator.

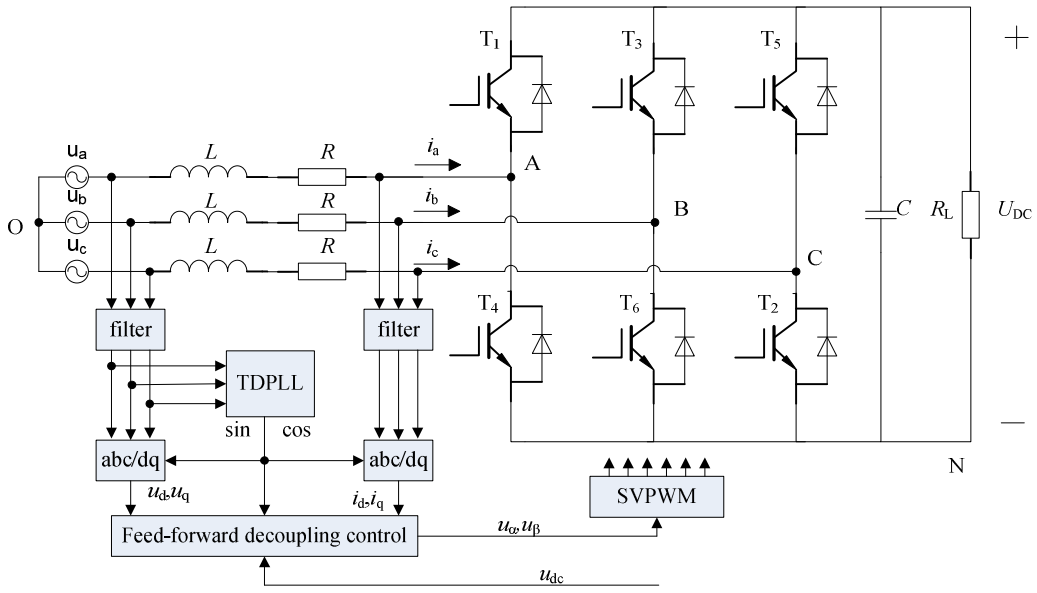

Figure 1. Main circuit and control diagram of three-phase svpwm rectifier

2.2. D-Q Model of SVPWM Rectifier

The mathematical model of the three-phase rectifier can be expressed as the following equation system (1) about the state variables of AC-side inductance current and DC-side capacitance voltage.

$$\begin{cases} L\dfrac{di_a}{dt}+Ri_a=u_a+\dfrac{(-2S_a+S_b+S_c)u_{DC}}{3} \\ L\dfrac{di_b}{dt}+Ri_b=u_b+\dfrac{(S_a-2S_b+S_c)u_{DC}}{3} \\ L\dfrac{di_c}{dt}+Ri_c=u_c+\dfrac{(S_a+S_b-2S_c)u_{DC}}{3} \\ C\dfrac{du_{DC}}{dt}+\dfrac{1}{R_L}u_{DC}=i_aS_a+i_bS_b+i_cS_c \end{cases} \quad (1)$$

The three-phase voltages ua, ub, uc and currents ia, ib, ic are time-varying AC variables, and couple with each other so that it is not easy to realize the stable control of the rectifier. Therefore, the model under the three-phase static coordinate system is converted to the model under the two-phase rotating coordinate system as eq.(2) through Park transformation. As a result, the fundamental sinusoidal variables under the three-phase symmetrical static coordinate system are converted to the DC variables under the synchronous rotating reference frame, which simplifies the design of the control system.

$$\left.\begin{aligned} u_d &= U_m\sin(\varphi-\theta) \\ u_q &= -U_m\cos(\varphi-\theta) \end{aligned}\right\} \quad (2)$$

Let $\theta=\omega t+\theta_0$, $\varphi=\omega t+\varphi_0$, then

$$\left.\begin{aligned} u_d &= U_m\sin(\varphi_0-\theta_0) \\ u_q &= -U_m\cos(\varphi_0-\theta_0) \end{aligned}\right\} \quad (3)$$

The fundamental-frequency AC voltages are converted to the DC D-Q components after Park transformation. And furthermore the mathematical model under the D-Q reference frame can be derived as eq. (4).

$$\left.\begin{aligned} L\frac{di_d}{dt} &= u_d+\omega Li_q-Ri_d-S_du_{DC} \\ L\frac{di_q}{dt} &= u_q-\omega Li_d-Ri_q-S_qu_{DC} \\ C\frac{du_{DC}}{dt} &= -\frac{1}{R_L}u_{DC}+\frac{3}{2}(S_di_d+S_qi_q) \end{aligned}\right\} \quad (4)$$

3. Modelling and Simulation of TDPLL

In general the different PLL methods have different phase detectors. The phase detector of three-phase digital PLL (TDPLL) is implemented through coordinate transformation different from the common PLL methods.

Let the phase of grid voltage $\varphi=\omega_1t+\varphi_0$, the phase output of PLL $\theta=\omega_2t+\theta_0$, where ω_1 and ω_2 are respectively the frequency of the grid voltage and the frequency of the PLL output.

According to (2) when the PLL is not yet in the capturing state, ud is an AC component.

$$u_d=U_m\sin[(\omega_1-\omega_2)t+(\varphi_0-\theta_0)] \quad (5)$$

When the PLL goes into the capturing state but the phase difference still exists, ud is a DC component representing the phase error between the input phase and output phase of the PLL.

$$u_d = U_m \sin(\varphi_0 - \theta_0) \tag{6}$$

When the PLL is completely locked,

$$u_d = 0 \tag{7}$$

The locking process of three-phase PLL is nonlinear but the phase difference is very small at the beginning of locking process, so the following equivalent substitution is applicable.

$$\sin(\varphi - \theta) \approx (\varphi - \theta) \tag{8}$$

As a result, the phase detection element of the three-phase PLL can be expressed as (13).

$$u_d = K(u_\alpha \cos\theta - u_\beta \sin\theta) \approx K(\varphi - \theta) \tag{9}$$

From the above analysis, it can be seen the phase detector of three-phase PLL is implemented by making the d-axis component zero.

The TDPLL consists of digital phase detector (PD), digital filter, digital voltage controlled oscillator (VCO) and sampling synchronizer from the structure diagram of TDPLL in Fig. 2 which compose a closed-loop phase control system. The digital phase detector implements static coordinate transformation and outputs phase error which is the difference between the given phase of voltage input and the PLL output. Based on the detected phase error, the PI regulator creates the error control signal which is then added to the offset frequency. As a result, the sum is used as the frequency control word of VCO. Then according to the frequency control word, the VCO produces the given phase from the phase accumulator and finds the sine and cosine values from the built-in lookup. The VCO provides the phase feedback for digital phase detector. At the same time, the sampling synchronizer provides the synchronization signals for the input and output of PLL, and the PI filter at the zero point of sine.

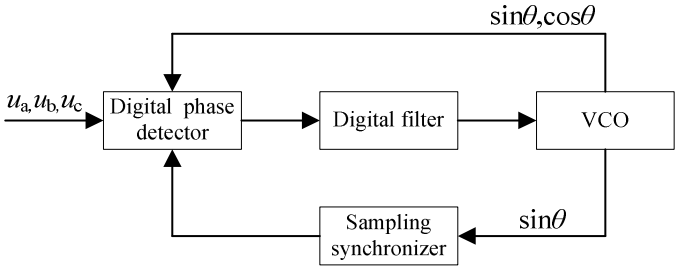

Figure 2. Structure diagram of TDPLL

Figure 3 demonstrates the discrete-domain model of the abc-αβ transformation based on the Xilinx blockset, which provides the input Uα, Uβ for the digital PD. In Figure 4, the input Uα, Uβ and the feedback signals sinθ, cosθ are sampled by four registers. The phase error is obtained through two multiplier blocks (Mult) and an adder block (AddSub). In the PI regulator, the integrator can be substituted by an accumulator as a result that the gain blocks CMult, CMult1, CMult2, the accumulator block (Accumulaor) and the adder block (AddSub) constitute a digital filter. In the Xilinx blockset, two methods can be used for VCO. One method is that at first the filter output angular frequency ω is integrated to obtain the phase θ, and then compute the sine and cosine values using the Sinecosine block in the Xilinx blockset. However, the width of the block is limited to 3-10 digits when running in a conventional PC, which leads to the low phase resolution. The other method is that the VCO is implemented by the DDS block. In the DDS block there exist phase accumulator and lookup, so the sine and cosine values can be

directly obtained. In addition, the accumulator has a phase width up to 32 bits, so the θ-sinθcosθ transformation is much more accurate.

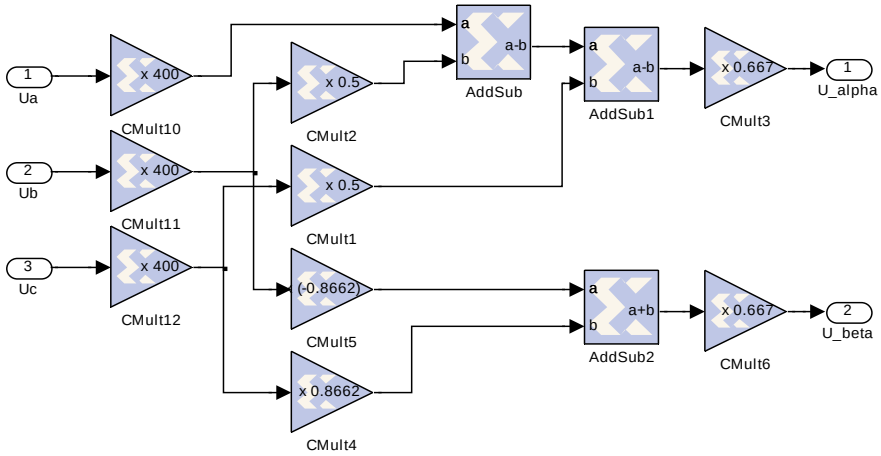

Figure 3. Abc-αβ transformation

The relation between the frequency control word M (data port of DDS), the system clock fclk and the output frequency fout can be expressed as following:

$$f_{out} = f_{clk} / 2^N \times M \tag{10}$$

Where fout=50Hz, fclk=100kHz, N is the integral number bits of the input signal. N=0 if the input is 32 digits since the width of DDS input is required to equal to decimal width. According to eq. (10), the central frequency control word M=5e-4, is none other than the control signal of frequency offset. Considering the output of low-pass filter (LPF) is likely flooded by the central frequency, the frequency offset is enlarged and then added to the LPF output. For this, 5e-4 can be enlarged as table 1 by the left shift block and vice versa the offset frequency can be scaled down to 5e-4 by the right shift block.

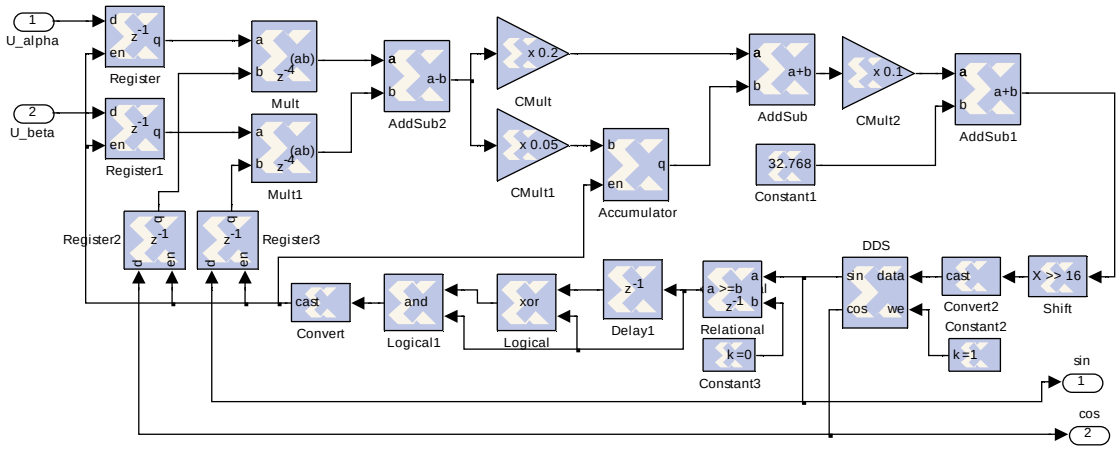

Figure 4. Three-phase digital pll

Table 1. Bit number of shift block and offset frequency

Left shift	11	12	13	14	15	16	17
Offset freq	1.024	2.048	4.096	8.192	16.384	32.768	65.536

Therefore the offset frequency should be set to 32.768Hz if 16-bit right shift block is used in Figure 4.

It is useful to find the difference at the zero-crossing point between the input signal and the feedback signal of the PLL since the precondition for the locking phase of TPDLL is that the phase error is very small. Therefore the narrow trigger pulses with the same period as the output of DDS sin port are generated at its zero-crossing point. The pulses provide the enable signals for the two sampling registers of the PD input, two sampling registers of the PD feedback, and the accumulator of LPF to synchronize the sampling and computation. In addition, the PLL operates only one time every fundamental period, as a result the computation load is largely reduced and the integration saturation is greatly improved.

In this section, a high-efficiency TDPLL is designed for the SVPWM control of a three-phase rectifier. Next section the application and results are presented.

4. Application of TPDLL to SVPWM Rectifier

The VHS-ADC, a high-speed data processing platform based on FPGA from Canada, is shown in Figure 5. It contains high-speed A/D, D/A channels and 32-bit GPIO port. The platform can link to Matlab/Simulink seamlessly and automatically compile and download from model to code. In addition, it improves greatly the simulation efficiency and research process through HIL (hard in loop) simulation together with the test circuit.

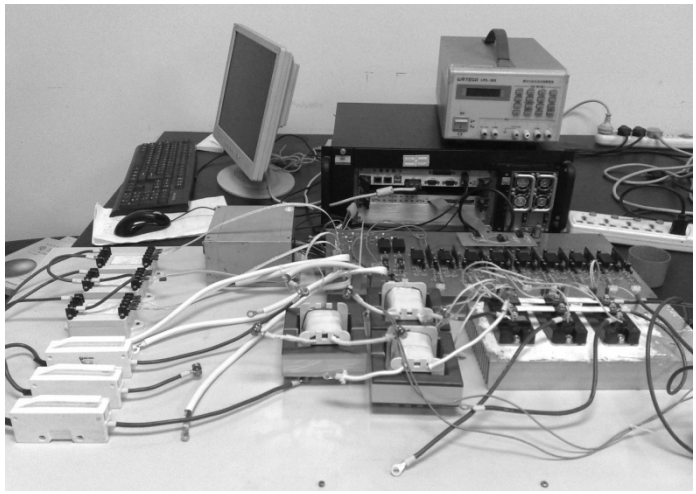

Figure 5. VHS-ADC test platform

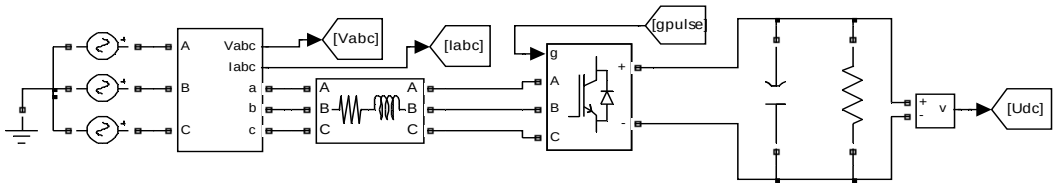

Figure 6. Main circuit model of three-phase rectifier

The main circuit model of three-phase rectifier is built in Matlab/Simulink as Figure 6. Let the amplitude of phase voltage be 311V, frequency 50Hz, AC-side resistance R=0.5Ω, inductance L=6mH, output filter capacitance C=1000uF, load resistance RL=18Ω.

The Figure 7 presents the control model of the SVPWM rectifier with digital PLL. The block TDPLL generates the unit vector (sin, cos) in accordance with the grid voltage for Park transformation and inverse Park transformation. The DBC block comprises the double closed-loop control strategy based on the feed-forward-decoupling method. The SVPWM block generates the drive pulses based on the space vectors.

To verify the Xilinx FPGA-based model and the PLL algorithm, the simulation test analysis is carried out under three situations of the voltage sag, three-phase voltage unbalance and ideal voltage.

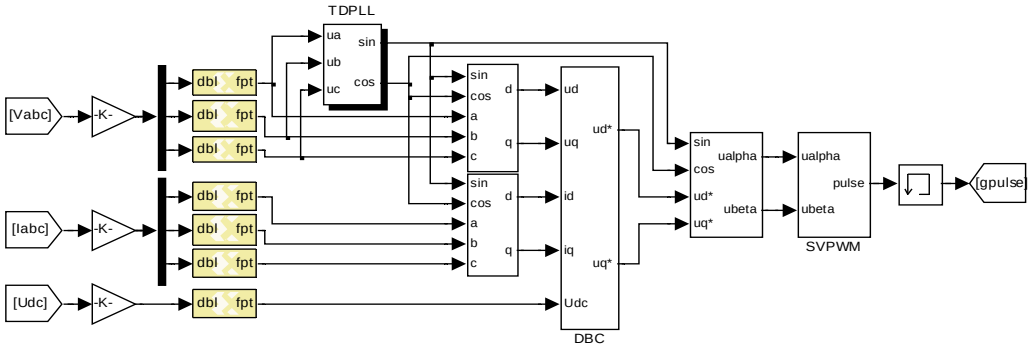

Figure 7. Control model of the svpwm rectifier

Figure 8-a presents the DC output of SVPWM rectifier when the voltages are ideal in AC side. From the figure it can be seen the dynamic process is short and the steady-state error is very small. The voltage and current wave in AC side are illustrated in Figure 8-b. The voltage and current are synchronized after a short time of several periods so that the high-PF rectification is realized. In Figure 8-c, the phase detection error of the PLL is rapidly reduced to zero.

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = 311 \begin{bmatrix} \sin(314t) \\ \sin(314t - 2\pi/3) \\ \sin(314t + 2\pi/3) \end{bmatrix} \tag{11}$$

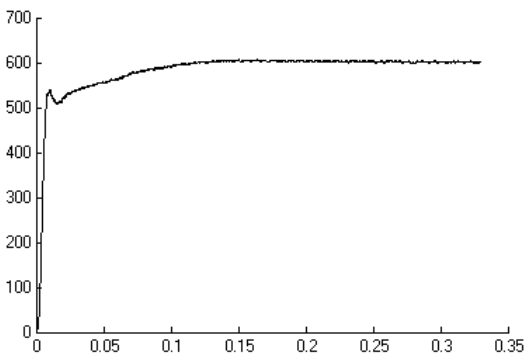

Figure 8-a. DC output under ideal voltage

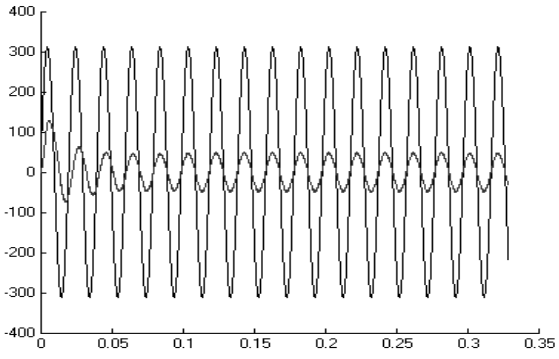

Figure 8-b. AC-side source voltage and inductance current under ideal voltage

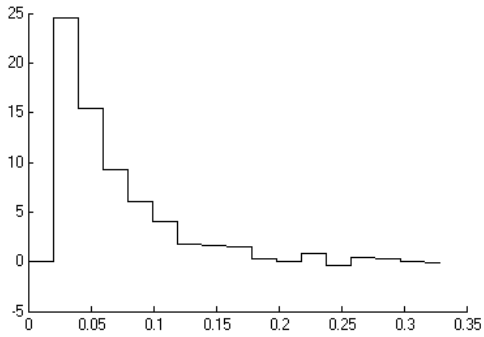

Figure 8-c. Phase detection error under ideal voltage

The segmented voltage is expressed as (12) in case of the duration between 0.135 and 0.23s of the voltage sag. Figure 9-a,b,c show the voltage and current in AC side, DC output and the error of phase detector. They will rapidly restore to normal operation with the help of TDPLL.

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = 200 \begin{bmatrix} \sin(314t) \\ \sin(314t - 2\pi/3) \\ \sin(314t + 2\pi/3) \end{bmatrix} \quad 0.135\text{s} \le t \le 0.23\text{s} \tag{12}$$

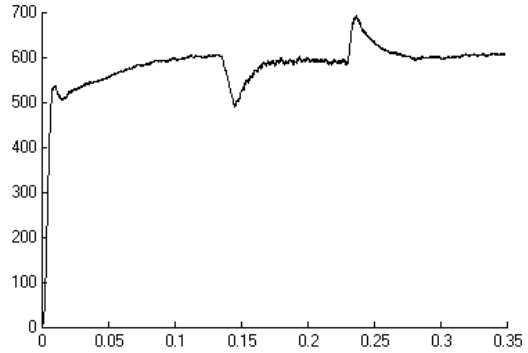

Figure 9-a. DC output in case of voltage sag

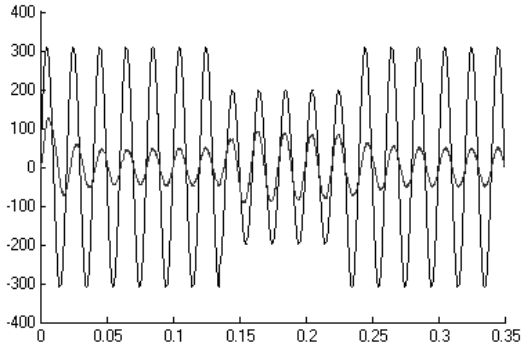

Figure 9-b. AC-side source voltage and inductance current in case of voltage sag

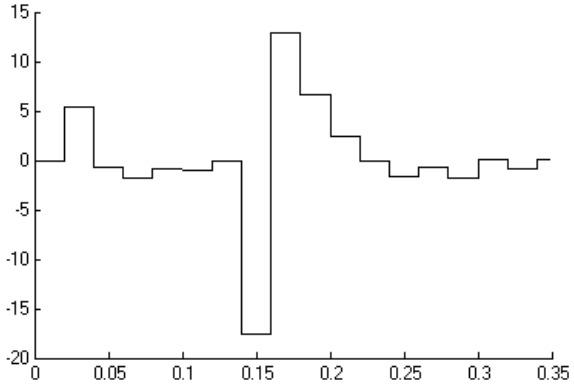

Figure 9-c. Phase detection error in case of voltage sag

The following segmented voltage function (13) represents an unbalanced three-phase voltage. Figure 10-a,b,c show the voltage and current in AC side, DC output and the error of phase detector. They also rapidly come to normal operation with the help of TDPLL.

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 311\sin(314t) \\ 250\sin(314t - 2\pi/3) \\ 311\sin(314t + 2\pi/3) \end{bmatrix}_{0.135\text{s} \le t \le 0.23\text{s}} \quad (13)$$

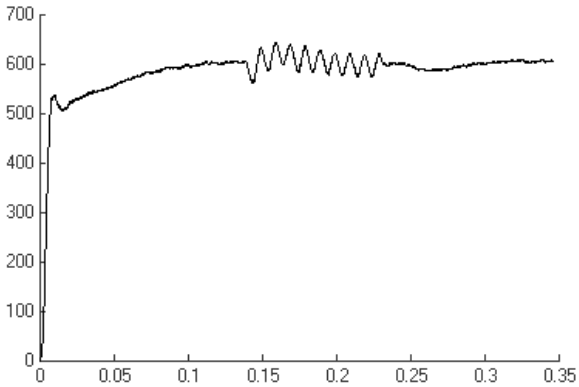

Figure 10-a. DC output in case of voltage unbalance

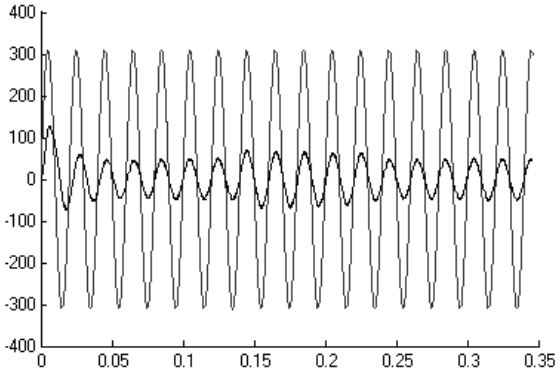

Figure 10-b. AC-side source voltage and inductance current in case of voltage unbalance

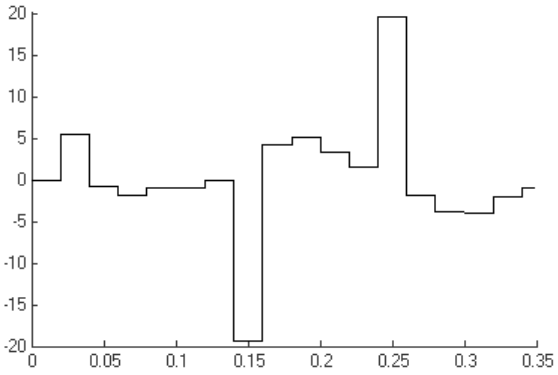

Figure 10-c. Phase detection error in case of voltage unbalance

5. Conclusion

The PLL technology is very useful for improvement of the power factor of three-phase SVPWM rectifier. A novel three-phase PLL solution is proposed based on the D-Q transformation and implemented digitally based on an FPGA platform. The TDPLL model is built with the Xilinx blockset integrated in Matlab/Simulink and then runs in the high-speed VHS-ADC simulation platform from Canada. The simulation and test results show the TDPLL is rapidly locked in case of different three-phase voltage disturbances. The soft PLL based on FPGA proposed is very suitable to the control of SVPWM rectifier with high parallelism and high power factor.

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