

Active voltage balancing strategy of asymmetric stacked multilevel inverter

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Article Info

Article history:

Received Feb 6, 2021

Revised Jun 26, 2021

Accepted Jul 7, 2021

Keywords:

Hybrid inverter topology
Multilevel converters
Voltage balancing strategy
Voltage Source Inverter

ABSTRACT

Multilevel inverters (MLI) play an important role in AC applications and are undergoing continuous development in topology and control. In higher levels inverters, conventional MLIs have high components count which calls for modification of these topologies to obtain the same number of levels with fewer components to reduce cost and size. Balancing of the capacitors voltages is crucial for the operation of the MLI and it becomes more challenging in higher levels. This paper presents an active voltage balancing strategy for a reduced switch count five-level topology which is the asymmetric stacked multilevel inverter (ASMLI). The ASMLI uses fewer components than the conventional MLIs when used in their five-level configuration. The proposed active voltage balancing strategy uses simple measurements and logic to assure a balanced capacitors voltages during steady state and transients. The performance was examined and compared based on two modulation techniques with LCL filter and RL load using MATLAB/Simulink. The results show that the active voltage balancing strategy can trace all capacitors voltages to the reference value simultaneously with less than 1% voltage error, fast dynamic response, and an acceptable total harmonic distortion (THD) which allows the proposed setup to be an available option for medium voltage applications.

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1. INTRODUCTION

In the last few decades, multilevel inverters became an appealing choice for electrical engineers in high power industrial AC applications due to its superior flexibility in output voltage and frequency, reduced filter requirements, lower dv/dt and lower switching losses with higher quality voltage and current waveforms than the standard two-level inverter [1]. Various topologies have been proposed by researchers throughout the years appropriate for different applications such as photovoltaic systems, flexible AC transmission systems (FACTS) devices, drive systems, etc [2]. Three types of these topologies were considered as conventional topologies which are cascade H-bridge (CHB) MLI, neutral point clamped (NPC) MLI and flying capacitors (FC) MLI [3], [4]. These topologies were commercialized and used in different industrial and power system applications, and it created a challenging race to invent new topologies and control schemes and to implement the most advanced control strategies in MLI to produce ultimate inverters for specific applications [5]. However as the number of levels increases the number of components needed and the control complexity increases [6] as well as preserving capacitors voltages becomes more challenging

due to unequal currents flow that charge/discharge the capacitors and the difficulty in controlling them, the matter that motivated the researchers to invent more topologies or combine them to create topologies with higher number of levels in lesser components [7]. Some of these topologies are active neutral point clamped multilevel inverter (ANPC-MLI) [8], stacked multicell converter (SMC) [9], cascade asymmetric multilevel converter (CAMC) [10] and T-type multilevel converter [11]. The control and modulation technique are very dependent on application [12], modulation techniques can be classified into low switching frequency [13]–[17] and high switching frequency [18]–[23]. Some solutions to capacitors voltage balancing problem are using separate DC sources or using external circuits to preserve the voltage, others are provided in [24]–[27]. In this paper, the main goal is to provide a robust voltage balancing strategy of the capacitors of a reduced switch count five level topology that combines a reasonable number of components with high quality waveform to be an available option for industrial and medium voltage applications. the ASMLI is based on the combination of three-level NPC MLI with a three-level FC MLI to form a five-level asymmetric stacked multilevel inverter fed from a common DC link which is suitable for medium voltage applications [28]. The proposed topology has less rating and fewer number of components for the same number of levels when compared to conventional topologies and a sufficient redundant state to efficiently control the voltages of the capacitors. The proposed active voltage balancing strategy functions the redundant switching states to preserve the capacitors voltages at the desired reference actively using only voltage measurements of the capacitors, current direction and simple logic. General steps of deriving the proposed balancing strategy are described to be derived for other MLI topologies. The performance of this setup is investigated based on two modulation techniques for comparison which are the phase-shifted pulse width modulation (PS-PWM) and level shift pulse width modulation (LS-PWM). The results show that the proposed voltage balancing strategy was able to preserve the capacitors voltages at the desired reference with less than 1% error on worst cases and able to readjust the capacitors voltages to a new reference in one electrical cycle.

This paper is organized as, section 2 presents the operating principles and structure characteristics of the proposed topology as well as the modulation techniques and the suggested voltage balancing strategy. In section 3, the robustness of this topology is proven by simulation results using MATLAB/Simulink. And the conclusions are drawn in section 4.

2. PROPOSED TOPOLOGY AND CONTROL SCHEME

2.1. Five-level asymmetric stacked multilevel inverter

The asymmetric stacked-five level inverter consists of 8 switches, 2 diodes, common DC contact capacitors, and two-level capacitors for each leg as shown in Figure 1. In this type of inverter, each pair of switches works complementary concerning each other to reduce control complexity. The capacitor's size should be equal to equally divide the voltage between them. The inverter can synthesize five voltage levels from nine switching states. Table 1 summarize all voltage levels of the possible switching states as well as the impact of each switching state on all four capacitors for the positive and negative load current. It can be noticed that there are seven states that has been discarded from Table 1. For the FC side, switches S1 and $\bar{S}2$ cannot be closed at the same time irrespective to other switches states also for the NPC side, switches S3 and $\bar{S}4$ cannot be closed at the same time as well. All states with the combination 10XX and XX10 should be avoided which leave four redundant switching states that can be used to balance the voltage of the capacitors. The current paths for all possible switching state are presented in Figure 2. This topology has the advantage of reduced rating and number of components compared to similar five levels topologies [29]. The semiconductor switches are all rated at $\frac{1}{4} V_{dc}$ except S1 and $\bar{S}2$ that should withstand $\frac{1}{2} V_{dc}$.

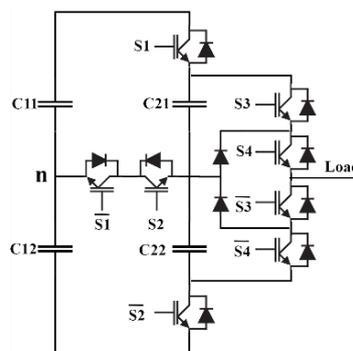


Figure 1. One leg of ASMLI

Table 1. Possible switching states with its effect on capacitors voltages

Output level	Possible state				Effect on C11		Effect on C12		Effect on C21		Effect on C22	
	S1	S2	S3	S4	IL>0	IL<0	IL>0	IL<0	IL>0	IL<0	IL>0	IL<0
-½ Vdc	0	0	0	0	N.E.	N.E.	C	D	N.E.	N.E.	N.E.	N.E.
-¼ Vdc	0	1	0	0	N.E.	N.E.	N.E.	N.E.	N.E.	N.E.	C	D
-¼ Vdc	0	0	0	1	N.E.	N.E.	C	D	N.E.	N.E.	D	C
0	0	1	0	1	N.E.	N.E.	N.E.	N.E.	N.E.	N.E.	N.E.	N.E.
0	0	0	1	1	N.E.	N.E.	C	D	D	C	D	C
0	1	1	0	0	D	C	N.E.	N.E.	C	D	C	D
¼ Vdc	1	1	0	1	D	C	N.E.	N.E.	C	D	N.E.	N.E.
¼ Vdc	0	1	1	1	N.E.	N.E.	N.E.	N.E.	D	C	N.E.	N.E.
½ Vdc	1	1	1	1	D	C	N.E.	N.E.	N.E.	N.E.	N.E.	N.E.

N.E. stands for no effect, C for charging and D for discharging

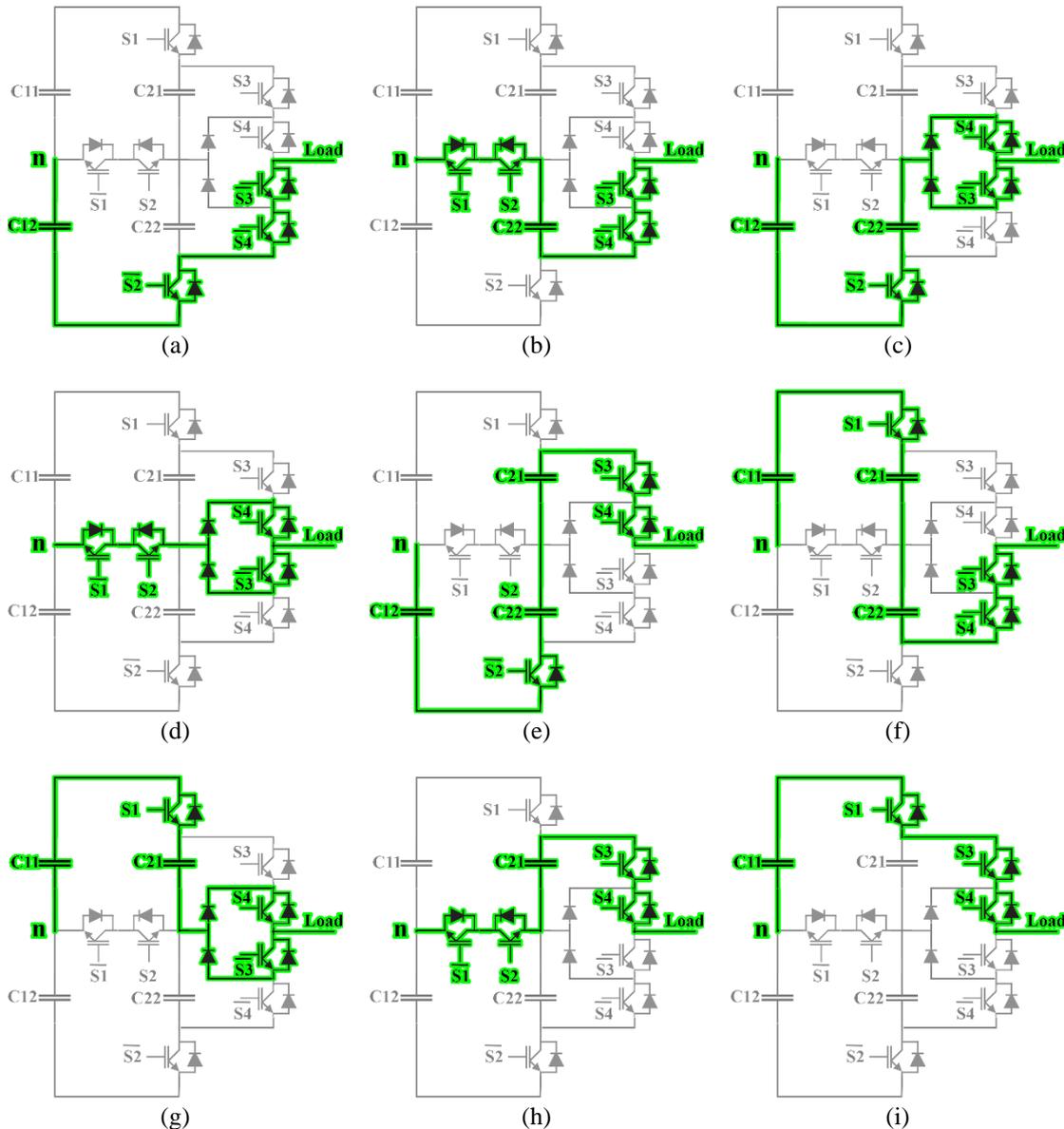


Figure 2. Current paths for all possible states; (a) -½ Vdc (0000), (b) -¼ Vdc (0100), (c) -¼ Vdc (0001), (d) 0 Vdc (0101), (e) 0 Vdc (0011), (f) 0 Vdc (1100), (g) ¼ Vdc (1101), (h) ¼ Vdc (0111), and (i) ½ Vdc (1111)

2.2. Modulation techniques

Two types of modulation techniques can be used in MLI, broadly classified as fundamental switching frequency techniques and high switching frequency techniques, the latter is used in this topology, specifically the sinusoidal pulse width modulation (SPWM) due to its simplicity and high performance.

A traditional SPWM can be extended to be used in Multilevel inverter by using (n-1) carriers, usually triangular (where n is the number of levels) with a frequency f_c that can be distributed in different ways [30] and compared with a reference sinusoidal signal in order to obtain gating signals that leads to the least distorted output voltage and current with minimum filter requirements and losses. In this paper two modulation techniques are used, PS-PWM and LS-PWM. In the first one a phase shift of $2\pi/N$ is applied to (n-1) triangular carriers to obtain the reference signal for the inverter whereas in the latter the carriers are distributed vertically to cover all voltage values and sub-classified into opposite phase disposition (OPD), in phase disposition (IPD), and alternate phase disposition (APD) depending on how the carriers are distributed. The LSPWM-IPD were reported to have better THD performance compared with LSPWM-OPD, LSPWM-APD and PS-PWM [22], [31]. At each instant of time a carrier is compared with the modulating signal with amplitude of M_a , each comparison gives (1) if the modulating sinusoid is greater than the triangular carrier and (0) otherwise. The results are added to give the command signal for MLI, which is required voltage at the output ports of the inverter.

2.3. Voltage balancing strategy

Multilevel inverters have a capacitors voltage unbalance problem, it will result in additional THD in output voltage and they may be damaged by overvoltage. The problem may be solved by the use of additional circuits to regulate the voltage or using separate dc sources. However, these solutions are not practical for most applications. The unbalanced capacitors voltage problem for the proposed topology can be solved by using the redundant switching states interchangeably without any additional components.

2.3.1. Proposed voltage balancing algorithm

The redundant switching states of ASMLI topology should be functioned to effectively balance the voltage of all leg capacitors. By inspecting each possible switching states and its effect on each capacitor's voltage in Table 1, the following steps are carried out to program an effective algorithm for this topology to balance the capacitors voltages. This algorithm is based on the measurements of the capacitor's voltages and the direction of the current with simple logic:

- Reference command signal is generated by comparing four carrier signals (number of levels-1) with reference modulation signal, five voltage levels are obtained (0, 1, 2, 3, and 4) each one corresponds to a specific ratio of Vdc ($-\frac{1}{2}$ Vdc, $-\frac{1}{4}$ Vdc, 0, $\frac{1}{4}$ Vdc and $\frac{1}{2}$ Vdc) respectively.
- Measure the voltage error of the capacitors by subtracting reference voltage from the actual voltage as well as indicate current direction.
- For the levels with no redundant states, the states are chosen straightforwardly because there is no other state. For the proposed topology, voltage levels ($\pm 1/2Vdc$) have no redundant states. On the contrary for the rest of the levels, a weighting between capacitors voltages is carried out to know which capacitor's voltage has a higher error voltage and should be corrected. It is done by comparing the error voltage of the capacitors that have a contrast charge/discharge characteristics in the stage to make a logical decision upon. For example, for positive load current in $-1/4Vdc$ stage, C12 and C22 have contrast characteristics and a weighting should be made to indicate which capacitor's voltage is to be corrected in the current PWM period.
- The optimal state is chosen to decrease voltage deviation of that specific capacitor i.e. charge it if the error > 0 and discharge it if the error < 0 .

Figure 3 and Figure 4 demonstrates the control scheme used for ASMLI topology where e_{xx} stands for error signal for the specified capacitor. The proposed voltage balancing strategy is analyzed and validated in simulation results.

2.3.2. Switching frequency vs. capacitors size

As stated before, redundant states can be used to effectively balance the voltage of the capacitors, however this strategy can be used further to reduce the size of flying capacitors, as the redundant states generate the same voltage levels, using the balancing strategy presented, the switching frequency can be increased to decrease the charge/discharge time of the capacitors, therefore; decreasing voltages deviation. And here a tradeoff can be made between the size of the capacitors versus switching frequency and therefore switching losses. The flying capacitors is dimensioned using the (1) [32]:

$$C_{fc} = \frac{I_{l,max}}{\Delta V_{fc} * f_{sw}} \quad (1)$$

where ΔV_{fc} is the allowed flying capacitor's voltage ripple and f_{sw} is the apparent switching frequency.

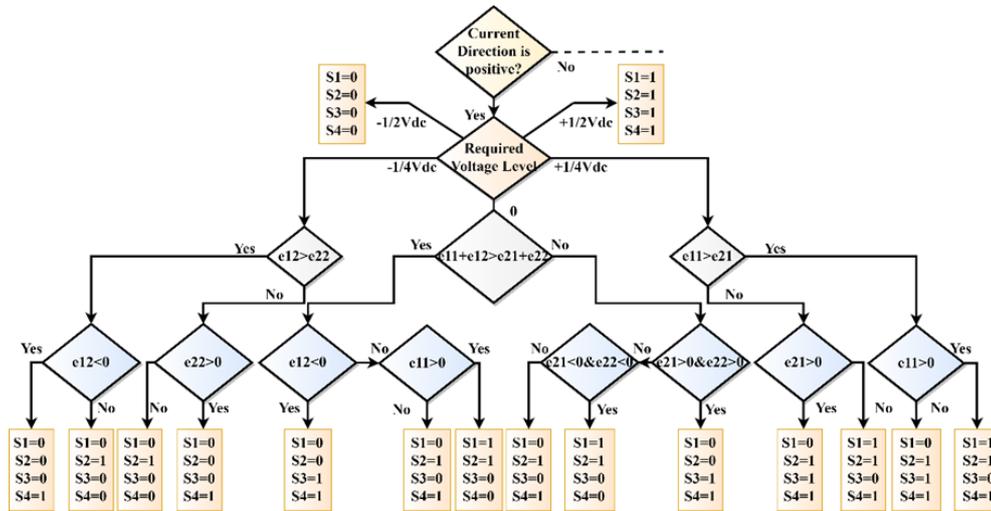


Figure 3. Decision making mechanism

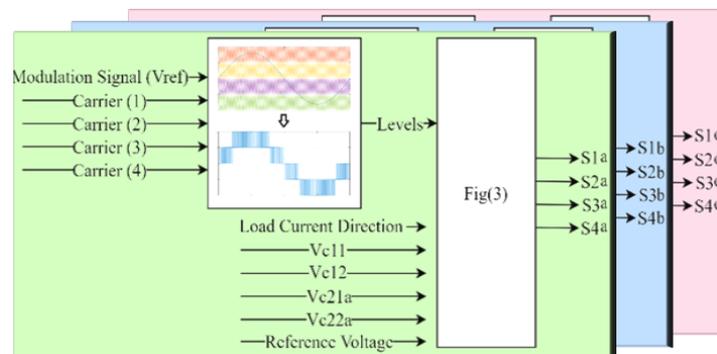


Figure 4. Block diagram of the proposed control scheme

3. RESULTS AND DISCUSSION

The performance of the proposed setup is investigated using MATLAB Simulink program, a three phase structure model in Simulink is constructed as shown in Figure 5, the simulation parameters are listed in Table 2. Two modulation techniques are used, PS-PWM and LS-PWM. The carriers intersection with the reference signal and the corresponding command signal for both techniques are shown in Figure 6. The command signal is sent to the voltage balancing algorithm to obtain the best switching combination for the inverter while keeping the capacitors voltages balanced. The output voltage is filtered using LCL filter designed based on [33]. Phase and line voltage waveforms are shown in Figure 7 and Figure 8. Fast fourier transform (FFT) analysis for phase and line voltages are shown in Figure 9 and Figure 10. Load current waveform and its FFT analysis are shown in Figure 11 and Figure 12.

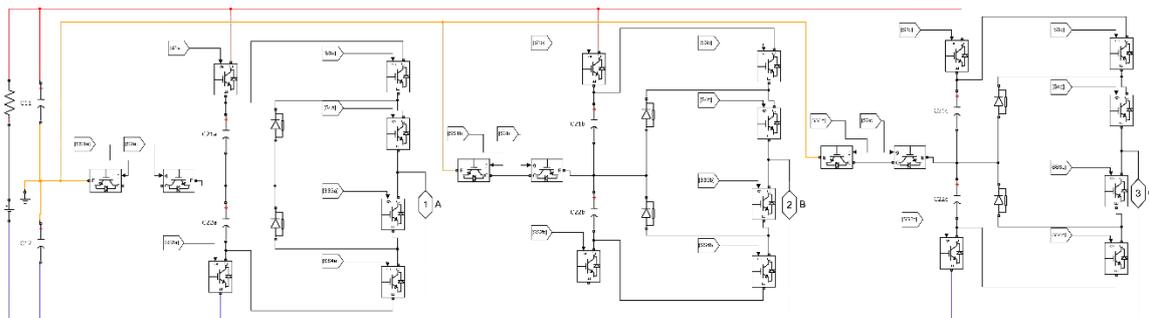


Figure 5. MATLAB/Simulink model

Table 2. Simulation parameters

Parameter	Value
System frequency	50 Hz
DC-link capacitors	2500 μ F
Flying capacitors	1300 μ F
DC voltage	600 V
Load resistance	5 Ω
Load inductance	2.28 mH
PS-PWM carrier frequency	1 KHz
LS-PWM carrier frequency	4 KHz
Modulation index	0.8
Filter capacitor	6 μ F
Filter inverter side inductor	2.1 mH
Filter load side inductor	2.1 mH

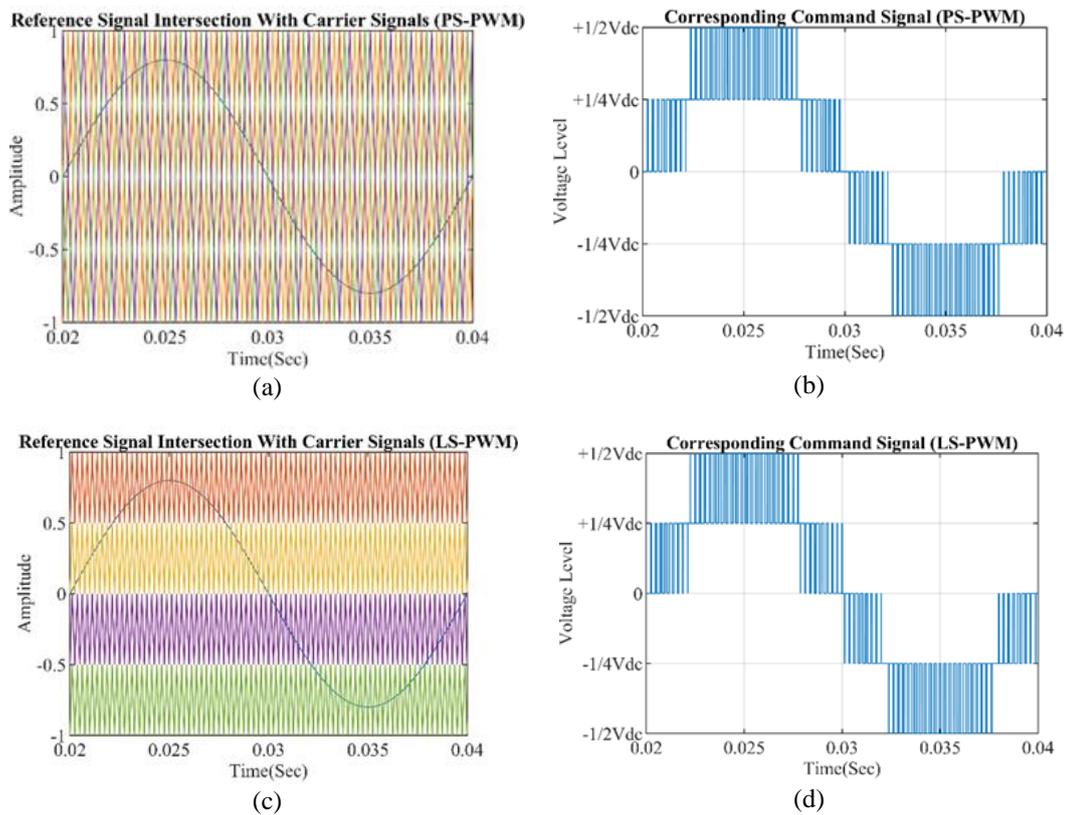


Figure 6. Reference signal intersection with carrier signal and the corresponding command signal; (a), (b) PS-PWM and (c), (d) LS-PWM

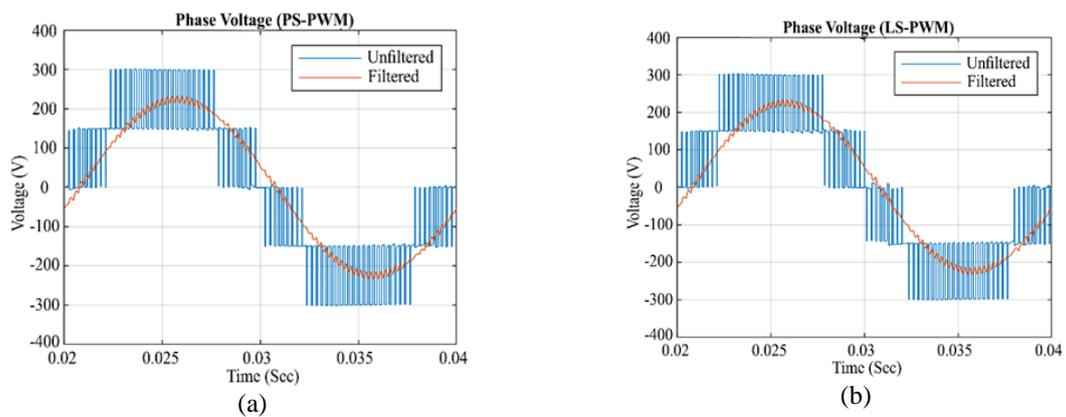


Figure 7. Phase voltage; (a) PS-PWM and (b) LS-PWM

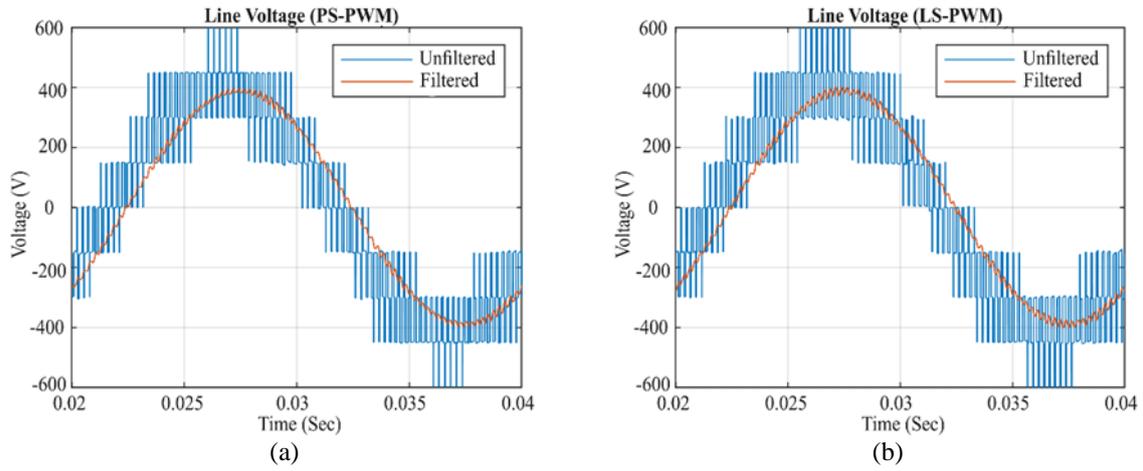


Figure 8. Line voltage; (a) PS-PWM and (b) LS-PWM

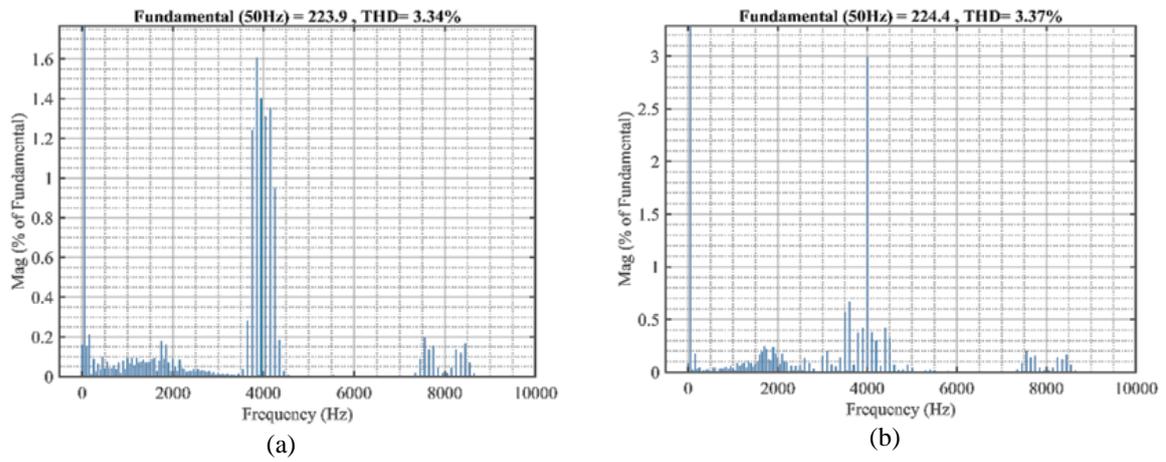


Figure 9. FFT analysis of phase voltage; (a) PS-PWM and (b) LS-PWM

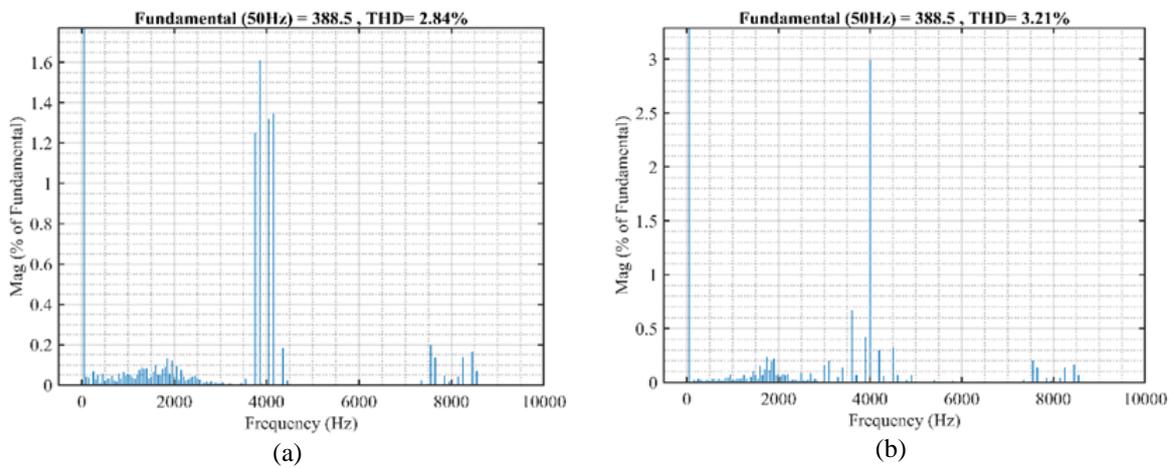


Figure 10. FFT analysis of line voltage; (a) PS-PWM and (b) LS-PWM

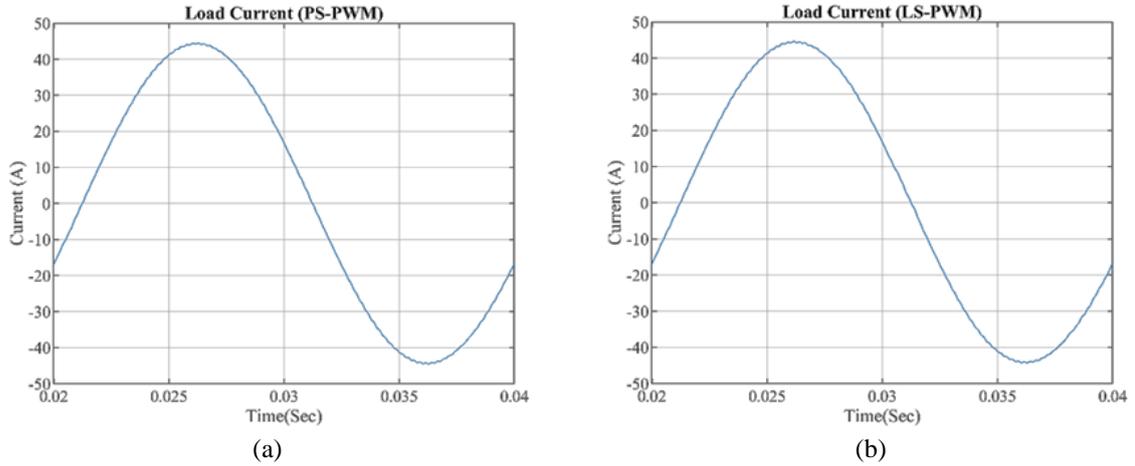


Figure 11. Load current; (a) PS-PWM and (b) LS-PWM

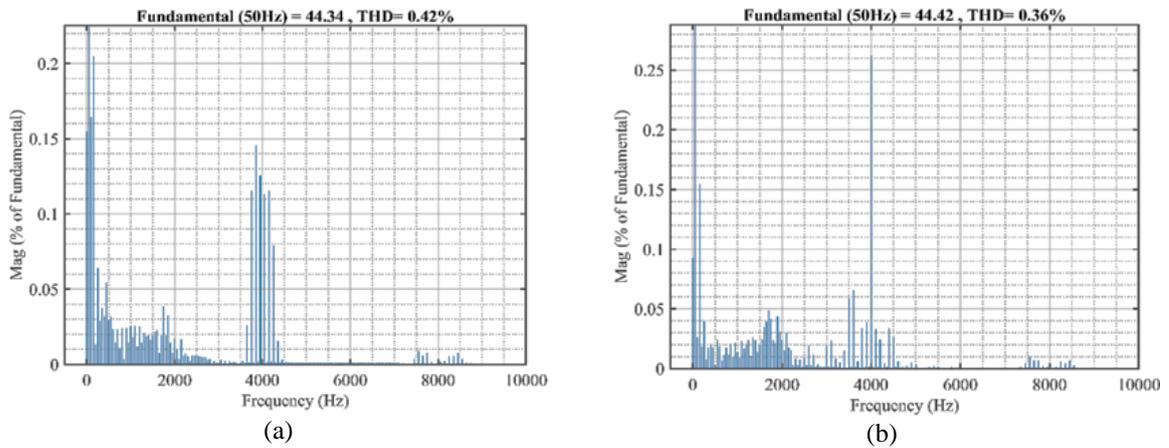


Figure 12. FFT analysis of load current; (a) PS-PWM and (b) LS-PWM

Source voltage is stepped from 600V to 3000V at the instant (0.05 sec) to imitate transient state and test the proposed balancing strategy dynamic response. Step response for one phase is shown in Figure 13.

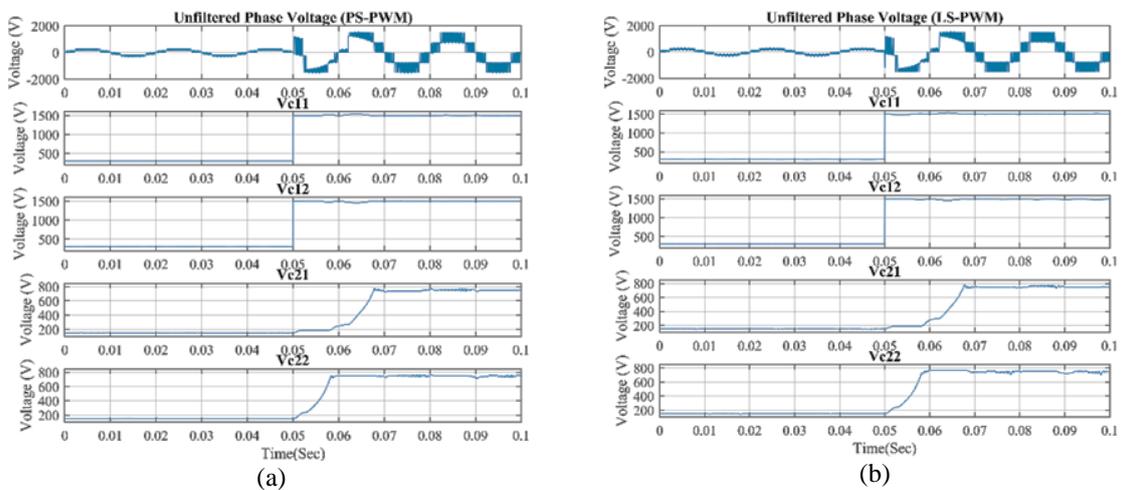


Figure 13. Capacitor voltages step response; (a) PS-PWM and (b) LS-PWM

Simulation results show an excellent performance and balanced capacitors voltages with acceptable voltage ripple of less than 1% in worst cases. The step response of V_{dc} shows that the capacitors take maximum time of one cycle to settle to the new reference voltage which reflects a good dynamic response. Both modulation techniques show a high waveform quality with a slight preference to LS-PWM due to lower THD in load current.

4. CONCLUSION

This paper proposed an active voltage balancing strategy for asymmetric stacked multilevel inverter. The ASMLI topology has reduced number of components and rating of semiconductor switches as compared to other five level topologies with redundant states that allows the proposed balancing strategy to be implemented. The proposed active voltage balancing strategy was derived for the ASMLI to keep the capacitors voltages at the desired reference with simple measurements and logic. The behavior of inverter under two modulation techniques were investigated and compared to each other with RL load. The inverter simulation results prove the robustness of the proposed topology and balancing strategy. Beside the less filtering requirements needed, the reduced rating and count of components for ASMLI with active capacitors voltages balancing is a clear advantage that allows this setup to be implemented in industrial and medium voltage applications in future.

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