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Research on the Key Technique of SPC Exchange Equipment Based on FPGA

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Abstract

In the program controlled exchange technology college course, the signal transmission and voice data exchange for the communication system were usually achieved by utilizing the program controlled telephone exchange equipment choosing MT8980 series chip as the processing core which was limited to the numbers of communication channels and inflexibility of information interchange manners. A variety of extern circuits, taking time slice generation circuit and tone signal generation circuit as examples, will even be required which directly causes the complexity of the whole structure. Considering the disadvantages referred above, a new method of SPC (Stored Program Control) exchange exploiting FPGA (Field Programmable Gate Array) is proposed in this paper. The time slice generation, signal tone generation, user calls, voice data exchange functions, as well as other secondary functions, were realized by applying the new approach which allows the further development through hardware in-system programming. The superiority of the means is furnished in the end via comparing the experimental data in detail.

Keywords*: FPGA, program controlled exchange, information process*

1. Introduction

The program controlled exchange experimental equipment choosing FPGA as the system core mainly contains host machine part and data processing and illustration part with the architecure as shown in Figure 1. The former primarily consists of central processing module which completes the functions of time slice signal generation, tone signal generation and data and communication command exchange among the 4-users terminals using FPGA core, 4-users module which imitates 4 real users phone including user line interface circuit, data storage and display module which stores call records imposing FLASH chip and in-time reveals each communication status on LCD, and extern output module which is connected with PC to transmit the call records information. The latter nationaly is a software running on PC and mostly implements the tasks of filtering, disposing and indicating the call records data coming from the hos machine. This paper emphsises on the achivement of program controlled exchange technique taking FPGA as the system kernel and the advantages comparing with the original technique [1-5].

1.1. Display and Control Module

Display and control module is made up of minimum embedded system and LCD module handling the principal functions of demonstrating each users operating state which is desicribed in table 1 on LCD as well as the calling telephone number and such parameters as waiting time length [6].

An instance is shown in Figure 2, where stamps black in H module column for user 1 and Z module column for user 2 which mean that user 1 is receveing ring-back tone after dialing and user 2 is in the situation of ringring.

1.2. Major Processing Module

As the system processing core, this module employs EP2C5Q208C8 which belongs to Altera corporation Cyclone II series chip with the help of PCM codec allocated with A/D part and D/A part and dual-tone multifrequency chip to realize the functions of time slice signal generation, signal tone production including dial tone, busy tone, ring back tone and vibration

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ring tone, the user call and communication command and voice data switch which is the SPC exchange crux through hardware programming [7].

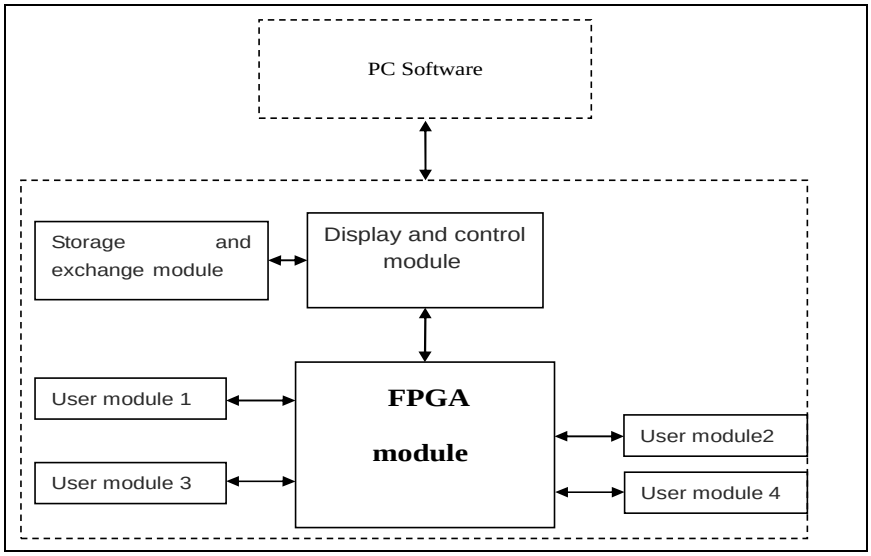

Figure 1. System architecture

Table 1. The Operating State Indication of Each Users

Character	Operating State Indication
G	On-hook
Z1	Off-hook
D	Wait
H	Ring-back tone
B	Dialing
Z2	Ringing
T	Call
M	Busy tone

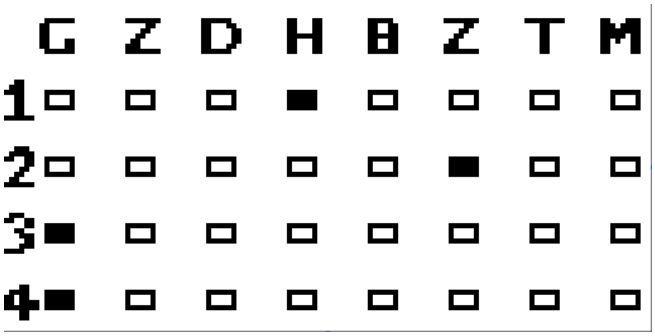

Figure 2. Operating state demonstration

1.3. User Module

This system presents four user modules to actualize the switching network function. The subscriber line interface circuit of SPC exchange generally possesses B (feed), O (overvoltage protection), R (ringing), S (monitoring), C (Encoding and decoding), H (mixed) and T (test) these seven functions. This circuit in this paper chooses a Legerity company AM79R70 chip which owns the advantages of current limit, on-hook transmission, reversal of polarity, TIP open

circuit, loop testing and other functions, while the encoding and decoding function of the system is executed by TP3067, a special encoding and decoding chip [8].

1.4. Data Storage and Exchange Module

This module contains two main functions: one uses FLASH chip to store records between any two users call which is able to store 1000 segments for each 4 users including the caller, the receiver, the communication time length and so on, another uses RS-232C serial interface to connect with PC in order to download system parameter configureuration and upload call data through software program [9].

1.5. Software on PC

Adopting VC++ in Visual studio program method, the software running on PC chiefly completes the inquiry and edit of call records and the ascertainment and settlement of call toll of which are listed below in detail [10]:

a) Set the users (4 in example) information: set the 4 users name, address, telephone number, system time and other information in the experiment system;

b) Set the system parameters: set the time parameter for non-dialing and non-answer;

c) Set the call toll: fixed toll and variable with different time interval are both available;

d) Set the transfer port: set the transportation rate and communication protocol for all the serial interface;

e) Operation for call data: “clear all the call data“, “delete the designated record”, “filter all the data”, “edit the appointed record”, “add a new record” and other operation for uploaded data and a brief analysis for the stored data ;

f) Download the configureuration information: handshake with the hardware of test box and download the software information such as users information and time information to the test box;

g) Upload the call data: handshake with the test box and upload the data stored in the test box to the database in PC;

h) Toll analysis: anaysis and calculation of user toll according to the different users, time interval and basic tariff.

2. Generation Method of Time Slice Signal and Signal Tone

FPGA module of the host mainly completes the functions of time slice signal generation, dual tone multiple frequency signal access and command signal and voice data exchange which is the SPC exchange key technique introducing Verilog HDL programming recipe. The original system commonly used analog circuit to generate signal tone including dial tone, busy tone, ring back tone and vibration ringtone, while this system adhibits FPGA + DAC chip scheme which takes on the strong augmentability and provides the possibility for further development. For instance, telephone conference, polyphonic ring tone and other additional application could be easily implemented by upgrading the program in FPGA without any modification for hardware platform [1-3].

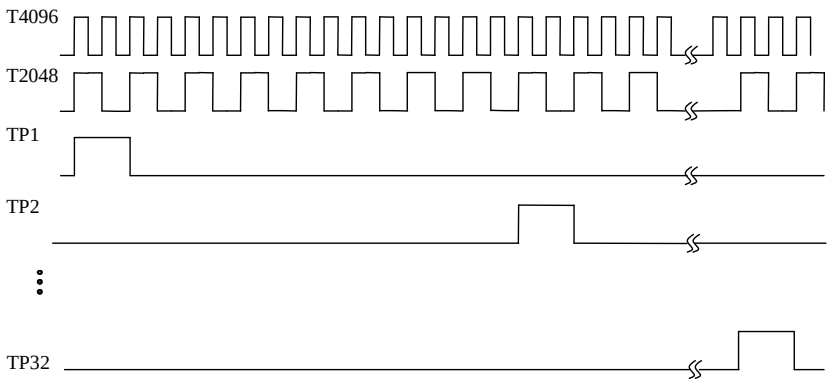

Figure 3. Time slice signal generation

2.1. Effect and Realization of Time Slice Signal

Main principle of the time division switching is to produce different time slice signal for every user module under the action of the main clock, each module transmits data information (including speech, signal sound, etc.) in different time slice. Time slice signal which is produced by FPGA according to the active crystal oscillator 4.096 MHz clock input is the core and foundation of the exchange system. As shown in Figure 3, FPGA chip produces T2048 main work clock and TP1 to TP32 a total of 32 channels time slice signal, who is delayed eight TP2048 clock which is used to transfer the users data. According to the SPC exchange standard, each 32 time slice form a big frame, which can transfer 32 channels signal at most. In this system the time slice TP1 to TP4 is distributed to the user 1-4 modules, TP5 to TP8 is allocated to each module DTMF dialing, TP9 is assigned to dial tone, TP10 is assigned to busy tone and TP11 is assigned to ring back tone [4].

2.2. Signal Tone Generation

In the light of SPC exchange criterion, signal tone such as dialing tone, ring-back tone, busy tone and vibration ring tone, which is engendered by the FPGA + DAC pattern with heavy flexibilty on producing some new signal tone like polyphonic ring tone through altering the configureuration program, is required to furnish the telephone terminal following the user operation accurately in each user module. The ASIC TP3067 is selected as the codec in this system due to the telephone switch applies 8-bit PCM code. The codec circuit for user 1 is given in Figure 4, where DR indicates the unified input serial data bus and DX sugessts the consolidate output serial data bus for modules which sent the data in distinct time slice, TPTS1 expresses the time slice for user 1, F-2048 denotes the globle clock and PCM1_IN remarks analog voice data input port.

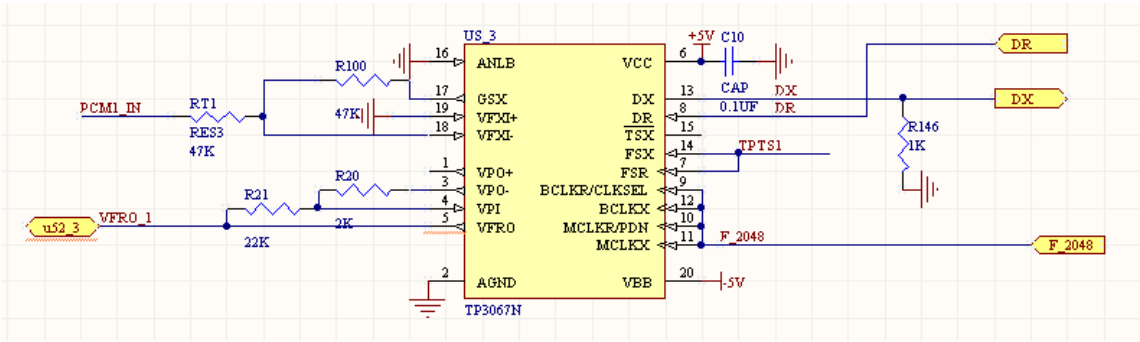

Figure 4. PCM codec circuit

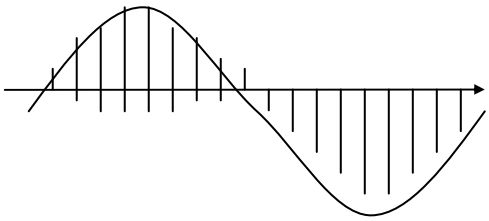

Figure 5. Sketch map of 450Hz sine wave sample

a) 450Hz sine wave generation

The four kind of signal tone referred former are all analog signal based on 450 Hz sine wave mostly which is the fundation of the system and generated using the FPGA+DAC mode, while DAC is achieved by PCM codec chip TP3067. The generation of sine wave uses cycle sampling method which divided a cycle of 450 Hz sine wave signal into 18 sampling point, as

shown in Figure 5.System samples the sine signal amplitude into a sequence of binary code according to A-law 13 line approximate nonlinear code law every 125 μs, then stores these binary code into the EEPROM in FPGA (Note: TP3067 code output, flips the value of a bit in even. For example + 2.5 V input should be 1111 1111, but TP3067 output is 1010 1010). When system requests producing the analog 450Hz sine wave, FPGA just needs to read the data in FLASH every 125 μs and output to the DAC chip under the action of the filter. An example of 18 samples output data in one period is shown in Figure 6.

Addr	+0
00	A1
01	C7
02	C6
03	A0
04	B0
05	D0
06	AC
07	D0
08	B0
09	A0
0a	C6
0b	C7
0c	A1
0d	B1
0e	D1
0f	AD
10	D1
11	B1

Figure 6. Original data stored in FLASH for one period

b) Synthesis of signal tone

All kinds of signal can also use digital way to be synthesized based on the production of the 450 Hz sine wave. The basic digital method to create a signal tone is: ①generate the 450Hz sine wave using the “a)” method; ②generate the ring back tone and busy tone on the base of the 450 Hz sine wave, the former is a combination of keeping the sine wave1 second on and 4 seconds off, while the latter is a periodic intermittent of 450 Hz sine wave every 0.25 second; ③ Vibration ring tone is a 25Hz square wave signal which can be directly generated by FPGA and transmitted to the user chip AR79R70 to be amplified for the service of user phone.

2.3. Access of Dual Tone Multi-frequency Signal

The first work of the SPC exchange is to dial to call others. DTMF (dual tone multiple frequency) method which allocated two different frequency for each button on the phone is widly employed in the current telephone system to complete the dialing process. In this SPC exchange system, every user modules are distributed to the independent DTMF unit all of which is composed of MT8870S monolithic DTMF receiving chip to receive the DTMF signal of the telephone users for amplification and filtering with the ilustration of Figure 7 and transformed to the parallel BCD code where indicated DTMFT1_1_I, DTMFT2_1_I, DTMFT3_1_I and DTMFT4_1_I. The FPGA stores the BCD code discrimination by DTMF module as the users call number and display it by LED on board.

2.4. Realization of Polyphonic Ring

Polyphonic ring means that, when other users are waiting to be connected, the ring-back tone will not be "beep ... beep ..." instead of some sweet music or a greeting.

In this system, we continue to make use of the basic generated principle of ring-back tone to produce the polyphonic ring: the system in advance stores 20 seconds digital music data

which is sampled every 125μs of the primeval music to be played and PCM coded using μ rate process, a total of 80,000 data. When polyphonic ring function is used, the system fetches a data in each frame during the original ring back tone gap and output followed by filtering and then the user will hear the music or greeting.

3. Achievement of SPC Exchange

Time division multiplexing is on the foundation of sample law which describes the possibility of recovering original analog signal from the corresponding time-dispersed sample pulse.Consequently time slice which could be used for transmitting other sample signal exists between the neighbour sample pulse when they hold a short cycle. Then several baseband signal could be transferred through one channel meanwhile and this is just the essential axiom of time division exchange.

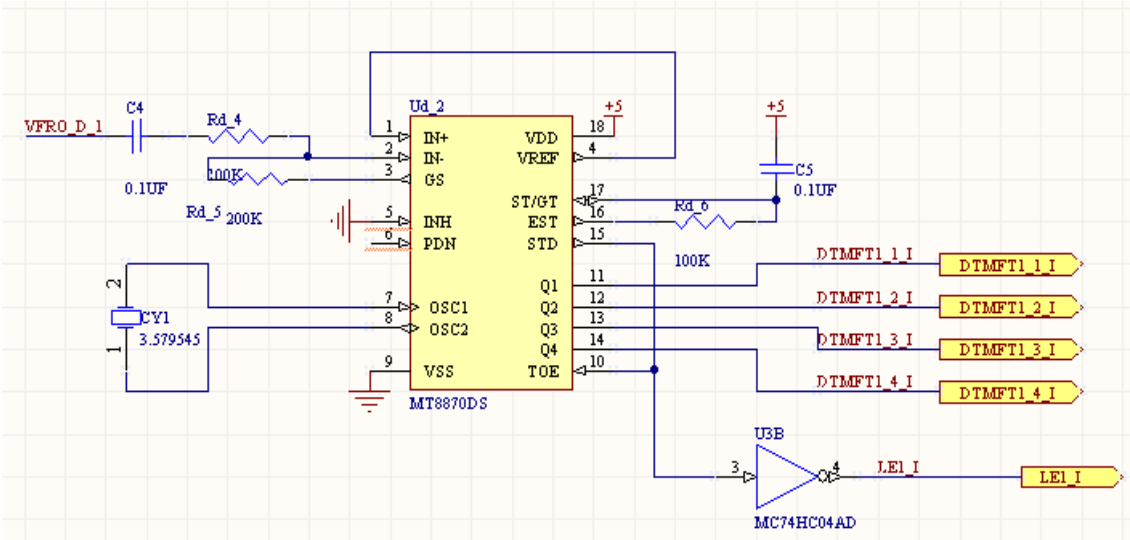

Figure 7. Circuit of DTMF

3.1. Accomplishment of Basic Exchange

This section will illustrate the FPGA implementation method of exchange process through an example user 1 calls user 2 with the detail below.

a) User 1 hooks off;
b) FPGA checks the hook off signal and send the dialing tone to user 1 terminal;
c) User 1 dials 4 times, each time of which send the 4-bit parallel BCD code analyzed by the DTMF detection module to FPGA;
d) FPGA identifies the integrated 4-bit dialing number and the information of user 1 calling user 2, then sends the ringring tone to user 2;
e) FPGA sends back-ring tone to user 1;
f) User 2 hooks off and FPGA starts to exchange the voice data with the detail that switching the voice data from the dispatch time slice of user 1 with the receiving time slice of user 2 and switching the voice data from the dispatch time slice of user 2 with the receiving time slice of user 1;
g) User 2 hooks on and FPGA sends the busy tone to user 1;
h) User 1 hooks on and the exchange procedure is over.

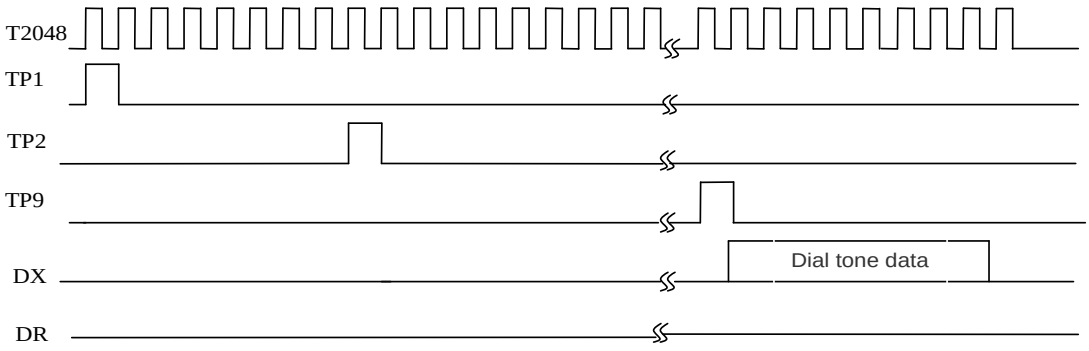

Figure 8. Initial status

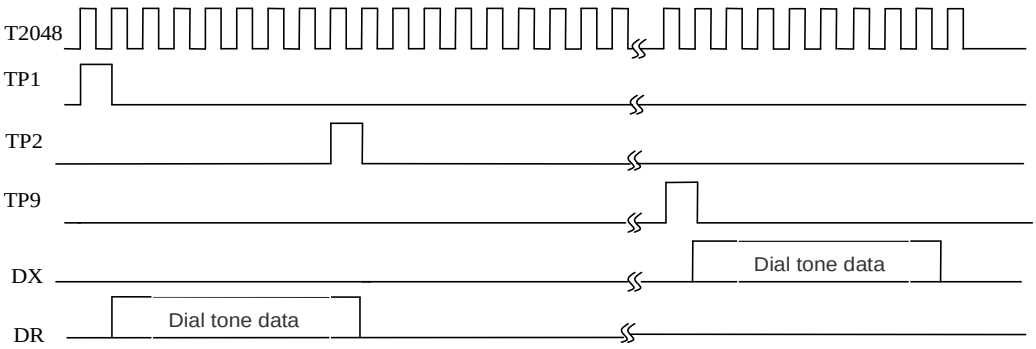

Figure 9. User 1 receive the dialing tone

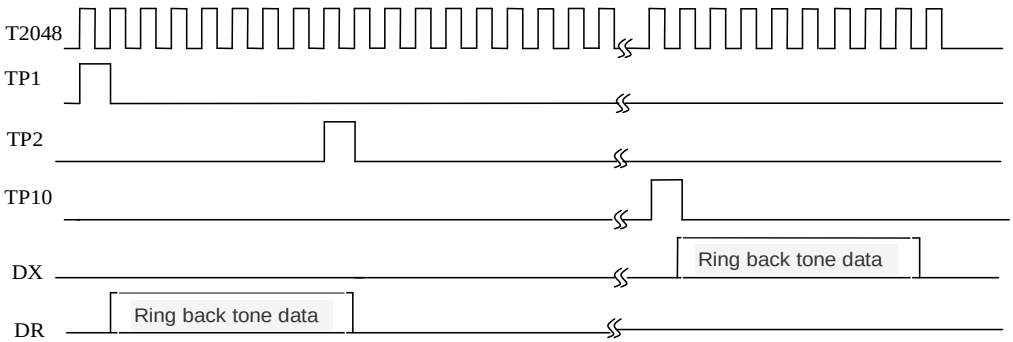

Figure 10. User 1 receive the back-ring tone

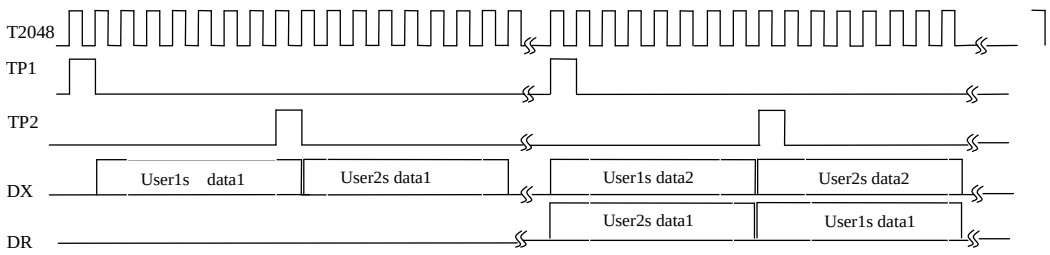

Figure 11. Voice data switch under the control of FPGA (the first frame data)

As shown in Figure 3, the T2048 is main working clock, TP1, TP2 is slot signals of the users 1,2, TP9 is the time slot of the dial tone, DX is a uniform serial output terminal (the output terminal connected to each user's module PCM encoded output), DR is the uniform serial input (the input terminal connected to the PCM encoded input terminal of each user module), all signal are produced by FPGA chip. First, when there is no user-hook, the data line DX only TP9 \ TP10 \ TP11 timeslot have respective output signal (dial tone, ring back tone, busy signal produced by FPGA (in accordance with the above method), while DR Online no signal, as shown in figure 8. When the FPGA detects user 1 is off hook, it copies the dial tone data in DX lineTP9 timeslot to the DR line TP1 timeslot, then the user 1 can hear a dial tone, all is shown in figure 9. FPGA continuously receive the four dialing code from the user 1 DTMF module and sent to determine the user 1 calls for user 2.

FPGA output 25Hz square wave ringing signal directly to the user 2 user module chip to drive the phone rang, at the same time copy the TP10 ring back signal data to the TP1 time slot, the user1 hears the ring back tone, illustrated in figure 10. When the user2 is off hook, the entire call process have been completed. Next the FPGA will complete voice switching process. In each successive frame of data, the FPGA will copy the data in DX Online TP2 timeslot (user2's voice data) to TP1 timeslot in DR line, the data DX Online TP1 timeslot (user1's voice data) to TP2 timeslot in DR line, so you can hear each other's voices, and the entire process is shown in figure 11. When one user hangs up, the FPGA stop this replication, the TP11S slot busy signal is copied to the other user's time slot, until both hang up, as shown in figure 12. In the entire exchange process described above, FPGA completed the entire work to the advantage of its good programmability.

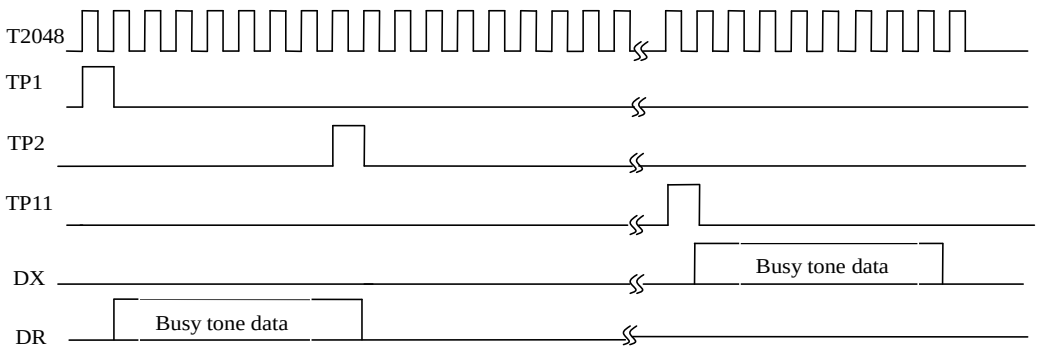

Figure 12. User 2 hook on

3.2. Actualization of Expanded Functions

Using FPGA as the core of the signal and data exchange, the system could easily completes the additional features such as conference call and the multi-party call. Conference calling can also be more convenient, such as three-way calling feature, after the completion of the call, the user1's voice signal is sent to the user2 and user3's time slot, the voice of the user 2 is sent to the user3 and user1's time slots, and so on, then complete a multi-voice switching function.

4. Result Explication

The primary function of the designed SPC exchange equipment is preferably fulfiled and the test result of PCM codec, signal tone generation and ensemble switch effection utilyzing FPGA is analyzed to certify the superiority of this system compared with the traditional one.

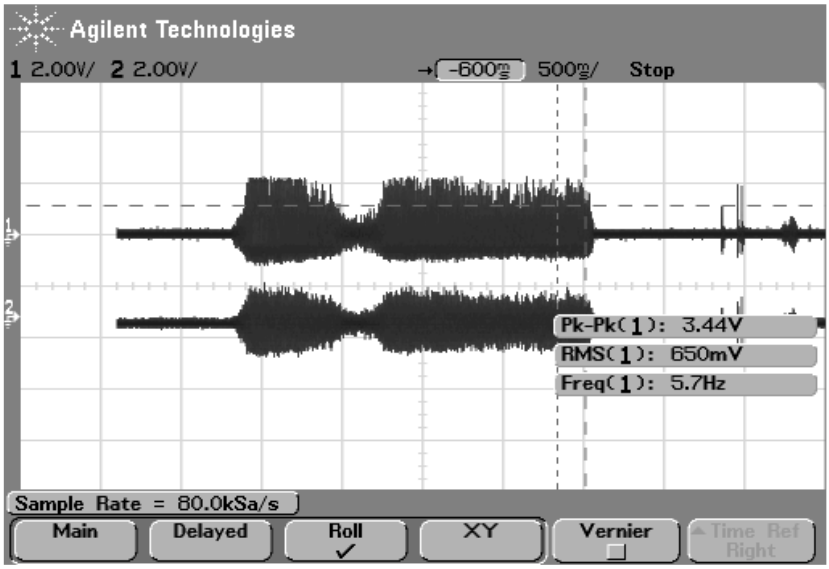

Figure 13. Comparision of sending voice signal and receiving voice signal

4.1. Analysis of PCM Codec Experimental Data

Analog signal should experience three transversion which are sampl, quantization and code in the code circuit to transform to digital signal with two common law which are μ law 15 polyline approximate transition mostly adopted in PCM-24 system and A law 13 polyline approximate transition employed in general 8-bit PCM code like this system. This paper exploits the FPGA + DAC scheme to emerge the analog signal and the FPGA + ADC approach to digitalize the analog signal which is the source of 8-bit PCM code in FPGA. A case of PCM coding and decoding is presented in figure 13, where drawing 1 indicates the original analog voice signal of user 1 during the communication procedure between user 1 and user 2 while drawing 2 illustrates the received analog signal of user 2 after being processed of ADC, data switch and DAC, moreover it is obvious that the two voice signal or DTMF signal generated by the buttons hold the same waveform only with some difference on amplitude. Coded by the TP3067 chip, the user 1 analog signal or DTMF signal is transmitted to the switch network which sends the transacted signal to user 2 who finishes the decoding and digitalization work.

4.2. Analysis of the Generated Signal Tone Experimental Data

a) Test data for dialing tone

Figure 14 sugessts the user 1 dialing tone waveform under the practical measurement, which acquires the signal processed by low pass filtering to the periodically 18 native data stored in EEPROM internal FPGA and calculated in accordance with the TP3067 compress rule. Due to the little disturbance and stable frequency, the user terminal could obtain such a distinct dialing tone. When the user hooks off under the promption of dialing tone for 20 seconds without dialing operation, the system will stop the dialing tone and send the busy tone.

b) Test data for back-ring tone

Figure 15, where balck zone intimates that 450Hz sine signal with 450 period which means one second is on, illustrates the user terminal waveform of back-ring tone which controls the 450Hz sine wave on-off under the practical measurement, and the telephone terminal will pronouce the “du.. du..” tone after amplifying the back-ring tone.

c) Test data for busy tone

Figure 16, where balck zone indicates that 450Hz sine signal with 450 period which means one second is on, expresses the user terminal waveform of busy tone which controls the 450Hz sine wave on-off under the practical measurement, and the telephone terminal will pronouce the “du.. du..” tone after amplifying the busy tone.

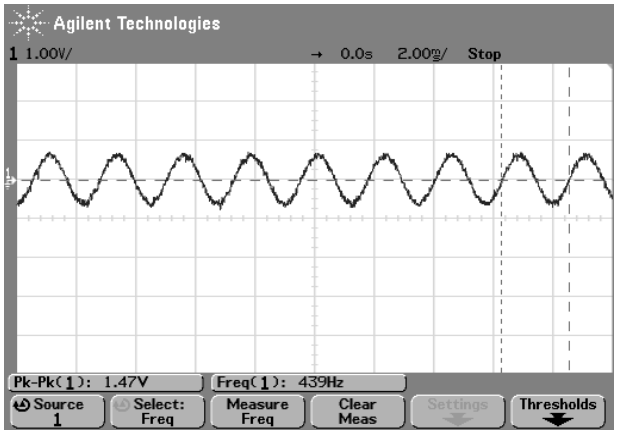

Figure 14. Test waveform for dialing tone

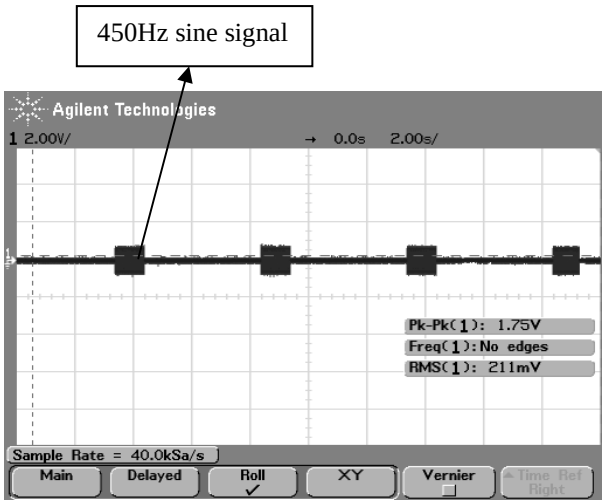

Figure 15. Test waveform for back-ring tone

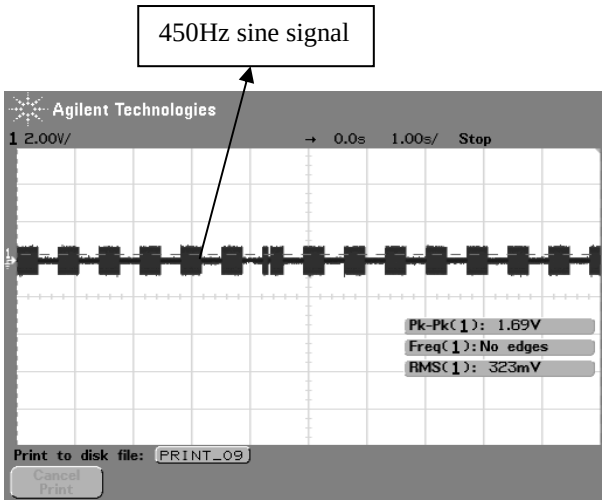

Figure 16. Test waveform for busy tone

d) Test data for vibration ring tone

The vibration ring tone is a 25Hz low frequency cycle signal which is combined with 1 second on followed by 4 seconds off. Figure 17 hints the vibration ring tone waveform for 1s on which contains 25 square wave of 25Hz low frequency. This tone, which is clear, simple and effective, is directly sent to the user terminal chip AM79R70 and transferred to the user phone after being amplified in the end.

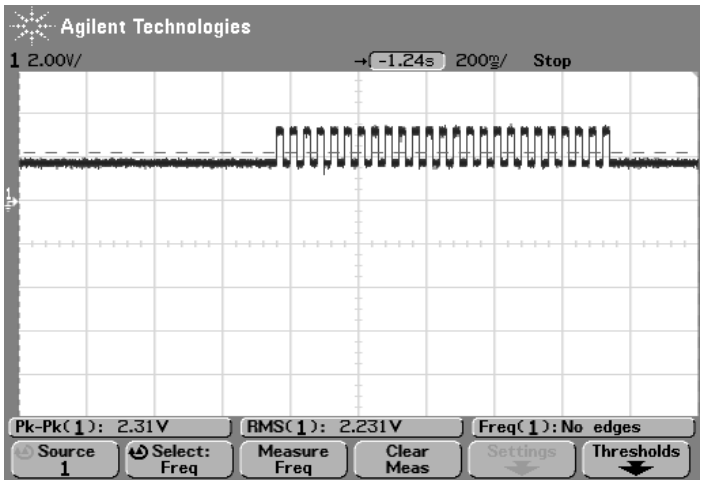

Figure 17. Test waveform for vibration ring tone

4.3. Contrast FPGA Exchange Technique with the Traditional Measure

The SPC exchange technology based on FPGA is a technique reconciled the time slice signal generation, signal dialing generation, communication command switch and voice data exchange with a great progress compared with the traditional means based on MT8980 which required additional MCU to program the MT8980 so as to realize the function of signal switch, furthermore the time slice signal generation has to make use of discrete digital circuits and this will make components cost and PCB area increase heavily once raising the user number. The detailed contrast is shown in table 2.

Table 2. Contrast of SPC exchange technique

Content	Based on FPGA	Based on MT8980
Time slice generation	FPGA generate together	Generate by discrete circuit individually
Basic signal tone generation	FPGA + DAC	Additional signal generation circuit
Signal and voice data switch manner	Achievement by FPGA program	Additional controller MT8980
User number increase	Easy	Exist limitation
Realization of additional function	Easy	Difficult
System device quantity	Few	Many
System PCB area	Small	Large
Cost	Low	Middle

5. Conclusion

Innovation of the system is to use the FPGA replace the special chip and analog circuit to generate signal and data exchange in the completion of the program-controlled telephone exchange, PC software supports the data analysis capabilities of the entire system more perfect. The signal tone produced by FPGA is clear and reliable, system signal and voice data exchange is correct flexible. The entire system design concept is innovative, easy to further development and has a good application prospect.

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