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Magnetic sensitivity modeling of dual gate MOS transistor

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ABSTRACT

In this paper, the magnetic field effect on the carrier transport phenomenon in the double gate metal-oxide-semiconductor field-effect transistor (MOSFET) has been investigated. This is done by exploring the Lorentz force and the behavior of a semiconductor subjected to a constant magnetic field. The magnetic field modulates the electrons position and density as well as the potential distribution in the case of silicon tunnel tunneling field-effects (FETs). This modulation impacts the device electrical characteristics such as ON current (I_{ON}), subthreshold leakage current (I_{OF}), threshold voltage (V_T), magneto-transconductance (g_{mm}) and output magneto-conductance (gm_{DS}). In addition, a hall voltage (V_H) is induced and modulated by the magnetic field. It has been observed that this voltage influences the effective applied gate voltage. It has been observed that the threshold voltage variations induced by the magnetic field is of paramount importance and affects the device switching properties both speed and power dissipation, noted that the threshold voltage V_T and (Ion/Iof) ratio are reduced by 10^{-3}V and 10^2 for a magnetic field of ±6 and ±5.5 Tesla, respectively. We have simulated the different behavior in the channel, mainly doping concentration, potential distribution, conduction and valence bands, total current density, total charge density, electric field, electron mobility, and electron velocity.

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1. INTRODUCTION

With the miniaturization of semiconductor technology, nanoscale integrated circuits have become very sensitive to the external magnetic field. Among the first measurements of the hall effect in silicon was made by Wick [1] on rather impure samples. Other studies were carried out by Shockley and Pearson [2] and by Putley and Mitchel [3], exploiting the hall effect on monocrystalline silicon with low impurities.

In the field of microelectronics technology reported parasitic effect on the external electrical characteristics in the field effect transistors metal-oxide-semiconductor field-effect transistor (MOSFET) [4]-[7], a few research has also motivated exploring the presence of a magnetic field in the carrier transport phenomena in any substance carrying current, and thus also in the active region of semiconductor devices especially in the technology of complementary metal-oxide-semiconductor (CMOS) field-effect transistor [8], [9]. The downscaling of dimensions of conventional MOSFETs at the nano-scale [10]-[12] is known to have a high magnetic sensitivity to the magnetic field [13], [14] because of the low active channel area. This leads to complicated various short channel effects (SCE) such as the effect of hot carriers effect, threshold voltage

roll-off, substrate carrier effect, higher change in hall voltage and drain-source resistance (R_{DS}) in the linear region [8], [13], [15], [16].

Experimental of several case studies indicate that the magnetic field induced current deflection on the drain-current voltage and changing the conductivity of the active region [17], induces asymmetrical magneto tunneling conductance in MOSFETs resulting of non-homogeneous space mechanical strain [18], [19]. The magneto-transconductance of N-type metal-oxide-semiconductor (N-MOS) transistors exposed to the external magnetic field B=7T and 14T is reduced by 7% and 28% respectively due to the current reduction that comes from the deflection of the current lines inside the channel consequently of the Lorentz force acting to the current [14], [20]. However, no research has been performed on the topic, certainly because the applications of such a very high field are limited.

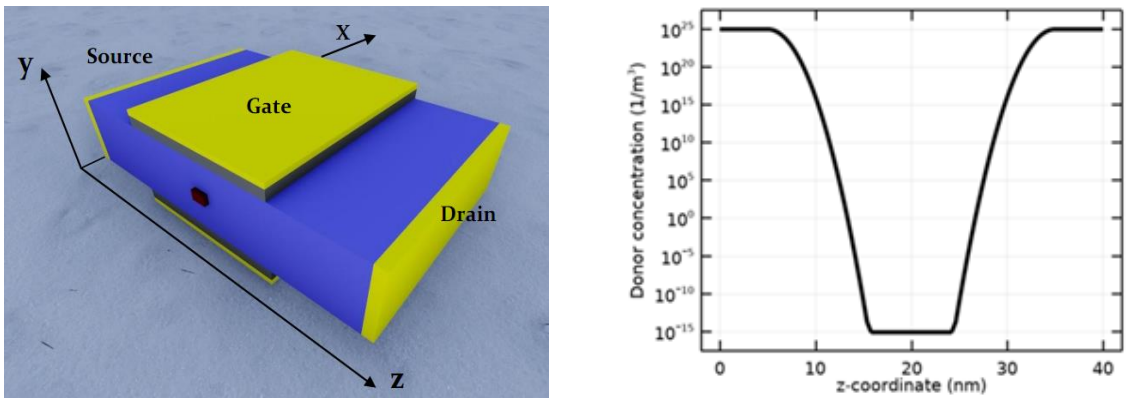
The simulation of hall effect devices is relatively new, started in the 1980s [21]-[23], and has helped to analyze and understand the operation of the hall-effect in complex devices such as integrated circuits. The aim of this article is an analysis of advanced CMOS integrated circuits at the nanoscale and their sensitivity to the external magnetic field. Their performance can be seriously impaired and thus result from unforeseeable malfunctions. In the case of vehicles and machines controlled by these circuits, control is systematically lost.

To remedy this, control of the effects of the external magnetic field on the operation of these circuits must be controlled. This control involves the quantification of these noises, their analysis, and their impact on the functioning of the circuits. For this, the double gate metal oxide semiconductor field effect transistor (DG MOSFET) transistor was considered and modeled by the finite element method, while taking into account all the effects of carrier transport in semiconductors under an external magnetic field. The results show excellent accuracy, comportment and good agreement compared with that obtained in the experimental study of MOSFETs technology.

2. DEVICE STRUCTURE AND PHYSICS

The structure of the device studied in our simulation is illustrated in Figure 1(a). The applied magnetic field B=(0, By, 0) is considered perpendicular to the current flowing between the two contacts drain and source oriented along the y-axis. The current density flowing through the silicon channel is along the z-axis. Two open circuit hall1 and hall2 rectangular contacts are provided for the detection of the hall voltage V_H, made on the DG MOSFET structure are placed perpendicular to the y-direction. The S (source), the D (drain) and the G (gate) are bias contacts. The length of the channel is L=20nm, its width is W-28nm. We assumed an enhancement n-type channel device. We shall denote the drain to source voltage by V_D, the gate to source voltage by V_G, and the threshold voltage by V_T.

Figure 1(b), illustrates the type of doping profile for the silicon DG MOSFET. Note that the electron concentration is highest in the source and drain extension contacts. The concentration is reduced past the limits of the source and the drain to the channel doped with acceptor impurity. The doping profile is a very important criterion in MOSFETs because it tells us about the desired drain current levels and the strength of the electric field in the device. The details of the device's physical parameters used in the structure are shown in Table 1.



(a) (b)

Figure 1. (a) Represent the schematic structure of an n-channel DG MOSFET and (b) show the impurity doping profile in the channel of Si DG MOSFETs

Table 1. Values of various parameters used in the simulation

Symbols	Parameters	Values
N_a	Impurity doping in the channel	$10^{14}cm^{-3}$
N_d	Impurity doping in source and drain	$10^{18}cm^{-3}$
t_{si}	Silicon film thickness	10nm
L_S ,L_D	Length of source and drain Oxide thickness	5nm
t_{ox}	Oxide thickness	2nm
$T^{'}=t_{si}$	Channel thickness	10nm
ε_0	Permittivity of vacuum	$8.8*10^{-12}F/m$
ε_{si}	Permittivity of silicon	$11.85*\ \varepsilon_0$
ε_{ox}	Permittivity of oxide	$3.9*\ \varepsilon_0$
T	Absolute temperature in Kelvin	300K
Φ_M	Metal work function	4.6eV

If a constant magnetic field, B is applied along a perpendicular to the direction of drain current, the Lorentz equation will be used to describe the hall effect in silicon DG MOSFETs [13]

$$m^* \frac{d^2r}{dt^2} + \frac{m^* dr}{\tau dt} = (-e)[E + (v_d \times B)] \quad (1)$$

here m^* is the cyclotron effective mass, r is the position, and τ the average (recombination) lifetime of the electron. v_d is the velocity at which electrons move through the hall effect. E is the electric field applied in a direction provided by the polarization contacts of the transistor. Then the hall field, ξ_H produced by the hall effect is given by [24],

$$\xi_H = \left(\frac{p{\mu_p}^2 - n{\mu_n}^2}{e(p\mu_p + n\mu_n)^2}\right)\left(\frac{I_D}{W.T'}\right)B_T \quad (2)$$

In case of n-type channel MOSFET, the drain current I_D is entirely carried by majority carriers, electrons consequently, $n\mu_n \gg p\mu_p$, thus (2) can be written as [17],

$$\xi_H = \left(\frac{-1}{en}\right)\left(\frac{I_D}{W.T'}\right)B_T \quad (3)$$

At low drain voltage V_D, in the linear region of operation of a MOSFET, $V_D<V_G-V_T$. The area density of carriers in the channel is approximately constant over the channel. This charge density is given by,

$$Q_{ch} \simeq C_{OX}(V_G - V_T) \quad (4)$$

where C_{OX} denote the gate oxide capacitance per unit area. The drain current I_D is given by [25],

$$I_D = 2\mu_{ch}C_{OX}\frac{W}{L}(V_G - V_T - V_D/2)V_D \quad (5)$$

so, I_D can be written as [26],

$$I_D = gm_{DS} \times V_D \quad (6)$$

where gm_{DS} is the channel conductance for$V_D \to 0$. The channel conductance is given by [25],

$$gm_{DS} = \frac{\partial I_D}{\partial V_D}\Big|_{V_G} = \mu_{ch}\frac{W}{L}\frac{8\varepsilon_{si}}{t_{si}}\frac{kT}{q}\beta_D \tan\beta_D \quad (7)$$

where μ_{ch} denotes the drift mobility of carriers in the channel, $\beta_D$is value at the drain, q is the electron charge, n_i is the intrinsic carrier density.

At higher drain voltage V_D ($V_D \leq V_G - V_T$), the carrier's charge density in the channel continuously decreases with increasing distance from the source. The drain current is generally given by [25],

$$I_D = \mu_{ch} \frac{W}{L} kT\, n_i\, t_{si}\, e^{q(V_G - \Delta\phi)/kT\left(1-e^{-qV_D/kT}\right)} \quad (8)$$

Channel conductance gm_{DS} in saturation region is given by [26],

$$gm_{DS} = \frac{I_D.\lambda}{1+\lambda.V_D} \cong I_D.\lambda \quad (9)$$

In long channel MOSFETs$\lambda \approx 0$, therefore$gm_{DS} = 0$. So, effect of magnetic field on the short channel MOSFETs, $\lambda \neq 0$ thus very minor effect may be observed when the drain voltage reaches the value $V_{DSat}=V_G-V_T$.

The charge density at the drain boundary of the channel is practically reduced to zero, which corresponds to the pinch point. Beyond the pinch point, the current remains practically constant. The drain saturation current is given byI_{Dsat} (V_{Dsat}) according to (8). The hall voltage of MOSFET is in the form [8],

$$V_H = G_H \frac{r_H}{Q_{ch}} I_D B_\perp \quad (10)$$

Recalling that Q_{ch} given by (4), G_H denotes the geometric correction factor and r_H the hall factor. In semiconductor physics, the classical model of carrier transport [27], [28] is based on continuity equations. In order to have a complete description, we would also need to take into account the following partial differential equation,

$$-\nabla.(\varepsilon \nabla V) = q(p - n + N) \quad (11)$$

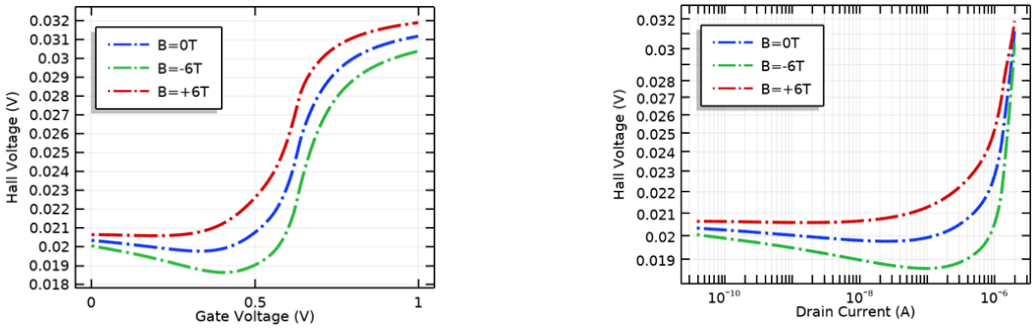
where V: denotes the electrostatic potential, ε: is the electrical permittivity of the material, q: is the electronic charge and $N=N_D-N_A$ is the fully ionized net impurity distribution. The solution of the Poisson in (11) is the electrostatic potential V. The discretization of the Poisson equation, the continuity equations of electrons and holes are necessary and a coupled method, which is a generalization of Newton's method, is used to calculate the initially proposed system by a numerical iterative method. And in order to express the impact of the magnetic field in the device, by solving and rewriting the usual D-D (drift-diffusion) model of carrier's densities taking into account the terms depending on the magnetic field emitted by the effect of the Lorentz force on the carriers.

3. RESULTS AND DISCUSSION

Figure 2(a), shows the variation of the hall voltage V_H induced on the surfaces of the hall contacts as a function of the gate voltages V_G applied to the gate (G) for three values of the applied magnetic field when existence (B=+6 and -6 Tesla) and absence (B=0 Tesla). We notice in the stationary state (Vg=0), the hall voltage is almost the same for the three values of the magnetic field. When the transistor has been biased, the hall voltage increases or decreases gradually and asymmetrically with respect to the zero-field (B=0 Tesla) depending on the direction of the applied magnetic field, and the hall voltage increases or decreases rapidly for higher values of gate voltage V_G Until saturation, when the migration of electrons on the hall walls stops.

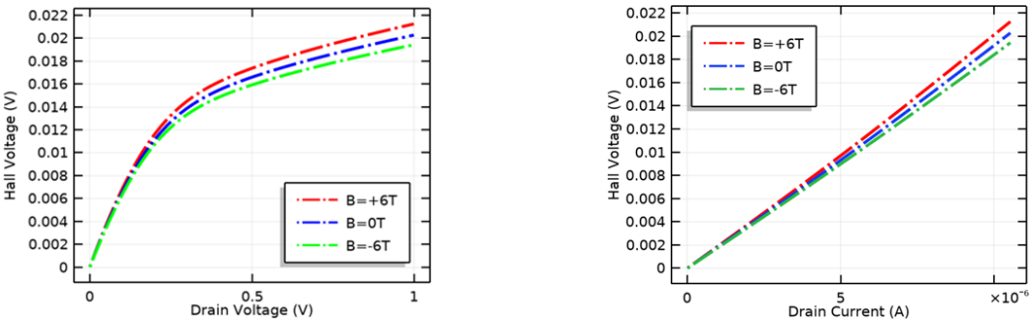
Figure 2(b), shows the variation of the hall voltage V_H as a function of the drain current I_D flowing under the drain and the source contacts developed by the gate voltages V_G applied to the gate contact (G) for three values of the applied magnetic field, B=+6, B=-6 Tesla and B=0 Tesla. We can see that in the quiescent state (Vg=0), the hall voltage is almost the same value for all three values of the magnetic field. As the gate voltage increases, the hall voltage increases or decreases gradually and asymmetrically with respect to the zero field (B=0 Tesla) depending on the direction of the applied magnetic field, and the hall voltage increases or decreases rapidly after just the threshold voltage V_T. For higher values of the bias voltage V_G hall voltage follows the same evolution until stability in the saturation region.

The hall voltage versus drains voltage and hall voltage versus drain current characteristics of the DG MOSFET surface recombination transistor is shown in Figure 3(a), and Figure 3(b), respectively, if the carriers are deflected towards the hall2 recombination surface, their concentration in the transistor channel decreases and the current also decrease. If the carriers are deflected towards the hall1 recombination surface, their concentration in the channel of the transistor increases, and the drain current also increases. This explains the difference in the hall voltage on the two surfaces of the hall1 and hall2 contacts. Therefore, this magneto-transistor is sensitive to the sign of the applied magnetic field.



(a) (b)

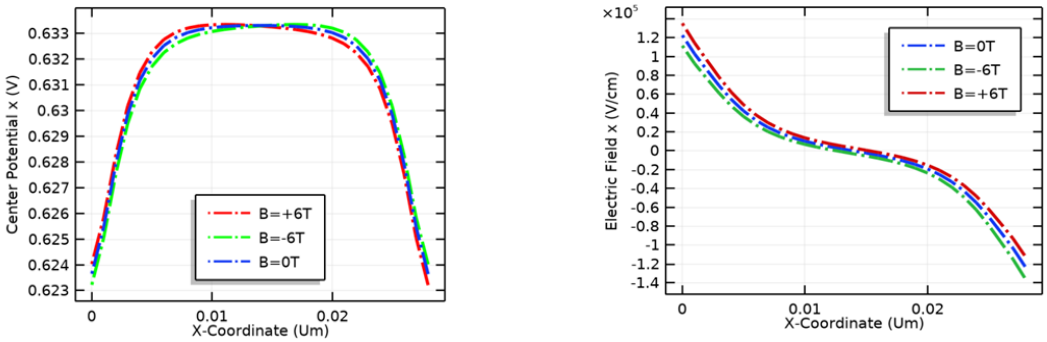
Figure 2. Characteristics of the DG MOSFET obtained by simulation; (a) hall voltage (V_H) variation with gate voltage when B=+6, -6 Tesla and B=0 Tesla at V_D=0.05V and (b) hall voltage V_H variation with drain current I_D for various gate voltage V_G, when B=+6, -6 Tesla and B=0 Tesla at V_D=0.05V



(a) (b)

Figure 3. Simulation-derived DG MOSFET characteristics; (a) hall voltage V_H variation with drain voltage (V_D) when B=+6, -6 Tesla and B=0 Tesla at V_G=0.05V and (b) hall voltage V_H variation with drain current I_D for various drain voltages, when B=+6, -6 Tesla and B=0 Tesla at V_G=0.05V

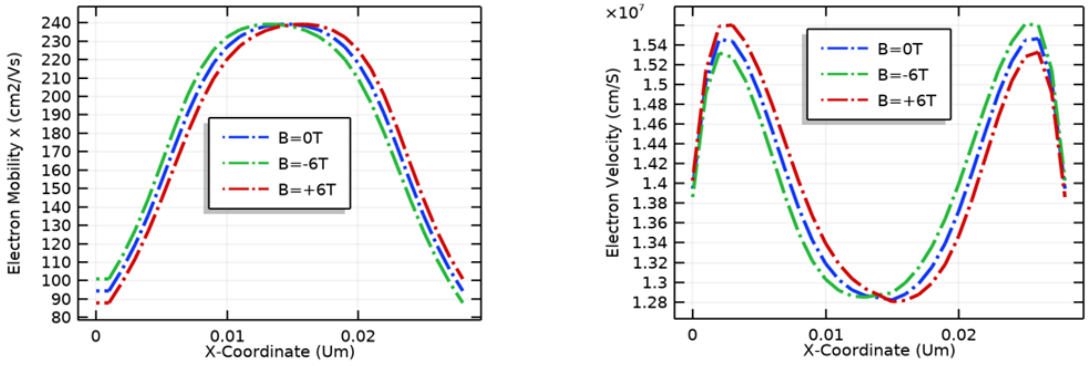
Figure 4(a), illustrates the center potential in the x-direction for three values of the magnetic field. The results are considered when the device is in the on state and the gate voltage varies from 0 V to 1 V and the drain voltage is 0.05V, hence a large value of the current in the channel under gate voltage. When the drain-source current emerged in a magnetic induction B perpendicular to the direction of this current, a hall effect appeared which gave rise to a potential difference between the two contact hall surfaces Figure 4(a), and a transverse electric field in the x-direction in the silicon channel Figure 4(b).



(a) (b)

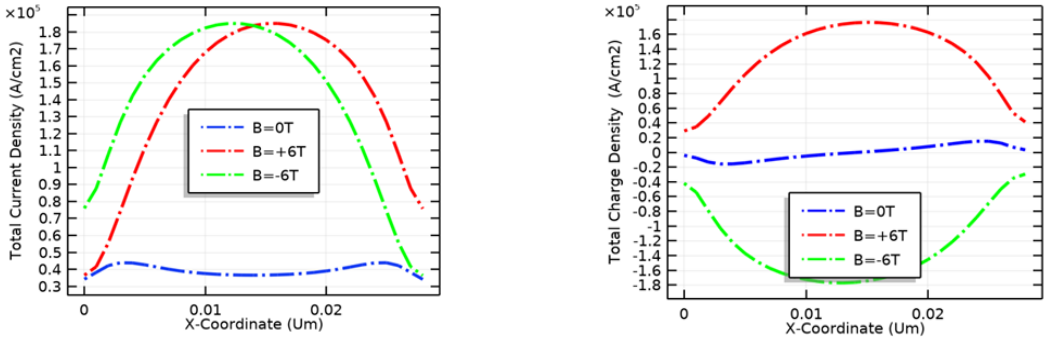
Figure 4. Simulation characteristics obtained from the DG MOSFET transistor; (a) center potential along the channel length in the x-direction for three values of magnetic field B=+6, -6, and B=0 Tesla at the various gate to source voltages V_G and V_D =0.05V and (b) electric field along the channel length in the x-direction for three values of magnetic field B=+6, -6 and B=0 Tesla at the various gate to source voltages V_G and V_D=0.05V

The electric field which compensates for the Lorentz force due to the charges which accumulate on the hal1 and hal2 faces tends to modify the mobility and the velocity of the electrons Figure 5(a), and Figure 5(b), respectively, along the x-axis while respecting both orientation and the absence of a magnetic field. The electrons crossing the silicon channel in the direction opposite to that of the drain current undergo the Lorentz force, according to the direction of the magnetic field, accumulating there, thus creating new trajectories of the current lines along the x-axis, illustrated in Figure 6(a), and a differential charge density distribution shown in Figure 6(b).



(a) (b)

Figure 5. Characteristics of the DG MOSFET obtained by simulation; (a) electron mobility along the channel length in the x-direction for three values of magnetic field B=+6, -6, and B=0 Tesla at the various gate to source voltages V_G and V_D =0.05V and (b) electron velocity along the channel length in the x-direction for three values of magnetic field B=+6, -6, and B=0 Tesla at the various gate to source voltages V_G and V_D=0.05V



(a) (b)

Figure 6. Simulation-derived DG MOSFET characteristics; (a) total current density along the channel length in the x-direction for three values of magnetic field B=+6, -6, and B=0 Tesla at the various gate to source voltages V_G and V_D =0.05V and (b) total charge density along the channel length in the x-direction for three values of magnetic field B=+6, -6, and B=0 Tesla at the various gate to source voltages V_G and V_D=0.05V

Figures 7(a), and 7(b), illustrates the energy band diagram of DG MOSFET transistor. The band diagrams are along the channel in the x-direction following the hall-field direction. The two band diagrams show the position of the valence and conduction bands. The two band diagrams are considered when the device is on and the gate voltage varies from 0 V to 1 V and the drain voltage is 0.05V, Hence an increased value of the current in the channel under the gate region. Also, quasi-fermi level shifts of electrons and holes appeared caused by the action of an induction field in the current which modifies the distribution of the energy band levels.

The I_D versus V_D curve under constant magnetic flux density, B=0 Tesla, 6 and -6 Tesla are shown in Figure 8(a). It can be seen that in the linear region of the I_D vs V_D curve, the drain current I_D remains the same with both directions of the applied magnetic field, but in the saturation region, I_D increases or decreases depending on the direction of the applied magnetic field. Due to the hall effect, since electrons accumulate on the surface of the hall1 and hall2 contacts, the value of the amplitude of the charge of the inversion layer per

unit area is effectively reduced, which reduces the magneto-conductance of the channel shown in Figure 8(b), and therefore, the drain current I_D is reduced. If the constant magnetic field, B is applied along the reverse direction, along the negative y-direction, then the effect will be totally opposite. In this case, the magneto-conductance will be increased, causing the drain current I_D to increase.

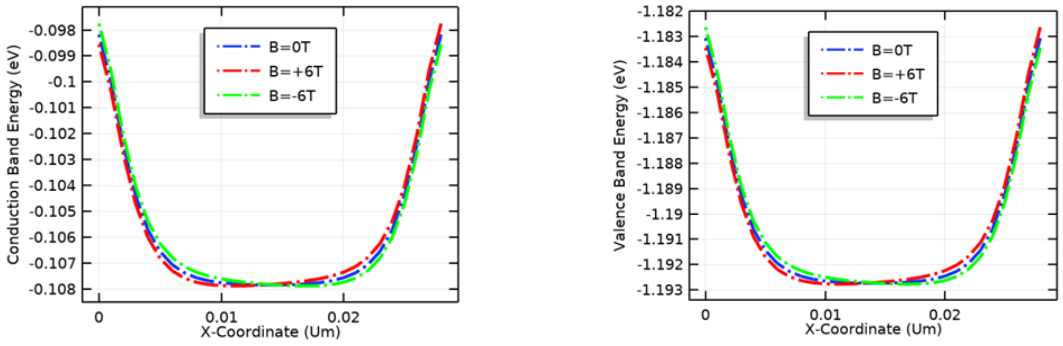


Figure 7. Simulation characteristics obtained from the DG MOSFET transistor; (a) conduction band energy along the channel length in the x-direction for three values of magnetic field B=+6, -6, and B=0 Tesla at the various gate to source voltages V_G and V_D=0.05V and (b) valence band energy along the channel length in the x-direction for three values of magnetic field B=+6, -6, and B=0 Tesla at the various gate to source voltages V_G and V_D=0.05V.

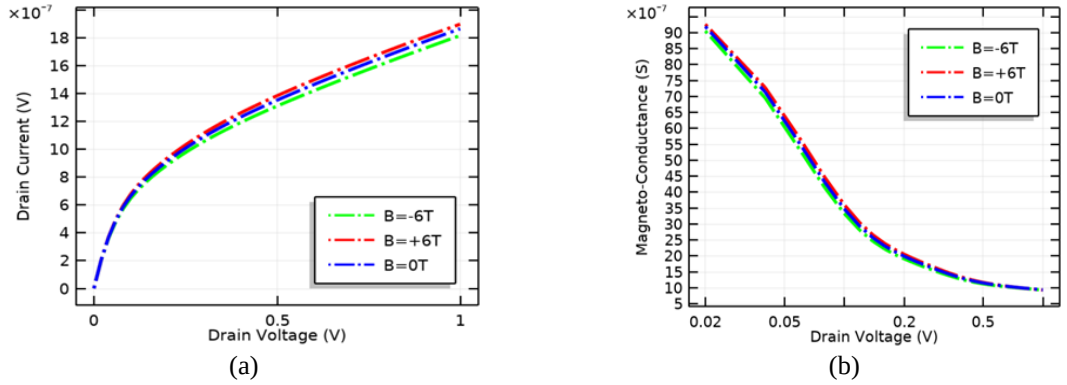


Figure 8. Simulation-derived DG MOSFET characteristics; (a) drain current (I_D) against drain voltage (V_D) when B=+6, -6 Tesla and B=0 Tesla at V_G=0.5V, after [17] and (b) valence band energy along the channel length in the x-direction for three values of magnetic field B=+6, -6, and B=0 Tesla at the various gate to source voltages V_G and V_D=0.05V

Figure 9(a), shows a proportionality of an imbalance of the drain current I_D as a function of the direction of applied magnetic field B, for the different values of the drain voltage V_D=0.1V, V_D=0.5 V, and V_D=1V. Note that there is a significant difference in sensitivity for the higher drain voltages which corresponds to the saturation region of the I_D vs V_D curve Figure 8(a). The difference is a little less in the region of the threshold voltage V_T=0.44072V at B=0Tesla0, but the difference is almost negligible if observed at the smallest drain voltages V_D. The result is obtained by the experimental work of [17], [18].

The sensitivity of the device for both channels has been evaluated and the results are shown in Figure 9(b). Here Figure 9(b). Illustrates a proportional sensitivity, between the difference of the Hall voltage as a function of the direction of applied magnetic field for the different values of the gate voltage Vg=0.1V, Vg=0.5V, and Vg=1V obtained in Figure 2(a). There is a significant difference in sensitivity for the different gate voltages, but the high difference is observed at gate voltages near the threshold voltage V_T=0.44072V at B=0Tesla.

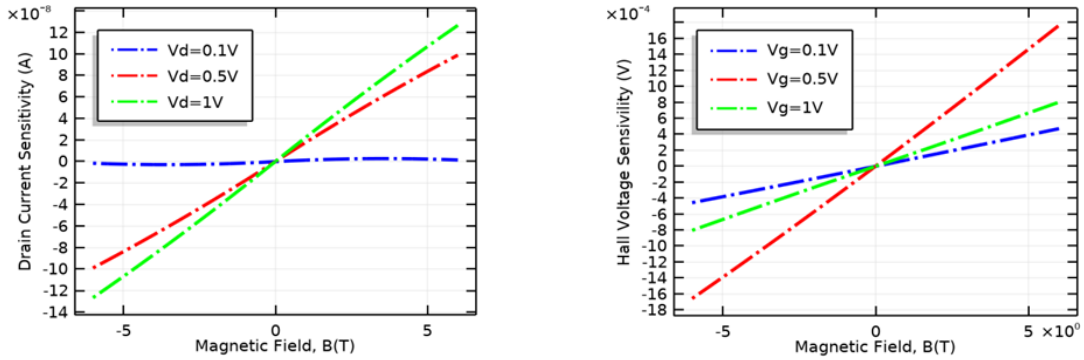


Figure 9. Simulation characteristics obtained from the DG MOSFET transistor; (a) drain current I_D imbalance $\Delta I_D=I_{D1}-I_{D2}$ against magnetics field and (b) hall voltage difference $\Delta V_H=V_{H1}-V_{H2}$ versus magnetics field

3.1. DG MOSFET performance analysis

The performance of the MOSFET circuits was also analyzed and characterized in the sub-threshold region, where the source gate voltage V_G was varied, while the source-drain voltage V_D was maintained at 50 mV. From these conditions, we calculate the different performance parameters of the DG MOSFET, the threshold voltage (V_T), ON current (I_{ON}), subthreshold leakage current (I_{OF}), (I_{ON} / I_{OF}) ratio, and the maximum of the magneto-transconductance (g_{mm}). These parameters are very important for the operation of analog circuits since in this mode of operation the transistor consumes less energy [29], [30].

In Figure 10, the source-drain current I_D was evaluated for three magnetic field values, at B=0T and within the magnetic field, B=+6T and B=-6T was found to have the same behavior for both directions orientation of the magnetic field (positive and negative) so that the source-drain current in the sub-threshold region and seems a little sensitive compared to the saturation region. The result shows that the source drain current I_D is dependent on the field strength and independent of the direction of magnetic field orientation [13], [20] in experimental studies. It is the same behavior for the maximum of the magneto-transconductance illustrated in Figure 11. This shows that the maximum of the magneto-transconductance decreases for the two orientations of the magnetic field with respect to 0 tesla [20].

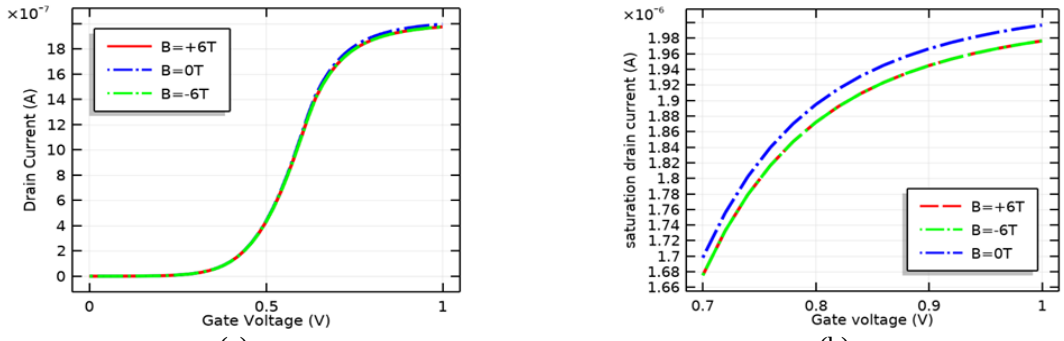
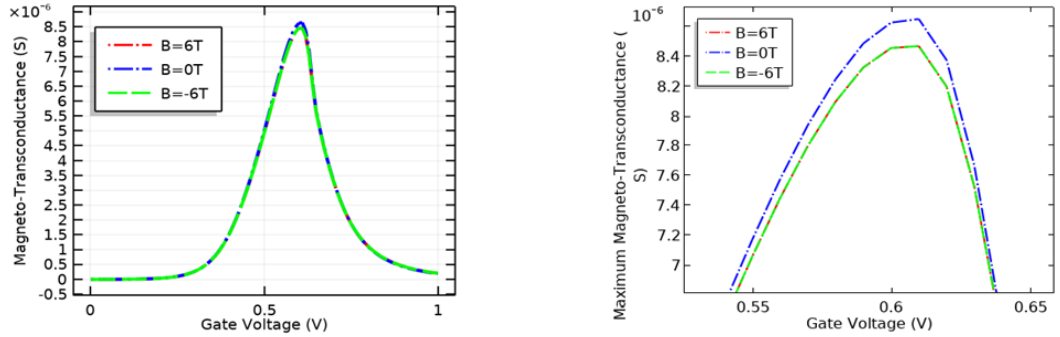


Figure 10. Simulation results from the DG MOSFET transistor; (a) drain current I_D against gate to source voltage (V_G) when B=+6,-6 Tesla and B=0 Tesla at V_D=0.05V, after [6], [7], [31] and (b) zoom in, on Figure 10

The sensitivity of the two parameters, the drain current at the threshold voltage V_{TH} and the maximum of the magneto-transconductance are evaluated as a function of the magnetic field B, which are presented in Figure 12(a), and Figure 12(b). Respectively, the result illustrates a significant decrease in the two parameters studied. The reduction in drain current at the threshold voltage confirms the reduction of the threshold voltage as a function of the magnetic field shown in Figure 13(a).

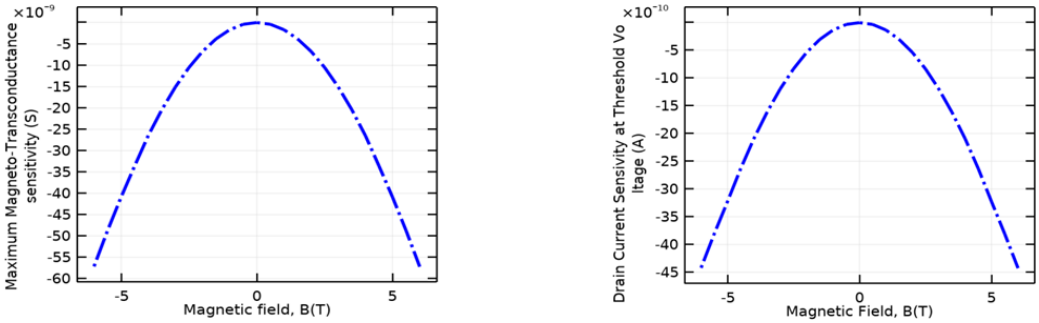
The sensitivity of the threshold voltage V_T and the (Ion / Iof) ratio considered as essential performance parameters of the MOSFET transistor is evaluated as a function of the magnetic field, and the results are shown in Figure 13(a). Here, Figure 13(b), shows that the threshold voltage V_T is reduced

depending on the applied magnetic field, which will affect the applied switching gate voltages, noting that the threshold voltage is reduced by 10^{-3}V for a magnetic field equal to ±6 Tesla. We also notice a significant disturbance of the (Ion / Iof) ratio shown in Figure 13(b), knowing that for a magnetic field equivalent to ±5.5 Tesla, the ratio is reduced by 10^{2}, this reduction is considered as an adverse effect in CMOS technology.



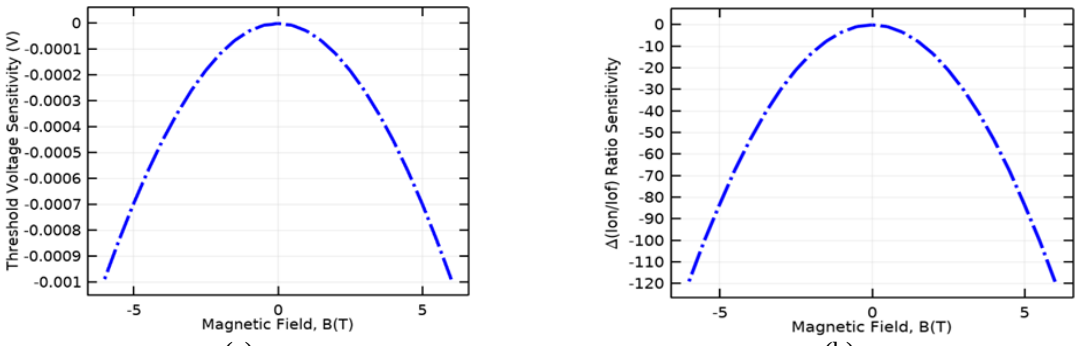
(a) (b)

Figure 11. Characteristics of the DG MOSFET obtained by simulation; (a) magneto-transconductance g_{mm} against the gate voltage V_G, when B=+6, -6 and B=0 Tesla at V_D=0.05V, after [6], [7], [31] and (b) zoom in, on Figure 11



(a) (b)

Figure 12. Simulation results from the DG MOSFET transistor; (a) maximum magneto-transconductance difference $\Delta g_{mm}=g_{mm1}-g_{mm2}$ against magnetic field B at V_D=0.05V and (b) drain current difference at threshold voltage V_T against magnetic field B at V_D=0.05V



(a) (b)

Figure 13. Simulation results from the DG MOSFET transistor; (a) threshold voltage (V_T) difference $\Delta V_T=V_{T1}-V_{T2}$ against the magnetic field (B) at V_D=0.05V and (b) (I_{ON}/I_{OF}) ration difference Δ (I_{ON}/I_{OF}) = $(I_{ON}/I_{OF})_1-(I_{ON}/I_{OF})_2$ against magnetic field B at V_D=0.05V

4. CONCLUSION

This article presented our first numerical simulation of the effect of a hall field induced by a magnetic field on the electrical characteristics of the n-type channel DG MOSFET transistor. It is shown that for short transistors, the hall voltage V_H peaked for both directions of the magnetic field in the threshold region as expected in a shorter channel FET compared to the long channel FET, conforms to many theories.

This states that the drain current (I_D) changes for different drain voltages (V_D) for directions of the applied magnetic field perpendicular to the direction of the drain current flow caused by the layer inversion charge, that directly reflects the magneto-conductance behavior. It is also shown that for short channel transistors, the drain current I_D and the magneto-transconductance (g_{mm}) are also reduced and found dependent on the intensity but not on the magnetic field direction. An undesirable effect observed concerns the reduction of the (Ion / Iof) ratio as a function of the applied magnetic field (B), which is one of today's requirements for CMOS technology. As a perspective of this work, we began to study the different solutions to be developed to remedy its controlled parasites, quantified in order to reduce them (or even eliminate them).

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