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Sinusoidal Signal Generator for ADC Testing in Mixed-Signal SOC

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Abstract

Sinusoidal signal can be used as stimulus to test static and dynamic parameters of ADC. A sigma-delta modulation based sinusoidal signal generator for ADC testing in SOC was introduced. The generator was built on the same chip with ADC. A numerical resonator generated a sinusoidal signal which was converted to a single bit stream by a sigma-delta modulator. Due to oversampling, the quantization noise was pushed to high frequency range. A high-quality sinusoidal signal was generated by low-pass filtering the bit stream. The sigma-delta modulator was inserted into the resonator to decrease silicon area overhead and calculate time. A cascaded integrator comb decimation filter was used as the low-pass filter. The amplitude and frequency of the output sinusoidal signal could be accurately set by digital parameter of the generator to meet the requirement of static and dynamic performances testing.

Keywords*: sinusoidal signal generator, sigma-delta modulator, cascaded integrator comb filter, ADC testing*

1. Introduction

Increasingly more analog and mixed signal cores are integrated in complex Systems-on-Chip (SOC). Those cores are normally very sensitive to noise and loading effects, which limit the external monitoring and make their test a major challenge in SOC technique [1]. To resolve the problem, one promising strategy is the BIST (built-in self-test) approach in which both stimulus generation and response measurement are performed on the chip. The most commonly used mixed signal devices are analog-to-digital converters (ADC) and digital-to-analog converters (DAC) [2].

Within the past few years, Several BIST schemes for ADC have been proposed in literature [1-5]. But few approaches in the literature have proposed to can test both the static and dynamic parameters in one BIST scheme because the silicon area overhead would be unacceptable. To measure both static and dynamic parameters, it is necessary to have trustful and highly configurable stimulus. In this paper, we focus on developing efficient sinusoidal signal generator for stimulus of ADC testing. The amplitude and frequency of the output sinusoidal signal can be accurately set by digital parameter of the generator to meet the requirement of static and dynamic performances testing.

2. Sinusoidal Signal Generator

Spectrum analysis and histogram analysis are commonly used methods to testing an ADC [6]. Spectrum analysis uses the steady state response of the ADC under test to a multisine stimulus to calculate the characteristics parameters of the ADC. There are so many dynamic behaviour of ADCs can be described by frequency-domain characteristics parameters, such as IMD (InterModulation Distortion), SINAD (Signal to noise and distortion ratio), THD (Total Harmonic Distortion), SNR (Signal to Noise Ratio), SFDR (Spurious-Free Dynamic Range). Histogram testing method is widely used for determination of nonlinearity errors of ADC. The histogram method involves the application of a given analog signal to the ADC input and the record of the number of times each code appears on the ADC outputs. Processing the measured data against a reference histogram then permits extracting the circuit's characteristics. The excitation signals for ADC under test can be either a low-slope ramp signal

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or a low-frequency sinusoidal wave. But a ramp generator is analog circuit which is normally very sensitive to noise and difficultly used to BIST. The input ramp should have at least two to four bits of resolution more than that of the ADC under test. In addition, it is easy to improve sinusoidal signal purity by suitable filtering [3,4]. So the stimuli of histogram analysis and spectrum analysis are sinusoidal signal. For static testing, an low-frequency sinewave is required. For dynamic testing, a high purity high-frequency sinewave is required.

One of the main stumbling blocks for BIST of ADC has been the difficulty of fabricating a precision analog signal generator on the same chip with the ADC without any external testing or calibration. Analog circuits are sensitive to parameters of the circuits. A significant percentage of mixed-signal SOC may contain DSP, digital, memory, analog and mixed-signal cores, so we can use those digital core to generate a sinusoidal signal. In [2,3], an all digital method that encodes an analog signal inside a pulse density modulated single bit-stream was shown to be capable of generating a high-quality analog multitone signal by simply low-pass filtering the bit stream with a rather imprecise filter. This paper modified the method in [2,3].

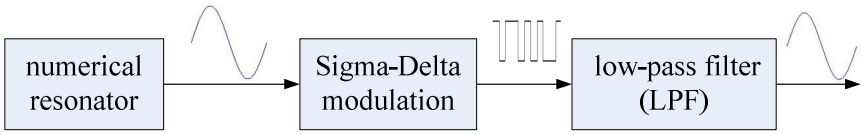

Figure 1. The scheme of the sinusoidal signal generator

Figure 1 illustrates the scheme of the sigma-delta modulation based sinusoidal signal generator. A numerical resonator output a sinusoidal signal which have noise. A digital sigma-delta modulator converted those discrete sinusoidal signals to a pulse density modulated single bit stream and push the noise to high frequency range. By using an low-pass filter (LPF), the high frequency range noise is filterd out. The output of the LPF is a high-quality sinusoidal signal. As this method is essentially all digital and can accurately set both the amplitude and phase of each of the sinewave, it is the ideal stimulus for ADC BIST in SOC. This paper modified the structure of the genrator and the LPF.

2.1. Numerical Resonator

The structure of the numerical resonnator is shown as Figure 2. The resommator resemble an LC resonator. The location of the resonator ploes is determined by configuuring the coefficients a_1 and a_2. Assuming the resonator is clocked at a rate f_{os} = 1/T, the oscillation frequency ω_0 will take the following form:

$$\omega_0 = \begin{cases} f_s \arccos(1 - \frac{a_1 a_2}{2}) & 0 < a_1 a_2 \le 2 \\ f_s[\pi - \arccos(1 - \frac{a_1 a_2}{2})] & 2 < a_1 a_2 < 4 \end{cases} \quad (1)$$

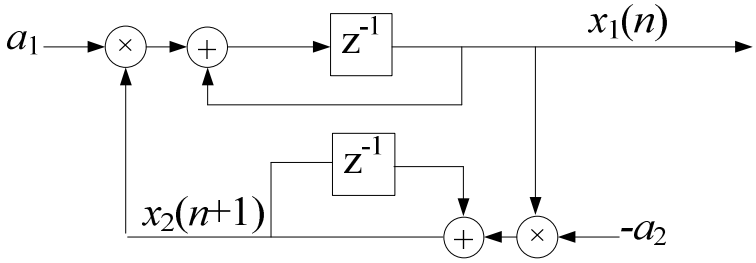

Figure 2. The structure of the numerical resonator

The amplitude (*A*) and phase (φ) of the oscillating tone are determined by the initial conditions imposed on registers x_1 and x_2:

$$A = \frac{(1 - a_1 a_2) x_1(0) + a_1 x_2(0)}{\sin(\omega_0 T + \phi)} \quad (2)$$

$$\varphi = \tan^{-1}\left(\frac{x_1(0)\sin(\omega_0 T)}{(1 - a_1 a_2 - \cos(\omega_0 T)) x_1(0) + a_1 x_2(0)}\right) \quad (3)$$

Based on equations (1)-(3), we can obtain the desired frequency, amplitude and phase of the sinusoidal signal through proper selection of coefficients a_2 and a_1 and the initial conditions on $x_1(0)$ and $x_2(0)$ [2].

2.2. Sigma-Delta Modulator

The sigma-delta modulator is used to transfer the resonator output signal into a 1-bit stream. The resonator output is a multi-bit sinusoidal digital signal of amplitude A and frequency $f_0=\omega_0/2\pi$. If we converted the digital signal to an analog signal a high resolution DAC is required that will increase the area overhead of chip. The sigma-delta modulator quantizes an input signal into 2 categories: above 0 or below 0, and converts an input signal to be 1 or -1, respectively. So a multi-bit digital input signal is encoded into a pulse-density of the a signal-bit stream. Figure 3 shows the scheme of sigma-delta modulator. $X_1(n)$ is the sinusoidal digital signal, $x(n)$ is the 1-bit output bit stream. For 1_{st} order sigma-delta modulator, the fuction H(z) is $H(z) = \frac{z^{-1}}{1 - z^{-1}}$.

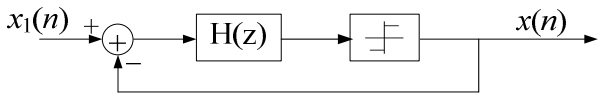

Figure 3. The scheme of sigma-delta modulator

Assuming the quantization noise delta is white, and noting that the total noise power is e_{rms}^2 in the range of $\pm\frac{f_s}{2}$,

$$e_{rms}^2 = \frac{1}{\Delta}\int_{\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \quad (4)$$

Where Δ is quantization step. The spectral density of the quantization noise is [7]:

$$E(f) = e_{rms}\sqrt{\frac{1}{f_s}} = \left(\frac{\Delta}{\sqrt{12}}\right)\sqrt{\frac{1}{f_s}} \quad (5)$$

If the signal is bandlimited to f_o, the sigma-delta modulator use a higher sampling rate, f_s, than the Nyquist rate, $2f_o$. Usually, the oversampling rate (*OSR*) is from 16 to 512, $OSR=f_s/2*f_0$,. When sigma-delta modulator use high sampling rates, or *OSR*>>1, the quantization noise is spread over the larger sampling frequency. Since the signals of interest are all below $f_B<<f_s$, $x(n)$ is fitered by a low-pass filter with bandwidth f_B which eliminates quantization noise greater than f_B. Then the noise power P_n that falls into the signal band will be given by:

$$P_n = \int_{-f_B}^{f_B} E^2(f)df = e_{rms}^2(2f_BT) = \frac{e_{rms}^2}{OSR} = \frac{\Delta^2}{12}\frac{1}{OSR} \quad (6)$$

So the quantization noise in-band is decreased since the overall power of noise is still the same.

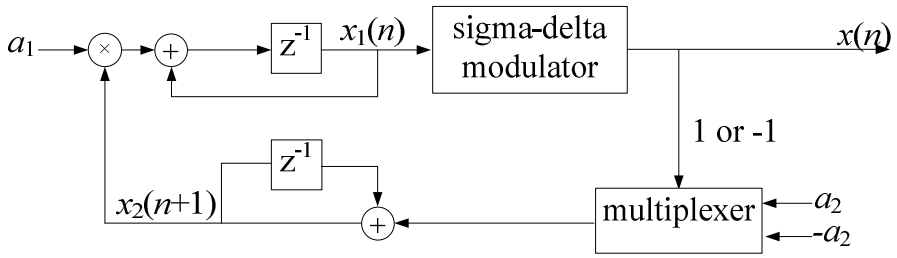

Figure 4. The modified resonator

In order to decrease the area cost and the complexity of the circuit, we modified the resonator. Firstly, the resonator works in oversampling rate f_s to avoid an interpolation filter. Secondly, we move the sigma-delta modulator into the numerical resonator. Because the sigma-delta modulator quantizes an input signal into 2 categories (1 or -1). So we can use a two input multiplexer instead multiplication (multiplicate a_2). At the same time, the coefficients a_1 is selected as 2^n, so the multiplication can be instead with a shift opration. The modified resonator is shown in figure 4.

2.3. Decimation Filter

In order to spread the quantization noise over a large frequency range, the sampling rate of the sigma-delta modulator must be fairly high. To recover the output signal or to lower the sampling rate, a down-sampling filter is required. Sigma-delta modulator spread the quantization noise to high frequency, to eliminate the high frequency noises, a low-pass filter is required. The low-pass filter eliminates the spectrum of X(ω) in the range of π/D<ω<π. The spectrum of X(ω) outside the range is eliminated. The main components of a decimation filter are a low pass filter and a down-sampling device, as shown in figure 5.

Figure 5. The scheme of the decimation filter

The input signal x(n) is the output signal of the sigma-delta modulator, $h(n)$ is a low-pass filter, so w(n) have the same frequencies, f_s, but the decimator reduces the sampling rate of the output signal y(m), to f_s/D, where D is the decimation factor. Then the output sequence of decimation filter y(m) is:

$$y(m) = \mathrm{w}(mD) \quad (7)$$

There are numbers of filter design techniques that can be applied to make a decimator. For example, multi-rate and/or multi-stage decimators are being used. In order to decrease area cost of chip, this paper selected the cascaded integrator comb (CIC) filter [8].

A comb filter or sinck filter has a transfer function as

$$H(z)=\frac{1}{M}\sum_{i=0}^{M-1}z^{-i}=\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}=\frac{1}{M}(1-z^{-M})\left(\frac{1}{1-z^{-1}}\right) \quad (8)$$

where *M* is the length of the filer, and its frequency response is

$$|H(z)|=\frac{1}{M}\frac{\sin(\omega M/2)}{\sin(\omega/2)}=\frac{\sin c(\omega M/2)}{\sin(\omega/2)} \quad (9)$$

The filter can be implementd by cascading the intergrator $\frac{1}{1-z^{-1}}$ with the comb filter $(1-z^{-M})$. This structure dose not require any multipliation or storage for the filter coefficients, so the area cost of chip is small. To obtain an efficient decimation structure, we start with an intergrator-comb filter followed by the downsampler. To improve the lowpass frequency response, we can cascade *k* CIC filter. the function of *k* CIC filter is:

$$H(z)=\left(\frac{1}{M}\sum_{i=0}^{M-1}z^{-i}\right)^{k}=\left(\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right)^{k}=\frac{1}{M}(1-z^{-M})^{k}\left(\frac{1}{1-z^{-1}}\right)^{k}$$

The structure of *K* CIC filter can be modified, order all integrators on one side of the filter and the comb filters on the other side, and then we aplly the first nobel identities as shown in figure 5.

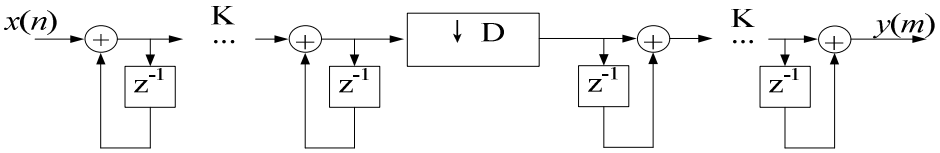

Figure 6. The structure of k CIC filter

So the structure of sigma-delta modulation based sinusoidal signal generator is shown as figure 7. Owing to the over sampling nature of the sigma-delta modulator and the low-pass filtering action of the decimation filter, the nosie of sinusoidal signal was attenuated. Selecte proper coefficients a_2 and a_1 and the initial conditions on x_1 (0) and x_2(0), we can obtain the desired frequency, amplitude and phase of the sinusoidal signal to meet the conditions of static and dynamic performances testing.

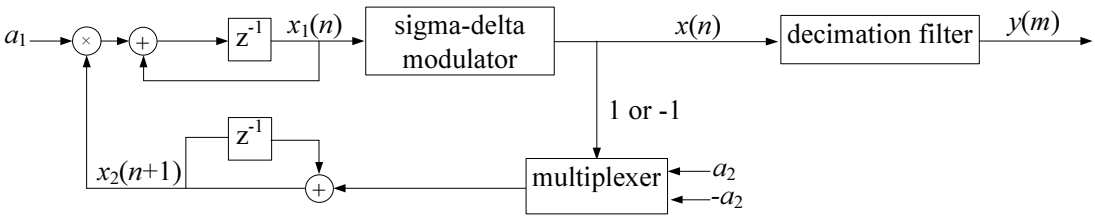

Figure 7. The structure of sigma-delta modulation based sinusoidal signal generator

4. Simulate Result

A 8-bit ADC of ADI corporation, the AD9289 is used to validate the efficiency of the method presented in this paper. The AD9289 is a monolithic, single-supply, 65 MSPS ADC with an on-chip, high-performance sample-and-hold amplifier and voltage reference, 1Vp-p to 2Vp-p input voltage range. We use ADIsimADC with Matlab on a PC platform to capture the ADC output codes and calculate the frequency spectral under a special stimulus. The behavioral modeling of the ADC and ADIsimADC are offered by ADI corporation.

For the dynamic testing, the values fos = 1MHz, a1 = 2^{-7}, a_2 =4.81928*10^{-3}, $x_1(0)$ = 0 , $x_2(0)$ = 0.78539 are selected, then we can obtain the oscillation frequency of f = 1Khz, A =1 and φ= 0. Figure 8 shows the sinewave of resonator output. The bit strem of sigma-delta modulator output is shown in figure 9. The spectrum of the bitsream of sigma-delta output is shown in figure 10. If the decimation factor D=4, the spectrum of the sinusoidal signal generator is shown in figure 11, the high frequeny noise is eliminated. Figure 12 shows the frequency spectrum of ADC response to the sinusoidal signal. The SINAD is 47.436dBc.

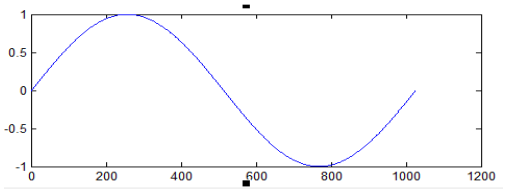

Figure 8. The sinewave of resonator output

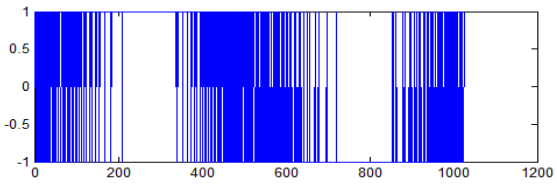

Figure 9. The bitsream of sigma-delta output

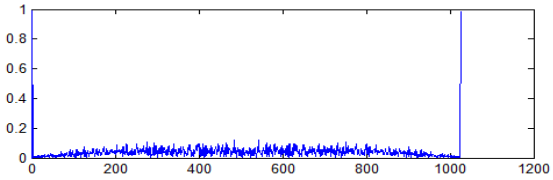

Figure 10. The spectrum of the bitsream of sigma-delta output

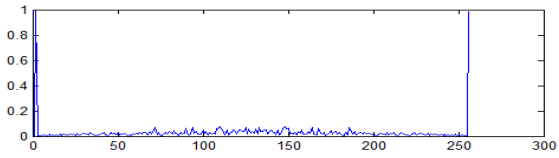

Figure 11. The spectrum of the sinusoidal signal generator

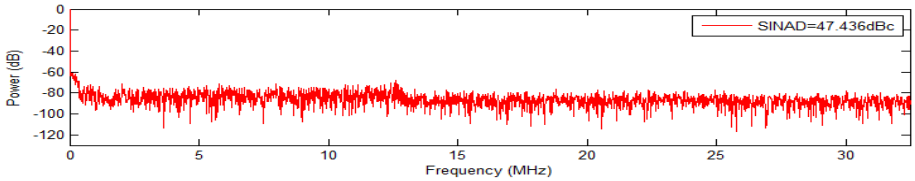

Figure 12. The spectrum of ADC response

4. Conclusion

Spectrum analysis and histogram analysis are commonly used methods to testing an ADC. The stimuli of histogram analysis and spectrum analysis are sinusoidal signal. For static testing, an low-frequency sinewave is used. For dynamic testing, a high purity high-frequency sinewave is used. A sigma-delta modulation based sinusoidal signal generator for ADC testing in SOC was introduced in this paper. Owing to the over sampling nature of the sigma-delta modulator and the low-pass filtering action of the decimation filter, the nosie of sinusoidal signal was attenuated. The frequency, amplitude and phase of the sinewave stimuli can be adjusted through proper selecting generator parameters which are stored in ADC WBR. So the silicon area overhead of the BIST structure of this paper is small. Simulation result proved the method in this paper is efficient.

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