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A Overlapping Carrier Based SPWM for a 5-Level Cascaded H-bridge Multilevel Inverter

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Abstract

This paper proposes a switching control for a cascaded H-bridge inverter structure with reduced switches which is used to improve the THD performance of a single phase five level CHB MLI. The multi level inverter is simulated for the conventional carrier overlapping APOD and the proposed carrier overlapping APOD Pulse Width Modulation (PWM) switching control technique. The total harmonic distortion (THD) of the output voltages are observed for both PWM control techniques. The performance of the symmetric CHB MLI is simulated using MATLAB-SIMULINK. It is observed that the proposed carrier overlapping APODPWM provides output with relatively low THD as compared to the conventional carrier overlapping APODPWM.

Keywords: *Multi-level inverter, APODPWM, THD, MATLAB/SIMULINK*

1. Introduction

An inverter is defined as an electrical devices that converts direct current (dc) input voltage to an alternating current (ac) output voltage of desired magnitude and frequency [1-4]. MLI aims at achieving higher power by using series of power semi-conductor switches with several low DC sources. Several multilevel topologies have emerged and the most common amongst them include the Diode-Clamped Multilevel Inverter (DCMLI), Flying-Capacitor Multilevel inverter (FCMLI) and Cascaded H-bridge Multilevel Inverter (CHBMLI) [6]. There are numerous switching control techniques for the CHBMLI but there are two Pulse Width Modulation (PWM) technique mostly used in multilevel inverter control strategy [2-5]. For high switching frequency, strategies such as space vector PWM, Selective Harmonics Elimination PWM and Sinusoidal PWM are used. Among these PWM methods, SPWM which is a carrier based disposition method (PDPWM, PODPWM and APODPWM) is mostly used for MLI [6-9].
In this paper, a MATLAB/SIMULINK analysis of the THD and Modulation index comparison between the APOD SPWM control strategy and a carrier overlapping PWM strategy for a 5 level CHB MLI with reduced power switches is presented.

2. Research Method

2.1. Cascade H-bridge Multilevel Inverter

Below is the general block diagram of multilevel inverter

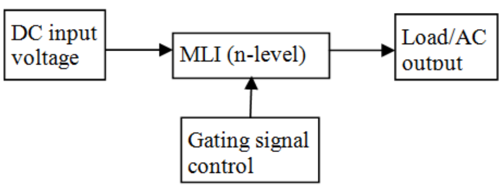

Figure 1. General block diagram of MLI

In general, Cascaded H-bridge MLI has two configurations namely asymmetrical CHB MLI and symmetrical CHB MLI.

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2.1.1. Asymmetrical CHB MLI

Asymmetrical cascaded H-bridge multilevel inverter. These are CHB MLI in which at least one of the dc supply source presents different amplitude, that is H-bridge cells are not fed by equal voltage and the arm cells have different effect on the output voltage steps. Asymmetrical MLI is illustrated with five levels in the figure below.

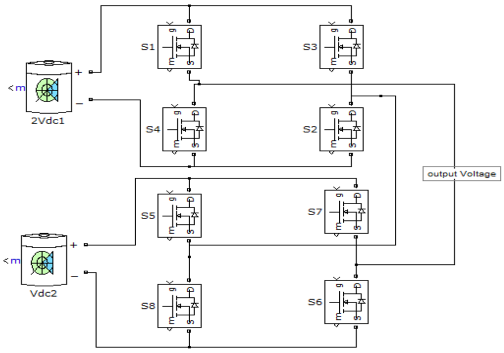

Figure 3. 7-level asymmetrical CHB MLI

2.1.2. Symmetrical CHB MLI

Symmetrical cascaded H-bridge multilevel inverter are the one in which the amplitude of the entire dc supply source to each H-bridge cells is equal [4].

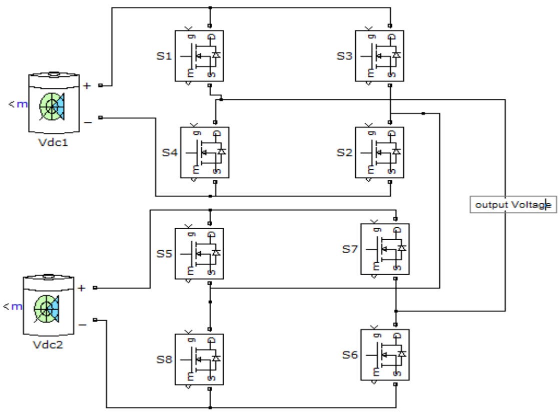

Figure 2. 5-level symmetrical CHB MLI

For example, each level can generate five different voltage outputs $\pm 2V_{dc}$, $\pm 1V_{dc}$, and $0V_{dc}$ by switching the different switches on and off. The output voltage of a multilevel inverter is the sum of all the individual inverter outputs.

$$V_{an} = V_{a1} + \cdots + V_{a[(x-1)/2]} \quad (1)$$

Where: V_{an} = 1-Ø voltage output, $V_{a1\ldots an}$= Output Voltage of individual modules, x= number of levels.

The Fourier transform for the stepped waveform is expressed as:

$$V(\omega t)=\frac{4V_{dc}}{\pi}\Sigma[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)]\sin(n\omega t)/n \quad (2)$$

Where n=*1, 3, 5, 7, .,.*

Each H-bridge unit generates a staircase waveform by phase-shifting its positive and negative phase switching timings. Further, each switching MOSFET always conducts for 180˚ (or half cycle) regardless of the pulse width of the quasi-square wave so that this switching method results in equalizing the current stress in each active device. Cascaded H-bridge topology is chosen for this paper.

2.2. Advantages of Cascaded H-bridge MLI

The advantages of CHB MLI configuration are [3]:

a) Staircase wave form quality which reduces electromagnetic compactibilty.
b) Modularity of control can be achieved.
c) Requires less number of components to achieve the same number of output voltage levels.
d) Draws input current with low distortion.

2.3. Disadvantages of Cascaded H-bridge MLI

The disadvantages of CHB MLI configuration are [3]:

a) Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.
b) Needs separate dc sources for real power conversions, and thus its applications are somewhat limited.

2.4. Types of Carrier based SPWM Techniques

There are different forms of modulation techniques for MLI. Generally, in the pulse width modulation technique, two signals are used, one is reference signal and the other is carrier signal [8].

This paper applied carrier based PWM techniques to the CHB-MLI by using multiple carrier waveforms and a sinusoidal reference wave form [10-12]. The number of carrier waveforms required to produce Y level output is (x-1), where x is the number of carrier waveforms [8].

The sinusoidal reference waveform has peak amplitude A_m and a modulating frequency f_m. The triangular carrier waveforms have a peak amplitude A_c and frequency f_c. The sinusoidal reference signal is continuously compared with all the triangular carrier waveforms. Whenever the sinusoidal reference signal/waveform is greater than the carrier signal, a modulated pulse width is generated. The modulation frequency ratio m_f is given as:

$$m_f = \frac{f_c}{f_m}. \quad (3)$$

The following are Carrier based Overlapping SPWM strategies:

1) Carrier Overlapping Phase Disposition PWM strategy (CO-PD PWM):

If all carriers selected have the same phase, the method is phase disposition method. It is generally accepted that this method gives rise to the lowest harmonic distortion in higher modulation indices. Figure 4 shows the arrangement phase disposition PWM method.

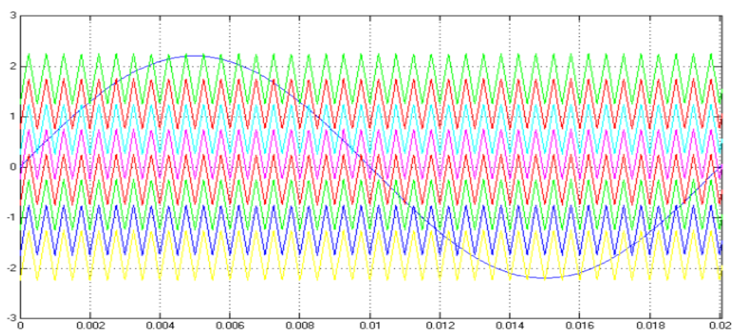

Figure 4. Arrangement of carrier overlapping phase disposition PWM method

Figure 4 depicts the Carrier overlapping PD PWM technique (CO-PD PWM), where the carriers with the same frequency f_c and peak amplitude A_c are arranged such that they overlap each other [5].

2) Carrier Overlapping Phase Opposition Disposition PWM strategy (CO-POD PWM): The carrier waves in the positive plane are 180^o out of phase with those in the negative plane. There is no harmonic at the carrier frequency and its multiples and the dispersion of harmonic occurs around them.

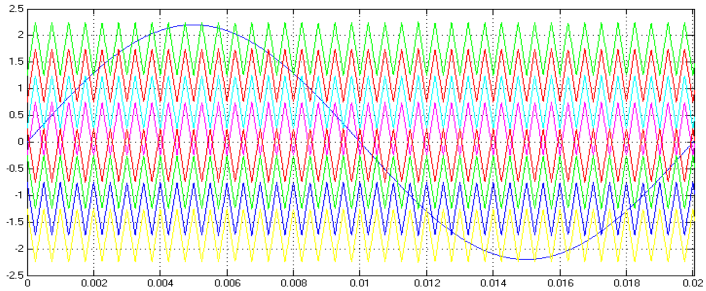

Figure 5. Arrangement of carrier overlapping POD PWM method

3) Carrier Overlapping Alternate Phase Opposition Disposition PWM strategy (CO-APOD PWM):

Each carrier in this method is phase shifted by 180^0 from its adjacent carrier. It is similar to phase opposition disposition. Figure 6 shows the overlapping carrier APOD PWM strategy.

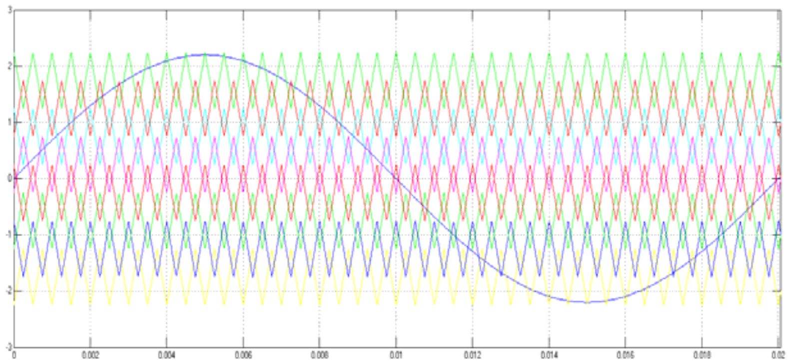

Figure 6. The arrangement of carrier overlapping APOD PWM method

Amplitude modulation index for Carrier Overlapping PD PWM, POD PWM, and APOD PWM is:

$$M_a = \frac{A_m}{2A_c} \tag{4}$$

2.5. Simulation Model

The cascaded 5-level single phase CHB MLI used for this implementation has two dc sources and six switches as shown in Figure 7.

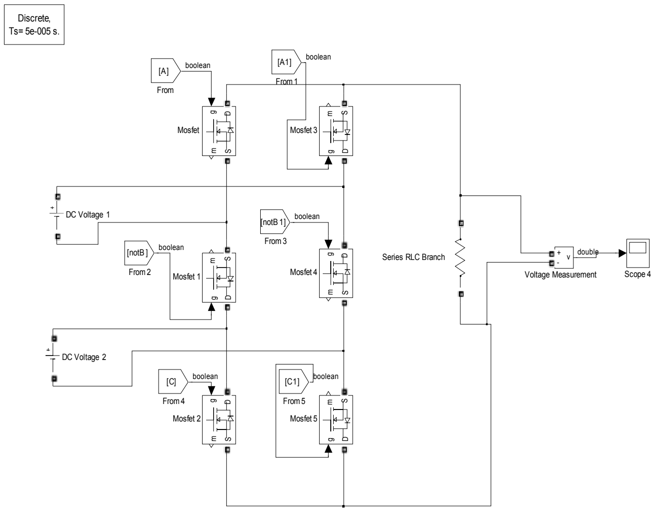

Figure 7. 5-level single phase CHB-MLI

The main advantage of this type of arrangement is its simplicity and improvement of the output voltage resolution with reduced number of components [11].

2.5.1. Operation of Cascaded H-bridge of Five-level MLI Topology

In an individual H-bridge, the output voltage is positive voltage ($+V_{dc}$), zero voltage ($0V_{dc}$) and negative voltage ($-V_{dc}$). Hence the desired output voltage levels for Five-level CHB MLI are ±2V, ±1V, and 0V.

The switching states for the voltage levels are presented as shown in the table below:

Table 1. Switching states of modified 5-level CHB MLI

Switching sequences						Voltage levels
S_1	S_2	S_3	S_4	S_5	S_6	
0	1	0	1	0	1	$+2V_{dc}$
0	1	1	1	0	0	$+1V_{dc}$
1	1	1	0	0	0	$0V_{dc}$
1	0	0	0	1	1	$-1V_{dc}$
1	0	1	0	1	0	$-2V_{dc}$

The above circuit diagram in Figure 7 and its switching state in Table 1 have been modified to avoid switching loss and unnecessary cost. This CHB MLI with six switches and two batteries will improve output waveform and reduce total harmonic distortion. One of the distinguishing features of the above circuit is that it can be used as seven level and five level CHB MLI respectively, by making the two dc input voltages to be different (asymmetric) and make the two dc input voltage equal (symmetric).

2.6. Proposed Overlapping APODPWM Technique

The new switching technique deployed for this paper is the carrier based overlapping APOD PWM with non-zero overlap. The strategy used in this form of technique is a modified overlapping APODPWM technique already known. It involves placing the triangular signals in overlapping mode without crossing the zero time axis. They are aligned both in the positive and negative planes respectively. This is illustrated as shown in the Figure below:

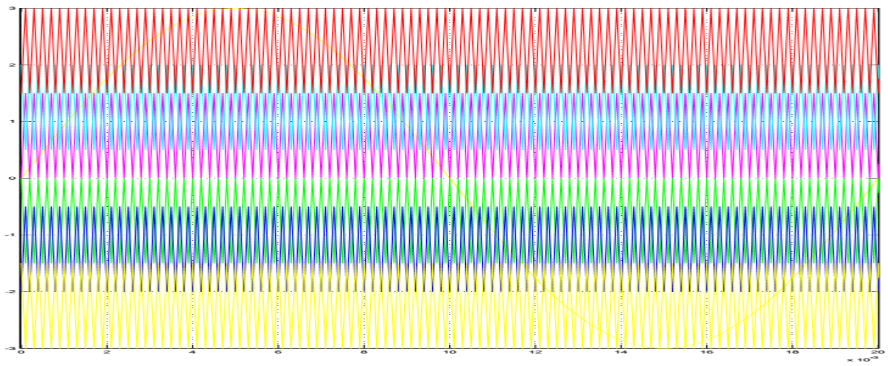

Figure 8. The arrangement of the proposed carrier overlapping APOD PWM

This form of switching is carried out at a carrier frequency of 5 kHz and a fundamental frequency of 50 Hz.

3. Results and Analysis

Simulation of the suggested modulation techniques for comparison for a CHB MLI with reduced switches is carried out using MATLAB/SIMULINK and the following parameters were used: V_{dc} =100V, f_c= 5 kHz and f_m= 50 Hz, M_a=1.0. The Simulated control techniques, Output Voltage waveform and FFT analysis of the 5-level CHB-MLI using both the CO-APOD and the proposed CO-APOD PWM are presented.

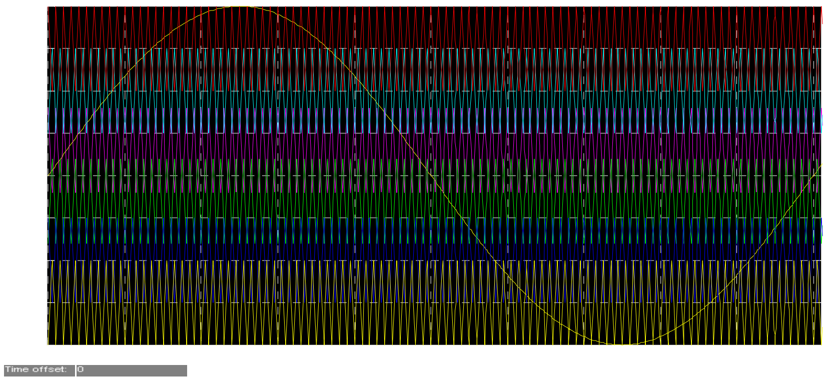

Figure 10. Reference and carrier frequency signal of CO-APOD

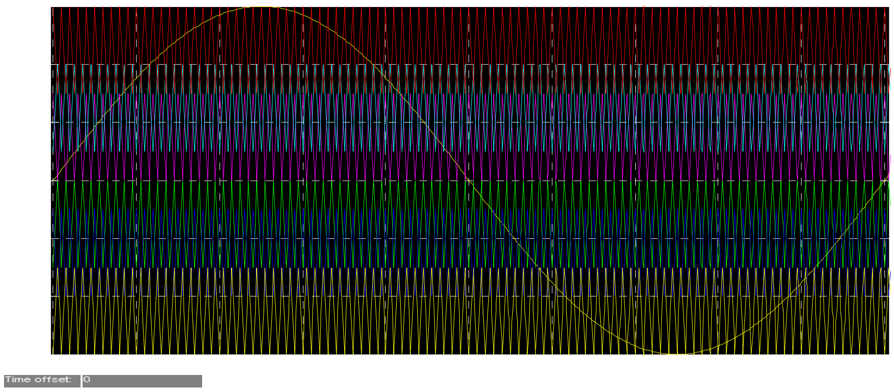

Figure 11. Reference and carrier frequency signal of proposed CO-APOD

The reference signal being super imposed on the six carrier signals are generated via logic combination in SIMULINK and are used for switching the gates of the power MOSFETS. A point to note is that for the proposed CO-APOD, there is no overlap across the zero time axes. The uniqueness of the proposed CO-APOD modulation scheme adopted herein is that it distributes the load evenly across the switching components thereby reduce switching losses.

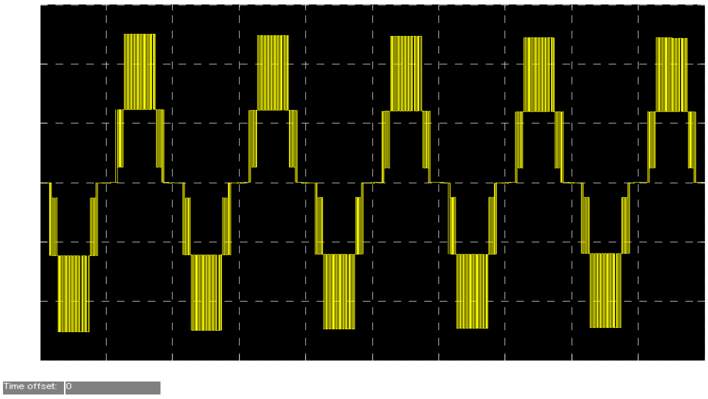

Figure 12. Output waveform of 5-level single phase CHB MLI in SIMULINK for CO-APOD

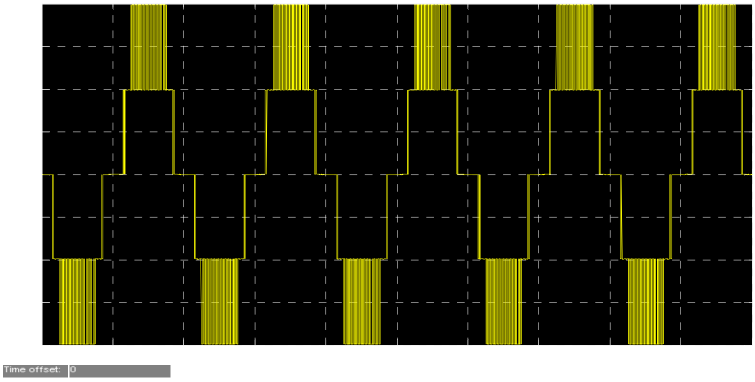

Figure 13.Output waveform of 5-levels single phase CHB MLI in SIMULINK for proposed CO-APOD

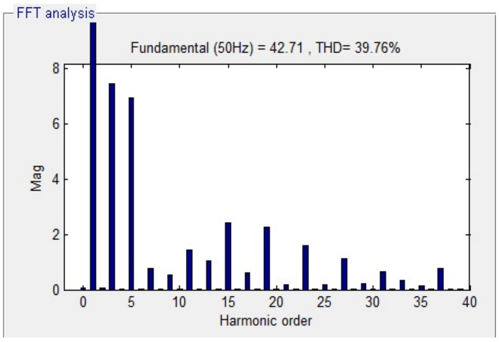

Figure 14. FFT analysis of THD for 5-level CHB MLI using CO-APOD

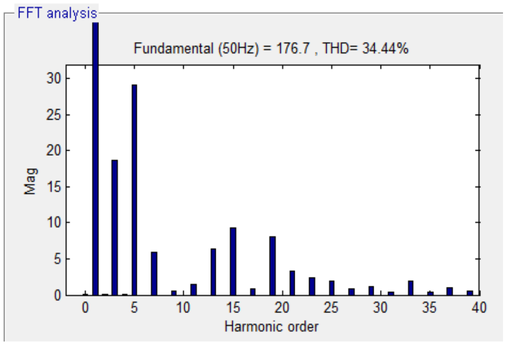

Figure 15. FFT analysis of THD for 5-level CHB MLI using proposed CO-APOD

The above graph represents the THD of the 5-level single phase CHB MLI for the different modulation techniques.

In the CO-APOD, the even order harmonics are eliminated as shown in Figure 14 but in the proposed CO-APOD FFT analysis as shown in Figure 15, the even order harmonics are completely eliminated.

4. Conclusion

This paper suggests a novel PWM technique using overlapping APOD PWM for switching pulses of a 5 level Cascaded Multilevel Inverter with reduced number of H-bridges while producing desired multilevel voltage output. Simulation using MATLAB/SIMULINK software was performed to show the suggested technique for CO-APOD PWM performed better with a THD of 34.44 % as compared to the conventional CO-APOD PWM with a THD of 39.76%

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