Capacitance study of integrated circuits matrix interconnects

Ahcene Lakhlef, Lounas Belhimer, Arezki Benfdila
Microelectronic Research Group, Faculty of Electrical Enginnering and Computer Sciences, MouloudMammeri University Tizi-Ouzou, Algeria

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ABSTRACT

Propagation delays and couplings between nearby lines affect the circuit performances (speed, power consumption) and operations. Propagation delays in longer lines can become critical compared to the clock frequency and can induce unwanted signals in neighboring lines ("crosstalk" phenomenon). Induced line capacitances can induce parasitic signals. Hence characterizing of these capacitances is of paramount importance. The present work deals with the analysis of capacitance of a multilayer conductor interconnect aiming for their possible exact extraction. We used three topologies of a microstrip conductor interconnects and identified the potential distributor and then computed the capacitance and inductance matrix using a finite element method. The first analysis dealt with parallel microstrip conductors and the second with two levels (plan) of a microstrip conductors the results are compared to those obtained by other methods and found quite encouraging.

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Corresponding Author:

Arezki Benfdila
Micro and Nanoelectronics Research Group
Faculty of Electrical Engineering and Computer Sciences
University Mouloud Mammeri
Tizi-Ouzou, Algeria
Email: benfdila@ummto.dz

1. INTRODUCTION

Since the beginnings of micro-electronics in the 1960s, integration densities and the speed of operation of integrated circuits have continued to increase: the size of transistors, the minimum cross-section and spacing of interconnections-that is, the conductive wires connecting the transistors to each other-are increasingly weak, for increasingly complex circuits. These improvements, which double the performance of circuits almost every two years, also amplify the parasitic effects in the chip. Thus the propagation times of a signal in the interconnection lines become critical for the operation of the circuits [1]. The adverse effects that have been ignored by the integrated circuit designers cannot be ignored due to the complexity of the interconnection network and the increasing frequency of power supply, resulting in higher signal delay [2]. The interconnect radiation resistances, line inductances and capacitances continue to increase, causing a significant increase in power supply noise [3]. So, in order to ensure electromagnetic compatibility at the integrated circuit involves an effective reduction of noise sources and the sources of disturbances [4], [5]. Electromagnetic modeling becomes necessary to ensure a predictive approach to all the risks of disturbances induced by electromagnetic interference [6]-[8]. This requires specific tools, models and knowledge in electromagnetic compatibility. The integrated circuit designer should take into account the capacitance and inductances that have not been considered previously, due to interconnection lengths and higher operating frequencies [9]-[11].

When designing and implementing integrated circuits, consideration should be given to the existence of parasitic capacitances between the interconnection lines in order to provide methods for sufficient reduction of the capacitive coupling influence either in led or radiated modes, and to improve their insensitivity to incoming noises, in order to ensure reliable operation [12]. In order to ensure electromagnetic compatibility in the integrated circuit, an effective reduction of noise sources and the origin of disturbances are required [13], [14]. The modeling of all high-performance systems, such as the design of integrated circuits is based on numerical capacitance and inductance field calculation methods; capacitance calculation has drawn the attention of IC designers to the complexity of interconnection networks. The simulation tools must make it possible to define an overall specification of the system to be studied, but the difficulty lies in passing on the noise margins on the system [15].

The increase in integrated circuit integration density has led to considerable development of micro and nanoscale technologies. However, this evolution required a large number of interconnects and significant lengths of conductors used for this purpose in a superposition of microstrip planes [16], [17]. In [18] starting from many rational approximations, a closed-form term for the mutual impedance per unit length of coupled IC interconnects with silicon substrate have been developed [19], the analysis of transmission lines and waveguides in quasi-TEM mode is achieved. We may mention finite difference methods (FDM) [20], Variation method [21], the method of moment [22], the Green's function approach [23], the Galerkin method [24], Finite Element Method [25]. With a complexity comparable to most devices, integrated circuits are also affected by electromagnetic compatibility [26]. As basic bricks for most systems, they are no longer seen as mere components, but as separate systems that can also be affected by their own operation. In an integrated circuit, the current flowing through the interconnections and the voltage swing of the logic gates are sources of electromagnetic noise [27]. This phenomenon is all the higher as the current flows throughout the circuit and the operating parts process several data at the same time.

This work is dedicated to the calculation of the electrical parameters (inductances, capacities) of the interconnection lines placed above a plane of mass using the method of finite elements in 2D by the resolution of the equations of the electrostatic. The aim of this work is to demonstrate the problem of the capacitive and inductive parasite effect on the normal functioning of an interconnect transmission line in an integrated circuit, as well as the importance of the finite element method for modeling such problems. The calculation of the capacity and inductance matrix requires both simulations and conductors, and for each simulation the coupling of all conductors must be considered a priori. However, in a current integrated circuit, there may be, on a surface of the order of a square centimeter, and on a total height of a few microns, more than 8 km of interconnections, that is to say "wires" entangled conductors.

This calculation is therefore very expensive in calculation time, so that to date, the calculation methods used are able to accurately simulate only small portions of circuits, of the order of a maximum of a hundred microns on the side. This is why we proposed the finite element method, for faster calculation time. The method will be compared with the Galerkin method and the moment method in order to validate the calculations. This work aims also at modeling electromagnetic phenomena and more specifically the parasitic effects between the lines of an interconnected network within an integrated circuit to predict possible electromagnetic compatibility (EMC) problems of integrated circuits. Our approach which is based on the finite element method is efficient and fast for the calculation of inductance and capacitance matrices for the type of non-homogeneous structures like the interconnects.

2. INTERCONNECTIONS PROBLEMS IN INTEGRATED CIRCUITS

The today problem of interconnects in an extra high density integrated circuits (ESI) is the wire length and forms that lead to highly generated (electromagnetic) noise. This noise affects the operations of digital circuits by altering the digital voltages (high and low values) corresponding to the (1) and (0) logics. As the density increases the today's ICs are becoming billions of transistors ICs and of few kilometers of wires inside [28]-[30]. Figure 1 shows the integrated circuit interconnect and metallization levels and Figure 2 illustrates the simulated electromagnetic interaction capacitance.

If the radiation problem is not taken into consideration, the IC reliability and lifetime will be severely affected. In order to tackle the problem, one has to know about interconnects characteristics that are basically capacitance and inductance (Resistance values are basically constant). Several works have been done about the subject [31], [32].

The capacitance m1 is the capacitance between line and via (a whole linking to plan levels of transistors) and the capacitance m2 is the line to line coupling capacitances. The capacitances are extracted considering the method given in Figure 1 and 2. We consider a plane containing various conductors consisting of a bus (say data bus). Later we consider a multilevel plane where layers of conductors are described.

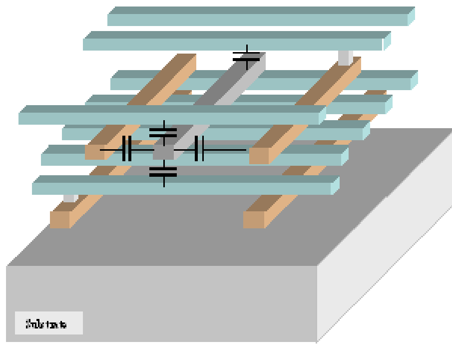

Figure 1. Metallization levels in an IC Chip

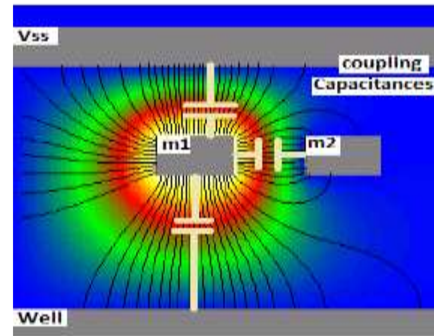

Figure 2. Electromagnetic interaction capacitance

3. MATHEMATICAL ANALYSIS

The basic approach of the finite element method is to subdivide the field of study into finite numbers of subdomains called elements. For electromagnetic problems, the matrix of parallel line capacitances of the microstrip, whose general algorithm begins with a function that has the dimensions of system energy aligned with the partial differential equation representing the two-dimensional distribution, must be evaluated is given by the equation of electrical potential for the region between tracks, we will associate the conditions to the limits of types Dirichlet and Neumann, with the electrical permittivityε (x, y) is a function of the position. The equation to be minimized in this situation is given by:

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = 0 \tag{1}$$

$$F(\phi) = \frac{1}{2}\int_R \varepsilon(x,y)(\nabla \phi(x,y))^2 dxdy \tag{2}$$

The expression of the potential is defined for each subdomain accordingly:

$$\phi(x,y) = \alpha_i(x,y)\phi_1 + \alpha_j(x,y)\phi_2 + \alpha_k(x,y)\phi_3 \tag{3}$$

The calculation of capacitances is carried out using the electrostatic model. This is done by applying a potential difference of 1 volt between the conductors. After solving the problem, the energy stored in the system and given by the following relation:

$$W_e = \frac{1}{2}\int_R \varepsilon |\nabla \phi|^2 dxdy \tag{4}$$

The per-unit length capacitance of each track can be writing

$$C = \frac{2W_e}{V^2} \tag{5}$$

The capacitance parameters for a parallel microstrip line system are described as follows [33]:

$$Q_i = \sum_{j=1}^{n} C_{sij} V_j \tag{6}$$

In order to generalize the study, the influence of the integrated circuit interconnection structure shown in Figure 1, we consider *n* parallel conductors whose parasitic capacitances are shown in Figure 3, with C_{12} C_{23} …$C_{4n}$are the capacitances coupled between lines and C_1 C_2…. Cn are the capacitances coupled between lines and ground plane.

In order to understand and confirm the current proposed formulation, we consider a planar interconnect line with four strips in the first part. In a two-layer dielectric medium we determine the capacitance and inductance matrix using the finite element method, Figure 4 shows the model's structure.

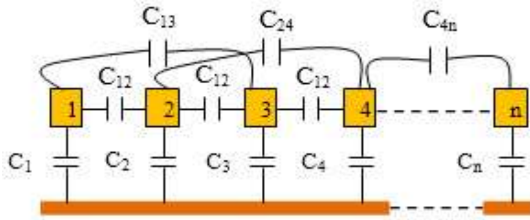

Figure 3. Per unit length capacitances

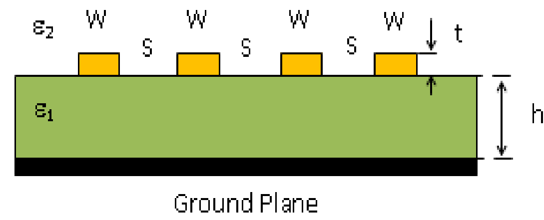

Figure 4. Symmetric microstrip coupled interconnect of general n conductors

Where V_j is the voltage of j_{th} conductor with reference to the ground plane, Q_i is the charge per unit length, C_{sij} is the capacitance of the short circuit between i_{th} and j_{th} conductor. Where the short circuit equivalent capacities can be acquired by:

$$C_{ij} = \sum_{j=1}^{n} C_{sij} \tag{7}$$

$$C_{ij} = -C_{sij}, \mathrm{i} \neq \mathrm{j} \tag{8}$$

Where Cij is the capacitance between both the ith conductor and the ground plane per unit length, the capacitance of [C] matrix for n conductor is determined by:

$$C = \begin{bmatrix} C_{11} & -C_{12} & .... & -C_{1n} \\ -C_{21} & C_{22} & .... & -C_{2n} \\ \vdots & \vdots & & \vdots \\ -C_{n1} & -C_{n2} & .... & C_{nn} \end{bmatrix} \tag{9}$$

$$[L] = \mu_0 \varepsilon_0 [C_0]^{-1} \tag{10}$$

Where, [L] is the inductance matrix, $[C]^{-1}$ is the inverse matrix of the capacitance of the multiconductor transmission line when all dielectric constants are set equal to one, capacitance per unit length matrix ([C] in pF/m), inductance per unit length ([L] in nH/m), impedance ([Z] in Ω), are the electrical parameters, $\mu_0$permeability of space or vacuum and $\varepsilon_0$istheair permittivity.

The expression of impedance per unit length as a function of the capacitance is given by:

$$[Z] = \sqrt{\frac{[L]}{[C]}} \tag{11}$$

4. RESULTS AND DISCUSSIONS

The geometric parameters of the studied model represented in Figure 4 are given by:

S=20µm; $\omega_1=\omega_2=\omega_3=\omega_4$=20µm; ε_1=11.7; ε_2=3.9; h=40µm; t=5µm

Figure 5 shows mesh by finite element, the basic approach of the finite element method is to subdivide the field of study into finite numbers of subdomains called elements. The approximation of the

unknown is done in each element of the interpolation functions. The interpolation function is also defined according to the geometry of the element that is chosen beforehand and coincides with the nodes of this element relative to the values of the unknown. The Figure 6 shows the surface potential distribution we Note that the value of potential increases as it gets closer to the carbon nanotube track that is powered.

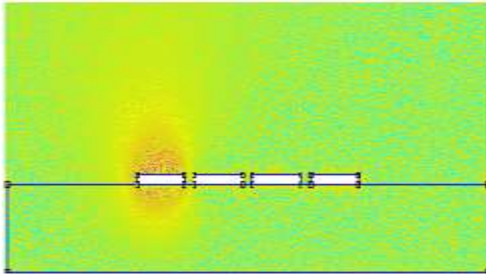

Figure 5. Mesh of the studied model

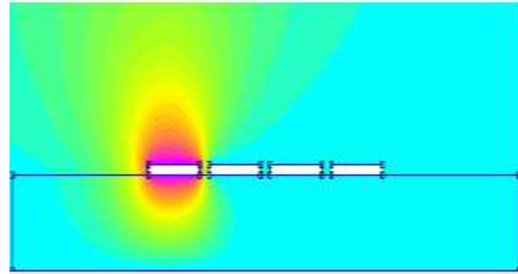

Figure 6. The distribution of potential lines

The capacitance and the inductance per unit length matrix of the coupled interconnects are given by:

$$C = \begin{bmatrix} 0.968 & 0.328 & 0.08 & 0.01 \\ 0.328 & 1.126 & 0.325 & 0.08 \\ 0.08 & 0.325 & 1.126 & 0.328 \\ 0.01 & 0.08 & 0.328 & 0.968 \end{bmatrix} L = \begin{bmatrix} 0.1063 & 0.0381 & 0.0220 & 0.0117 \\ 0.0381 & 0.1025 & 0.0387 & 0.0219 \\ 0.0220 & 0.0387 & 0.1025 & 0.0381 \\ 0.0117 & 0.0219 & 0.0381 & 0.1062 \end{bmatrix}$$

For the first level of metallization it is found that the ground plane capacitance is more important than the between line to line capacitance. It is also noted that whenever the distance between lines is large the parasitic capacitance between lines is small. Table 1 shows the FEM results for the self-capacitance per unit length of the fourth conductor transmission lines interconnect with two dielectric layers. They are compared with the Galerkin method.

Table 1. The system capacity matrix of Figure 6

Capacitance (10^{-10}F/m)	Galerkin method	Our work
C_{11}	0.475	0.968
C_{12}	-0.582	-0.328
C_{13}	-0.114	-0.08
C_{14}	-0.062	-0.01
C_{22}	0.289	1.126

The impedance matrix is given by:

$$Z = \begin{bmatrix} 0.3846 & 0.3182 & 0.2699 & 0.2160 \\ 0.3166 & 0.3957 & 0.3287 & 0.2706 \\ 0.2683 & 0.3286 & 0.3963 & 0.3198 \\ 0.2144 & 0.2702 & 0.3196 & 0.3884 \end{bmatrix}$$

In the next section, we demonstrate our work with modeling as four two-level interconnect lines with two dielectric layers. Our calculation is fixed on the calculation of the inductance and capacity matrix, Figure 7 shows the geometry of the model. Figure 8 shown the Surface potential distribution of two coupled interconnect strip two levels conductor lines.

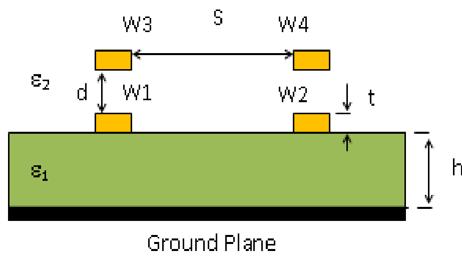

Figure 7. Symmetric two-level microstrip

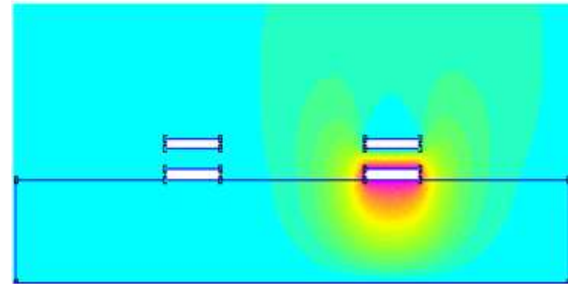

Figure 8. Surface potential distribution of two coupled interconnect strip two levels conductor lines

The geometric parameters of the studied model represented in Figure 7 are given by:
S=60µm; $\omega 1=\omega_2=\omega_3=\omega_4$=20µm; t=5µm; ε_1=11.7; ε_2=3.9; h=40 µm; *d*=30µm.
The capacitance and the inductance per unit length matrix of the coupled interconnects are given by:

$$C = \begin{bmatrix} 6.921 & 1.251 & 1.312 & 2.104 \\ 1.251 & 8.602 & 4.962 & 3.978 \\ 1.312 & 4.962 & 12.86 & 1.409 \\ 2.104 & 3.978 & 1.409 & 14.012 \end{bmatrix} L = \begin{bmatrix} 0.2125 & 0.1016 & 0.0683 & 0.0676 \\ 0.1016 & 0.2619 & 0.1226 & 0.1019 \\ 0.0683 & 0.1226 & 0.1473 & 0.0599 \\ 0.0676 & 0.1019 & 0.0599 & 0.1245 \end{bmatrix}$$

There is an increase in the capacitance of the higher level by contributing to the lower level capacitance, hence, it can be deduced that the capacitive parasite effect is greater when metallization level is raised. Table 2 shows the FEM results for the self-capacitance per unit length of the fourth conductor transmission lines interconnect with two dielectric layers. They are compared with the Moment method.

Table 2. The system capacity matrix of Figure 7

Capacitance (10^{-10}F/m)	MoM	Our work
C_{11}	7.158	6.921
C_{12}	-1.284	-1.251
C_{13}	-1.296	-1.312
C_{14}	-2.224	-2.104
C_{22}	8.732	8.602
C_{33}	13.39	12.86
C_{44}	14.11	14.01

The impedance matrix is given by:

$$Z = \begin{bmatrix} 0.7629 & 0.7553 & 0.6077 & 0.5786 \\ 0.7553 & 0.9686 & 0.7539 & 0.6942 \\ 0.6077 & 0.7539 & 0.6359 & 0.5479 \\ 0.5786 & 0.6942 & 0.5479 & 0.5533 \end{bmatrix}$$

Capacity is found to be less important in the first case than in the second case, in this part, we have to demonstrate the effect of the geometry of the interconnection track on the values of parasitic capacitance. We consider the same geometry for the Figure 4 and Figure 7. To determine the matrix [C] of the given structure, the simulation was made by varying some parameters

The parameters taken into consideration in the simulation are: the thickness of the track (t) ranging from (5 to 10µm), the height of the oxide (h), ranging from 40 to 100µm. Table 3 shown the Parameters values of five cases were simulated. A general analysis makes it possible to notice that the capacitances towards the mass, C_{11} and C_{22} decrease with the increase of the distance h, concerning the plane of mass as show in Figure 9. At the same time, the C_{12} and C_{13} capacities vary in phase, with the increase in h. on finding that the wider the track, the greater the parasitic coupling between the lines.

Figure 10 shows the capacitances as a function of the simulated cases, it can be seen that with the increase in the distance between the interconnection lines and the ground plane, the capacitance values decrease. This reduction is explained by the fact that the distance of the interconnections to the ground plane is varied in order to optimize the thickness of the oxide layer for which the ratio of the parasite capacitance to the capacitance is small.

Table 3. Parameters values of five cases were simulated

Parameters (µm)	Case 1	2	3	4	5
W	20	20	20	20	20
S	60	60	60	60	60
t	5	10	5	10	5
h	40	40	80	80	100

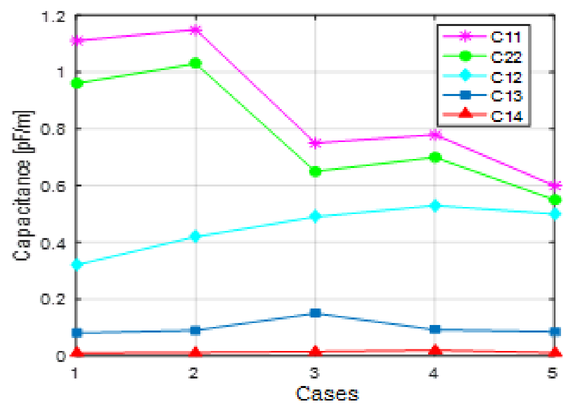

Figure 9. Capacitance per unit length vs. track geometry (of Figure 4)

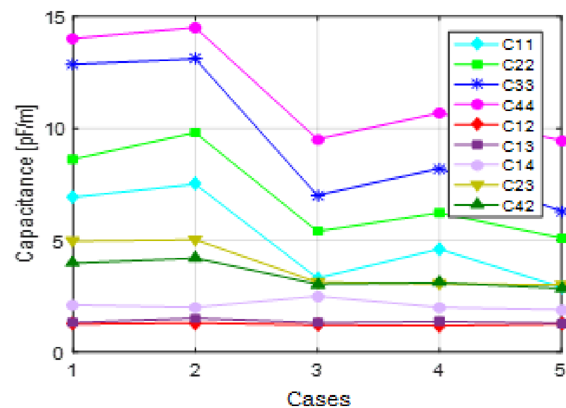

Figure 10. Capacitance per unit length vs. geometry of track (of Figure 5)

5. CONCLUSION

The motivation of our work is to calculate the parasitic capacitances between the interconnections in the integrated circuits. These capacitances are obtained by calculating the load on the surface of the conductors, that is, the normal derivative of the potential on the surface of these conductors. The resolution of the potential equation is done using the finite element method with Dirichlet type boundary conditions. The originality of this work was to propose a method based on the finite elements to study the problems of parasitic components as well as the optimization of the ideal interconnect geometry for which the parasitic effect is less important. We modeled the four-conductor interconnects lines with two dielectrics layers, we have identified the potential distribution of different geometries of the interconnection lines. The capacitance matrix and the inductance for each geometry have been calculated. Some geometric parameters have also been varied to remedy to parasitic capacitances problems. We have found that as the thickness of the dielectric layer increases, the parasitic capacitances between the tracks increase with the levels of interconnection. For higher level of interconnection, the capacitances with respect to ground plane decreases drastically. The results obtained with the finite element method agree with those found in the literature. Our method is simpler to implement and is of good accuracy.

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BIOGRAPHIES OF AUTHORS

Ahcene Lakhlef received his Electronics Engineering degree in 1988 and his MPhil degree in Microelectronics from the University of Sciences and Technology, Setif, Algeria, in 1994. He received his DSc degree in Microelectronics and Device Physics from MouloudMammeri University, Tizi-Ouzou, Algeria. He joined the University MouloudMammeri, Tizi-Ouzou, Algeria, in 1994. Currently, he is a Dsc researcher at the University M. Mammeri where he is also a lecturer. His research interests include reliability, testability, technology characterization of semi-conductors C(V) and I(V), and NBTI modeling.

Lounas Belhimer received the Master’s degree in the subject of Electric Drive from Mouloud Mammeri University, Tizi-Ouzou, Algeria in 2013, and received his Ph.D degree in Modeling and Desing of Electromagnetic System from MouloudMammeri University, Tizi-Ouzou, Algeria in 2020. His research interests include modeling of electromagnetic compatibility in microelectronics and nanotechnology devices.

Arezki Benfdila received his Electronics Engineering degree from the National Institute of Electricity and Electronics, INELEC, Boumerdes, Algeria, in 1989 and his MPhil degree in Microelectronics in the same institute in 1993. He received his DSc degree in Microelectronics and Device Physics from MouloudMammeri University, Tizi-Ouzou, Algeria. He joined the University M. Mammeri in 1993, and currently, he is a full professor and a research director. He is a Bureau Member of the National Microelectronics and Nanoelectronics Network and expert at ministry level in his field. His research interests include nanoelectronics, MOS devices and microelectronics. He directed several PhD theses. He hasbeen a friend and associate member of the ICTP-UNESCO-IAEA, Trieste, Italy from 2000 to 2020.