

# Voltage harmonics reduction in single phase 9-level transistor clamped H-bridge inverter using nearest level control method

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## ABSTRACT

This paper proposes a nearest level control method based modulation scheme for a 9-level symmetrical transistor clamped H-bridge (TCHB) inverter. The topology has gained increasing research focus due to its advantages in obtaining high-quality output while using a reduced number of electronic components. The device count for getting a 9-level output voltage is 10 switches compared to 16 switches being used in a conventional 9-level cascaded H-bridge (CHB) inverter. The significant contribution of the research is the development of the nearest level control (NLC) method that operates at the fundamental frequency, thus reducing switching losses, and able to reduce harmonic content significantly. The reduced harmonic content can lessen the power quality problem. The NLC modulation scheme shows that the overall THD is reduced without the need for filtration. The 50 values of harmonic content will be counted that follows the IEEE Standard 519. MATLAB/Simulink based simulations and experimental results obtained from the laboratory prototype of a single-phase TCHB inverter feeding an  $R$  load validate the theoretical analyses and effectiveness of the proposed modulation scheme.

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## 1. INTRODUCTION

Higher power drives are required by industrial users. The commercial drivers for this are higher production rates and improved efficiency with cost reduction [1-2]. To reduce the implementation cost, a reduced number of switches in a whole system is normally considered. The mature drive topologies, which are generally based on two-level inverters, are not capable of meeting ever-increasing power demands due to the lack of semiconductor devices that features adequate voltage and current ratings. Hence, high power demands are presently met using multilevel inverters (MLIs). Despite that, reliability is one of the significant issues of MLIs as they use a large number of switches in contrast to two-level inverters. Due to that, the TCHB inverter will be used and analyzed in this research work. The TCHB inverter is a recently developed topology which was first introduced in [3]. TCHB inverter is part of MLIs topologies that recently found used in the literatures [4-6]. MLIs include an array of devices and capacitors at different voltage levels. The increased levels in the output require more semiconductor switches in the system. However, it is worth mentioning that the device count for obtaining a 9-level output for TCHB inverter is 10 switches compared to the 16 being used in a conventional 9-level CHB inverter. In other words, the implementation of TCHB inverter is able to reduce the implementation cost due to the reduced number of switches employed and at the same time capable of improving the system reliability. This statement is supported in [7], which pointed out that the TCHB inverter

can easily be extended to any number of levels using very few active switches, thereby improving the reliability of the system. There are two types of TCHB that can be found in the literatures, which are TCHB with symmetrical arrangement and TCHB with asymmetrical arrangement. The Symmetrical arrangement exists when the DC voltage sources of the TCHB cells have equal values, whereas the asymmetrical arrangement exists when the DC input voltage values are different. Symmetrical and asymmetrical arrangements of TCHB inverter can be found in [8-11].

The modulation technique plays a significant role in determining the performance of the MLIs since it determines the voltage and current harmonics in the system. Previous studies have used modulation techniques that either operated in high- or low-switching frequency. The aim of this research work is to enhance the performance of the TCHB inverter by offering improved performance at lower switching frequencies. Hence, low-switching frequency modulation technique will be applied and analyzed in this research work. In the literatures, selective harmonic elimination (SHE) [12-17], nearest vector control (NVC) [18-19] and nearest level control (NLC) [20-22] modulation techniques are considered having and provide good performance results in low-switching frequency environment. Even though the SHE method is efficient in eliminating some significant low-order harmonics and obtaining better THD, it requires the solution of complex, non-linear transcendental equations. Iteration methods such as the newton-raphson (NR) method [15] or optimization algorithms such as particle swarm optimization (PSO) [16-17] are used to solve such equations. However, these methods are complicated, time-consuming and inappropriate for large numbers of levels. The working principle of NLC and NVC are approximately the same, except that, the NLC considers the nearest voltage level to the reference instead of the nearest vector in case of the NVC [23-24]. The NVC method requires additional computational resources because it is a simplified version of Space Vector Modulation [25-26]. Considering all relevant literatures, it can be stated that NLC is the simplest and most straightforward method among all low-switching frequency modulation techniques since NLC is able to reduce the overall THD value as well as demonstrating an excellent performance of the overall system. Not only that, but NLC also requires low computational time. In this research work, a comprehensive analysis of the NLC method will be provided. The proposed TCHB inverter with NLC method is analyzed in simulation and verified by experiments at different values of modulation index,  $M$ . The findings of this study indicated that the symmetrical TCHB inverter and its proposed control method are effective for obtaining better THD.

## 2. THE 9-LEVEL TCHB INVERTER

The configuration of a 9-level symmetrical TCHB inverter is illustrated in Figure 1. It consists of two identical TCHB cells powered by equal DC sources. Two switches of each TCHB cell (total of four) must conduct at the same time to generate any output level. The 9-level TCHB inverter is synthesized by adding the individual voltages of the two cascaded TCHB cells (1).

$$v_{inv} = v_1 + v_2 \quad (1)$$

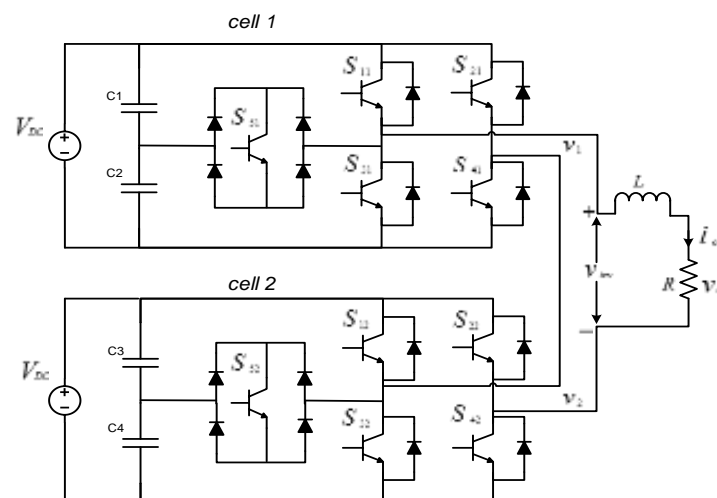


Figure 1. The 9-level symmetrical TCHB inverter

The output voltage waveforms of Cell-1, Cell-2 and the 9-level inverter are displayed in Figure 2(a) and (b). The switching angles are selected alternatively so that Cell-1 triggers at angles  $\theta_1$  and  $\theta_3$ , and Cell-2 switches at angles  $\theta_2$  and  $\theta_4$ , as shown in Figure 2(a). Using this arrangement, Cell-1 contributes to the output voltage of the inverter more than Cell-2, and this is due to the order in which the switching angles have been arranged. It is also possible that Cell-1 triggers at angles  $\theta_1$  and  $\theta_4$ , and Cell-2 triggers at angles  $\theta_2$  and  $\theta_3$ , as shown in Figure 2(b). This arrangement will make each cell contribute equally to the output.

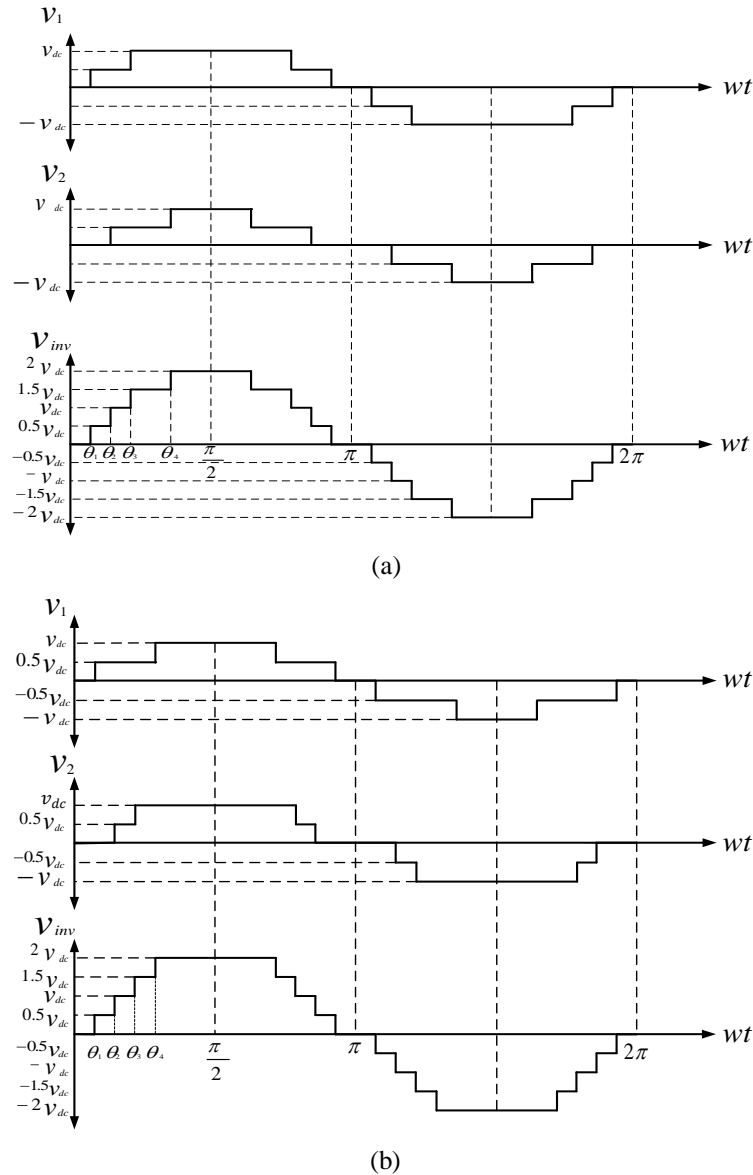


Figure 2. (a) Voltage waveforms for Cell-1, Cell-2 and the inverter, respectively, (b) Voltage waveforms Cell-1, Cell-2 and the inverter, respectively. (The second arrangement)

### 3. THE PROPOSED NLC METHOD

The basic principle of the NLC method applied to symmetrical 9-level TCHB inverter is illustrated in Figure 3. As shown in Figure 3(a), the reference is compared with the inverter voltage levels. In the beginning, the output remains at zero level for some time, then, when the reference is at  $0.25v_{dc}$  or above, the output switches to  $0.5v_{dc}$  level. It remains at  $0.5v_{dc}$  level until the reference reaches  $0.75v_{dc}$ , at which the output switches to  $v_{dc}$  level, and so on until all levels are obtained. Since each step of the TCHB inverter is of  $0.5v_{dc}$  magnitude, the maximum approximation error is  $0.25v_{dc}$ , as indicated in Figure 3(a). The NLC control logic for the TCHB inverter is illustrated in Figure 3(b).

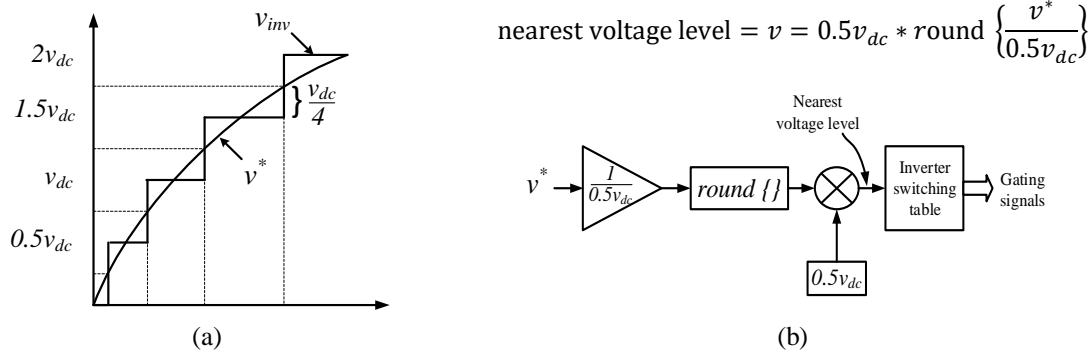


Figure 3. Nearest level control method (a) waveform synthesis (b) control diagram

The modulation index,  $M$  for symmetrical TCHB inverter is given by:

$$M = \frac{2V_{ref}}{s * V_{dc}} \tag{2}$$

where  $s$  is the number of steps in a quarter wave, and  $V_{ref}$  is the amplitude of the reference.

#### 4. ANALYSIS OF THE INVERTER OUTPUT VOLTAGE

The output waveform of the TCHB inverter is a quarter-wave symmetry, so, the output voltage can be represented using the fourier series as:

$$V_{inv}(wt) = \sum_{n=1}^{\infty} b_n \sin(nwt) \tag{3}$$

where  $b_n$  is the Fourier coefficient, and it equals zero for even  $n$ , but, for odd  $n$ , it is given by:

$$b_n = \frac{2v_{dc}}{n\pi} \sum_{i=1,3,5,\dots}^s \cos n\theta_i \tag{4}$$

where  $s$  is the number of switching angles (steps) in a quarter wave.  $\theta_i$  is the switching angle and should be within  $[0, \pi/2]$ . The switching angles ( $\theta_1 - \theta_4$ ) are calculated for a range of the modulation index from ( $M = 0.875$ ) to ( $M = 1.15$ ). At  $M = 0.875$ , the 9-level output starts. Below this point, less number of levels are obtained (less than nine levels). The switching angles are plotted against the modulation index for the given range, as shown in Figure 4. The switching angles for the 9-level symmetrical TCHB inverter using the NLC method are calculated using the following equation:

$$\theta_i = \sin^{-1} \left( \frac{i - 0.5}{4M} \right), \quad i = 1, 2, 3, 4 \tag{5}$$

The total harmonic distortion THD is calculated by:

$$THD = \frac{1}{Y_1} \sqrt{\sum_{n=2}^{\infty} Y_n^2} \tag{6}$$

where  $Y$  can be voltage or current. The voltage THD evaluated throughout a range of the modulation index is shown in Figure 5. Figure 5 demonstrates that as  $M$  increases, the voltage THD decreases, but after  $M = 1.08$ , the THD rises with the increase in  $M$ . The graph shows that the minimum voltage THD is obtained at  $M = 1.08$ , and it is equal to 7.87%. Table 1 illustrate the number of angles, the number of voltage levels and

the maximum obtained voltage of each level for the 9-level symmetrical TCHB inverter provided with the range of the modulation index.

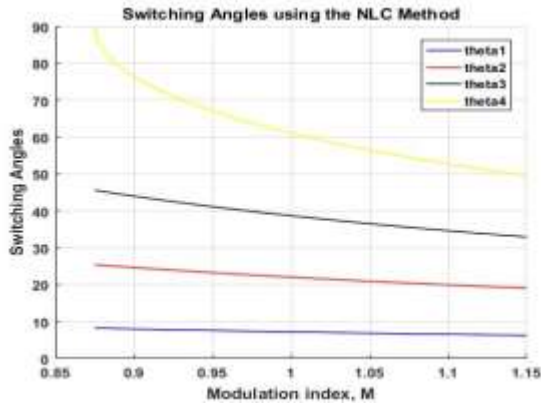


Figure 4. Switching angles versus the modulation index for the 9-level TCHB inverter

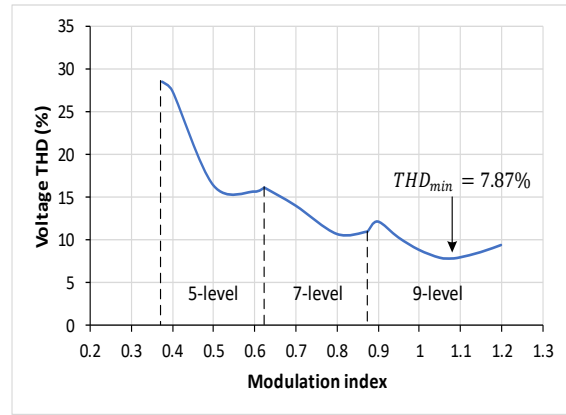


Figure 5. THD versus modulation index using NLC

Table 1. Number of angles, number of voltage levels and maximum voltage according to the modulation index

Modulation index, M	Number of Angles	Voltage levels	Maximum Voltage
$M \geq 0.875$	4	9	$2v_{dc}$
$0.625 \leq M < 0.875$	3	7	$1.5v_{dc}$
$0.375 \leq M < 0.625$	2	5	$v_{dc}$
$0.125 \leq M < 0.375$	1	3	$0.5v_{dc}$

## 5. RESULTS AND DISCUSSION

### 5.1. Simulation and experimental results

The assessment for the research work includes simulation and experimental work. The 9-level symmetrical TCHB inverter and its control method are simulated in MATLAB/Simulink. The block diagram of the simulation is illustrated in Figure 6, and an overview of the experimental setup is shown in Figure 7. The configuration is composed of two identical TCHB cells, which are supplied with equal DC sources. The parameters of the prototype are shown in Table 2 for the simulation and Table 3 for the experimental setup. The switching states are sampled in Matlab/Simulink at 5 us, and the sampled data is saved in look-up tables (LUTs), then the LUTs are processed using Quartus II software. These LUTs are loaded to the first FPGA, and another FPGA is used to provide a blanking time of 2 us to prevent the switches from being short-circuited. The output voltage and current of the inverter are displayed in Tektronix TDS 2024C oscilloscope. The voltage and current THDs are measured using Fluke 435 power quality analyzer.

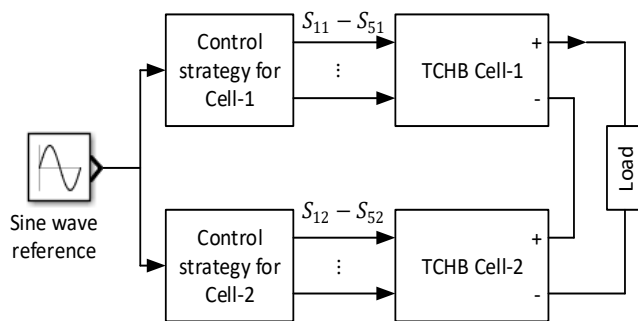


Figure 6. Block diagram for the simulation of the 9-level TCHB inverter and its control method

Table 2. System parameters used for simulation

Parameter	Value
DC voltage for cell-1 and cell-2	60 V
DC-link capacitors	2200 uF
Load resistance	100 Ohm
Fundamental frequency	50 Hz

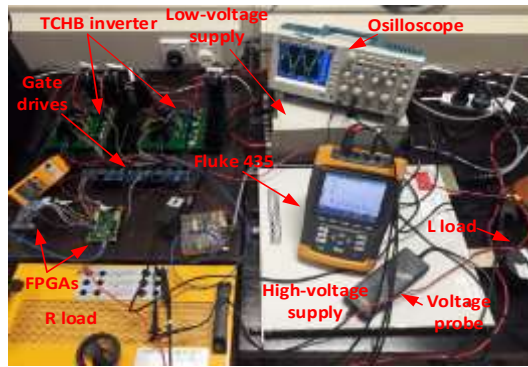


Figure 7. The experimental setup

Table 3. System parameters for experimental tests

Parameter	Value
DC voltage for <i>cell-1</i> and <i>cell-2</i>	60 V
IGBT	IRG4PC50UD
Power diodes	RHRG30120
DC-link capacitors	2200 uF
Load resistance	100 Ohm
FPGA for LUTs	Cyclone IV EP4CE22F17C6N
FPGA for blanking time	Cyclone IV EP4CE6E22C8
Fundamental frequency	50 Hz

Figure 8 shows the simulation results for the 9-level symmetrical TCHB inverter. Figures 8(a) and (b) are for a system with  $M = 1$ , and Figures 8(c) and (d) are for  $M = 1.08$ . Referring to Figure 5 shows that the system THD will be in the lowest value when  $M = 1.08$ . It is observed from the 9-level output voltages shown in Figures 8(a) and (c) that the THD for voltage when  $M = 1$  is 8.89% and around 7.87% when  $M = 1.08$ , as shown in Figures 8(b) and (d) respectively. There is a decrease of about 1.02% between both modulation indices.

To verify the simulation results, the same values of the modulation index are observed for the experimental results. The same settings and machine parameters used in the simulation are used in experimental work, as stated in Tables 2 and 3. Voltage THDs for these values of the modulation index are shown in Figure 9. When  $M = 1$ , the displayed result shows that the THD of the voltage is 9.1%, as shown in Figure 9(b), which indicates a difference of 0.21% between simulation and experiments. While for  $M = 1.08$ , the voltage THD is 8.0%, as shown in Figure 9(d), with 0.13% difference compared to the simulation results. The slight difference between the simulation and experimental results shows that the NLC method is able to reduce the THD in the system. It should be pointed out that the displayed THD in the Fluke 435 is only for the first 50 harmonics and not for all harmonics. The NLC method demonstrated that the strategy does not eliminate specific harmonics like the SHE method, which eliminates some low-order harmonics; rather, it minimizes the overall THD of the inverter.

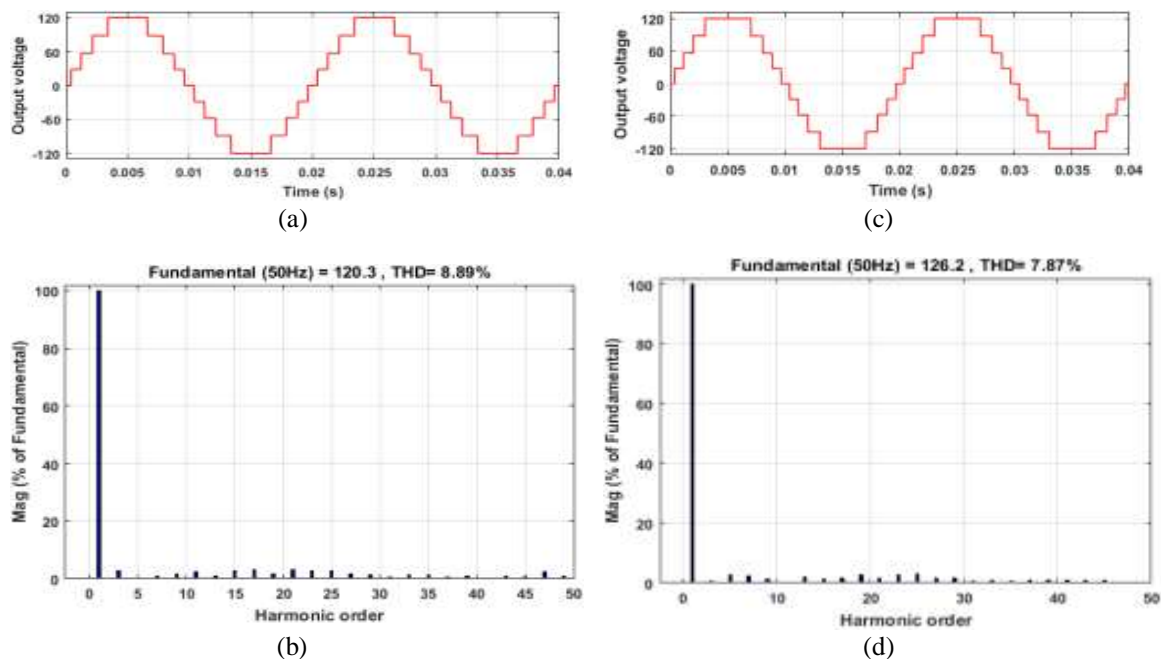


Figure 8. Simulation results using  $R$  load (a) output voltage waveform at  $M = 1$ , (b) voltage THD at  $M = 1$ , (c) output voltage waveform at  $M = 1.08$  and (d) voltage THD at  $M = 1.08$

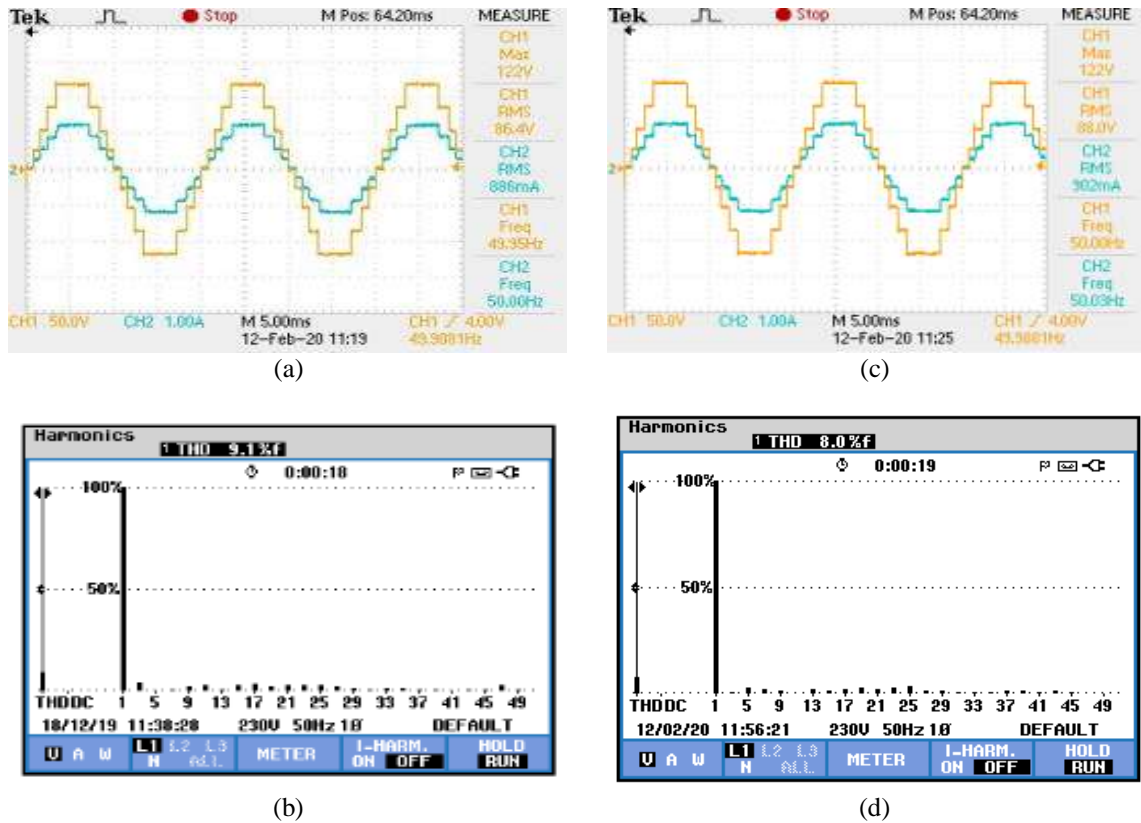


Figure 9. Experimental results using  $R$  load (a) output voltage waveform at  $M = 1$ , (b) voltage THD at  $M = 1$ , (c) output voltage waveform at  $M = 1.08$  and (d) voltage THD at  $M = 1.08$

## 6. CONCLUSION

This paper presents an NLC modulation scheme for the 9-level symmetrical TCHB inverter. TCHB having a reduced number of total device count compared to other multilevel inverter topologies is an asset. The experimental validations performed, confirmed that the strategy implemented is effective in reducing the harmonic content in the voltage at the fundamental frequency. The experimental results show a good agreement with the analyses done in simulation. As far as the voltage harmonic is concerned, the NLC modulation scheme offers simplicity in the technique. Not only that, the overall THD is reduced without the need for filtration.

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