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Comparative investigation of 15 level and 17 level cascaded H-Bridge MLI with cross H-Bridge MLI fed permanent magnet synchronous motor

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ABSTRACT

Multilevel inverters offers eminent solutions to high voltage high power applications due to the association of several devices in a series configuration. In this paper, a comparative investigation of both 15 and 17 level cascaded H-Bridge multi level inverter with cross H-Bridge fed permanent magnet synchronous motor are presented by appropriate simulations and mathematical analysis. Comparative analysis includes Inverter output voltage and current, number of switching devices, stator current and speed of PMSM and total harmonic distortion levels. Limitation of several switching devices, which can afford high voltage in the inverter is the major problems raised in this study. The advantage of this analysis is to figure out the appropriate inverter that can be used for real time application by considering the factors via. Harmonic distortion, output voltage, current, number of switching devices etc. Validation of the analysis is processed through Matlab/Simulink Platform.

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1. INTRODUCTION

Micro grids are increasing day by day, which is combination of many sources like Diesel Generators, Solar power, Wind power, Fuel cell etc. To integrate these sources with power grid or to supply power to local loads power electronic converters play an important role. The two-level inverter cannot supply the power to medium and high power loads with good efficiency but multilevel inverters can supply the power at good efficiency.

The primary principle of MLI is to share the operating voltage of inverter between switches connected in circuit. So switches with low rating can be used in high voltage/power rating applications, which reduce the cost of inverter. As level of output voltage increases level of harmonics decreases at low switching frequencies so cost of filters reduces [1, 2].

The major topologies of multilevel inverters are Diode clamped (NPC) multilevel inverter [3], Capacitor clamped (FC) multilevel inverter [4] and Cascaded H bridge (CHB) multilevel inverter [5]. The common problem among above topologies is number of switches required [6, 7] increases significantly with increase in output voltage level [8], which tends to increase in cost, size and complexity of switching and implementation of hardware circuit [9-11]. The NPC multilevel inverter and the FC multilevel inverter, the

capacitor voltage can be regulated using redundant switching states but as the level of voltage increase the number of capacitors and clamping diodes required and complexity in control scheme increases.

In cascaded H bridge multilevel inverter, the H-Bridge cells with DC source are connected in series. Based on the type of DC sources CHB multilevel inverter is classified as symmetrical (equal DC sources) [12-14] and asymmetrical (unequal DC sources) [15-17]. The symmetric topology gives good modularity and packaging due to the identical structure of each H – Bridge but number of switches increases rapidly with the increase in level of output voltage. With asymmetric topology the level of output voltage can be increased with less number of switches but the rating of some of the switches is nearly equal the maximum operating voltage and designing of hardware circuit is more challeging. The topologies discussed above are conventional. Many topologies are invented in recent years. The cross H bridge multilevel inverter [18] is connected with specific cross connections with DC sources as shown in Figure 2 and Figure 4. Due to enormous applications there is a huge attention on multilevel inverters. Multilevel output generated using multi winding transformer [19, 20] is not economical for high power/voltage applications.

In this paper, a comparative investigation of 15 and 17level MLI for both cascade and cross H-Bridge switching configurations are presented, for both cascaded & cross H-Bridge inverter level of harmonic content reduces with the increase in the level of voltage. The proposed 3-phase 15 & 17- level multilevel inverter is fed to PMSM and verified speed and stator current of the motor.

2. SWITCHING PROFILE

2.1. The relation between level of output voltage, number of switches and number of voltage sources

Cross H Bridge:

$$N_s=V_L+1 \quad (1)$$

$$V_L=2*V_s+1 \quad (2)$$

$$N_s=2(V_s+1) \quad (3)$$

$$N_D=\frac{V_L+1}{2} \quad (4)$$

Cascaded H Bridge:

$$N_s=2*(V_L-1) \quad (5)$$

$$V_L=2*V_s+1 \quad (6)$$

$$N_s=4*V_s \quad (7)$$

$$N_D=V_L-1 \quad (8)$$

Where V_L is level of output voltage, N_s is number of switches, V_s is number of voltage sources, N_D=no. of switching devices in current path. Comparison of number of switches for the above two topologies is shown Table 3.

2.2. Switches voltage rating

In cross H bridge MLI the standing voltage of switches S_1,S_2,S_{n-1} andS_n is V_{dc} and other switches standing voltage [21-23] is $2V_{dc}$ and the standing voltage of all switches in cascaded H bridge is $V_{dc.}$ The total standing Voltage of cross H brige MLI and cascaded H bridge is = $2*(V_L-1)*V_{dc}$

Where V_L is level of output voltage.

2.3. Switch losses

The major losses of the switches are conduction and switching losses [24-26]. Conduction losses occur due to on-state voltage drop and equivalent resistance. Switching losses occur due to non ideal operation of switches. The average conduction losses of a transistor $(P_c, T(t))$ and diode $(P_c, D(t))$can be written as follows:

$$P_c, T=\frac{1}{2\pi}\int[V_T+R_T i^{\beta}(t)]\ i(t)d(\omega t) \quad (9)$$

$$P_c, D = \frac{1}{2\pi}\int [V_D + R_D i(t)] i(t)\, d(\omega t) \quad (10)$$

The total conduction losses of multilevel inverter per cycle (P_c) = $(P_c, T + P_c, D)$*N_D (11)

The switching loss of the switches is given as $P(sw) = f * (T_{on} * E_{on} + T_{off} * T_{off} * E_{off})$ (12)

Where V_T and $V_D$are transistor and diode voltage drop (on state) respectively. R_T and R_D are transistor and diode equivalent resistance respectively, f= frequency, T_{on}=no. of times switches on, T_{off}=no. of times switches off. Comparison of switching losses of discussed topologies are shown in Table 4.

3. 15-LEVEL MULTILEVEL INVERTER

3.1. Cascaded H-Bridge

Figure 1 shows cascaded H-Bridge 15-level MLI with seven dc sources and 28 switches. Four switches comprise one leg and each leg is connected to one dc source of same voltage rating.

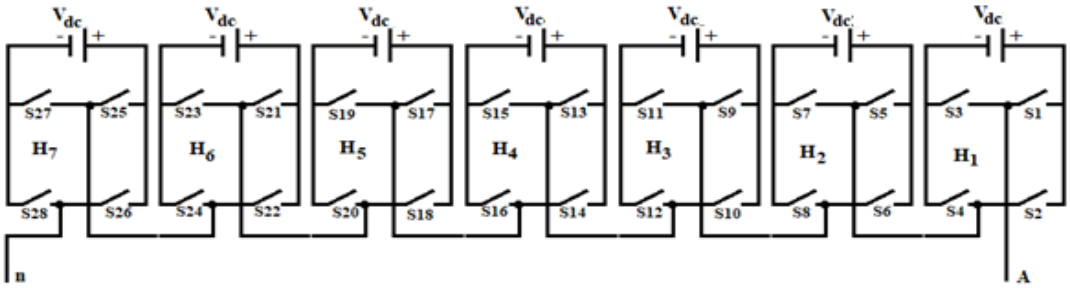

Figure 1. Single phase 15-level cascaded H-Bridge MLI

3.2. Cross H-Bridge

From (1) number of switches required in cross H-Bridge MLI is 2(V_s+1) = 2*(7+1) = 16 switches, the same can be seen from Figure 2. Where V_s is number of voltage sources. Switching configuration for Single Phase 15-level Cross H-Bridge MLI is shown in Table 1. For each output voltage there are various switching patterns as shown in Table 1. However for the complete analysis the highlited switching pattern (in bold) is considered. The conduction path for +5Vdc is shown in Figure 2(b).

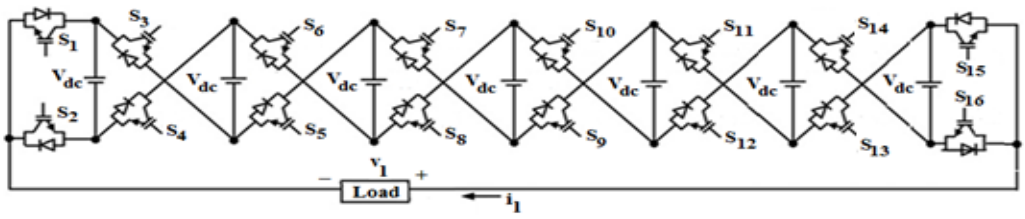

Figure2(a). Single phase 15-level cross H-Bridge MLI

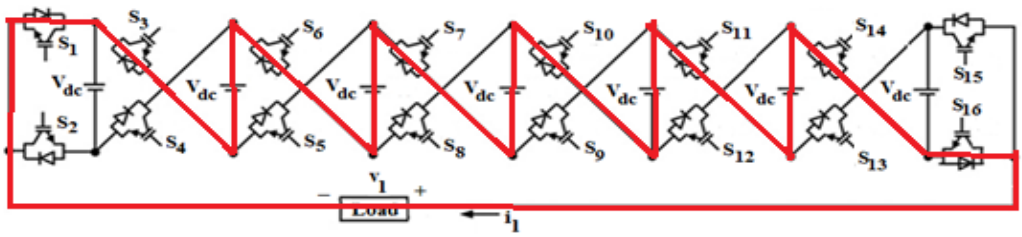

Figure2(b). Conduction path for +5Vdc of 15-level cross H-Bridge MLI

Table 1. Switching pattern of cross H-Bridge 15-level MLI

S.No.	O/P Voltage	Switches ON	S.No.	O/P Voltage	Switches ON
1	7 V_{DC}	$S_2S_3S_6S_7S_{10}S_{11}S_{14}S_{15}$	9	- 7 V_{DC}	$S_1S_4S_5S_8S_9S_{12}S_{13}S_{16}$
2	6 V_{DC}	$S_1S_3S_6S_7S_{10}S_{11}S_{14}S_{15}$ $S_2S_3S_6S_7S_{10}S_{11}S_{14}S_{16}$	10	- 6 V_{DC}	$S_1S_4S_5S_8S_9S_{12}S_{13}S_{15}$ $S_2S_4S_5S_8S_9S_{12}S_{13}S_{16}$
3	5 V_{DC}	$S_1S_3S_6S_7S_{10}S_{11}S_{14}S_{16}$ $S_2S_3S_6S_7S_{10}S_{11}S_{13}S_{15}$ $S_2S_4S_6S_7S_{10}S_{11}S_{14}S_{15}$	11	- 5 V_{DC}	$S_1S_4S_5S_8S_9S_{12}S_{14}S_{16}$ $S_1S_3S_5S_8S_9S_{12}S_{13}S_{16}$ $S_2S_4S_5S_8S_9S_{12}S_{13}S_{15}$
4	4 V_{DC}	$S_1S_3S_6S_7S_{10}S_{11}S_{13}S_{15}$ $S_1S_3S_6S_7S_{10}S_{11}S_{14}S_{15}$ $S_2S_3S_6S_7S_{10}S_{12}S_{14}S_{16}$ $S_2S_4S_6S_7S_{10}S_{11}S_{14}S_{16}$ $S_1S_3S_6S_7S_{10}S_{12}S_{14}S_{16}$	12	- 4 V_{DC}	$S_1S_4S_5S_8S_9S_{11}S_{13}S_{15}$ $S_1S_3S_5S_8S_9S_{12}S_{13}S_{15}$ $S_2S_4S_5S_8S_9S_{12}S_{14}S_{16}$ $S_2S_4S_6S_8S_9S_{12}S_{13}S_{16}$ $S_1S_3S_5S_8S_{10}S_{12}S_{14}S_{16}$
5	3 V_{DC}	$S_1S_3S_5S_7S_{10}S_{11}S_{14}S_{16}$ $S_2S_3S_6S_7S_9S_{11}S_{13}S_{15}$ $S_2S_4S_6S_7S_{10}S_{11}S_{13}S_{15}$ $S_2S_4S_6S_8S_{10}S_{11}S_{14}S_{15}$ $S_1S_3S_6S_7S_9S_{11}S_{13}S_{15}$	13	- 3 V_{DC}	$S_1S_3S_5S_8S_9S_{12}S_{14}S_{16}$ $S_1S_3S_5S_7S_9S_{12}S_{13}S_{16}$ $S_2S_4S_5S_8S_9S_{11}S_{13}S_{15}$ $S_2S_4S_6S_8S_9S_{12}S_{13}S_{15}$ $S_1S_4S_5S_7S_9S_{11}S_{13}S_{15}$
6	2 V_{DC}	$S_1S_3S_5S_7S_{10}S_{11}S_{13}S_{15}$ $S_1S_3S_5S_7S_9S_{11}S_{14}S_{15}$ $S_2S_3S_6S_8S_{10}S_{12}S_{14}S_{16}$ $S_2S_4S_6S_7S_{10}S_{12}S_{14}S_{16}$ $S_2S_4S_6S_8S_{10}S_{11}S_{14}S_{16}$ $S_1S_3S_6S_8S_{10}S_{12}S_{14}S_{16}$	14	- 2 V_{DC}	$S_1S_4S_5S_8S_9S_{11}S_{13}S_{15}$ $S_1S_3S_5S_7S_9S_{12}S_{13}S_{15}$ $S_2S_4S_5S_8S_{10}S_{12}S_{14}S_{16}$ $S_2S_4S_6S_8S_9S_{12}S_{14}S_{16}$ $S_2S_4S_6S_8S_{10}S_{12}S_{13}S_{16}$
7	V_{DC}	$S_1S_3S_5S_7S_{10}S_{12}S_{14}S_{16}$ $S_1S_3S_5S_7S_9S_{11}S_{14}S_{16}$ $S_2S_3S_5S_7S_9S_{11}S_{13}S_{15}$ $S_2S_4S_6S_7S_9S_{11}S_{13}S_{15}$ $S_2S_4S_6S_8S_{10}S_{12}S_{13}S_{15}$ $S_2S_4S_6S_8S_{10}S_{12}S_{14}S_{15}$	15	- V_{DC}	$S_1S_4S_6S_8S_{10}S_{12}S_{14}S_{16}$ $S_1S_3S_5S_8S_{10}S_{12}S_{14}S_{16}$ $S_1S_3S_5S_7S_9S_{12}S_{14}S_{16}$ $S_1S_3S_5S_7S_9S_{11}S_{13}S_{16}$ $S_2S_4S_5S_7S_9S_{11}S_{13}S_{15}$ $S_2S_4S_6S_8S_9S_{11}S_{13}S_{15}$ $S_2S_4S_6S_8S_{10}S_{12}S_{13}S_{15}$
8	0	$S_1S_3S_5S_7S_9S_{11}S_{13}S_{15}$ $S_2S_4S_6S_8S_{10}S_{12}S_{14}S_{16}$			

4. 17-LEVEL MULTILEVEL INVERTER

4.1. Cascaded H-Bridge

Figure 3 shows cascaded H-Bridge 17-level MLI with eight dc sources and 32 switches. Four switches comprise one leg and each leg is connected to one dc source of same voltage rating.

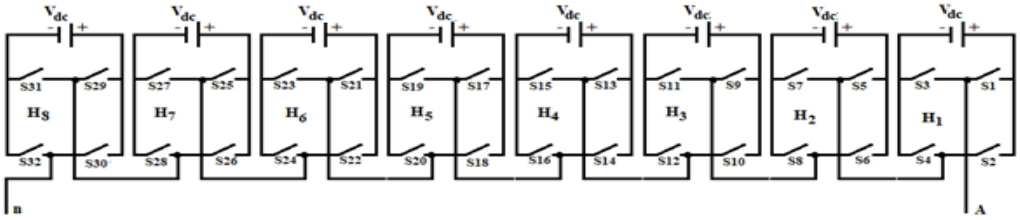

Figure 3. Single phase 17-level cascaded H-Bridge MLI

4.2. Cross H-Bridge

From (1) number of switches required in cross H-Bridge MLI is $2(V_s+1) = 2*(8+1) = 18$ switches, the same can be seen from Figure 4. Where V_s is number of voltage sources.

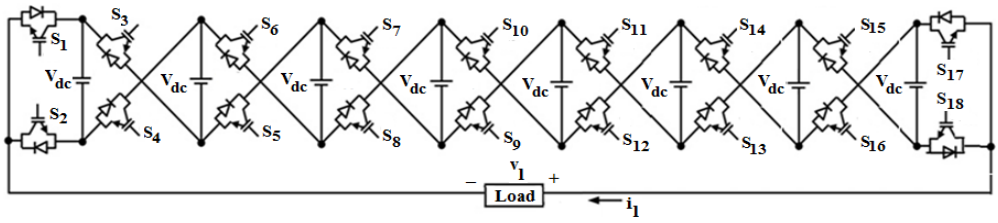

Figure 4. Single phase 17-level cross H-Bridge MLI

Table 2. Switching pattern of cross H-Bridge 17-level MLI

S.No.	O/P Voltage	Switches ON	S.No.	O/P Voltage	Switches ON
1	8 V_{DC}	$S_2S_3S_6S_7S_{10}S_{11}S_{14}S_{15}S_{18}$	10	- 8 V_{DC}	$S_1S_4S_5S_8S_9S_{12}S_{13}S_{16}S_{17}$
2	7 V_{DC}	$S_2S_3S_6S_7S_{10}S_{11}S_{14}S_{15}S_{17}$ $S_1S_3S_6S_7S_{10}S_{11}S_{14}S_{15}S_{18}$	11	- 7 V_{DC}	$S_1S_4S_5S_8S_9S_{12}S_{13}S_{16}S_{18}$ $S_2S_4S_5S_8S_9S_{12}S_{13}S_{16}S_{17}$
3	6 V_{DC}	$S_2S_3S_6S_7S_{10}S_{11}S_{14}S_{16}S_{18}$ $S_2S_4S_6S_7S_{10}S_{11}S_{14}S_{15}S_{18}$ $S_1S_3S_6S_7S_{10}S_{11}S_{14}S_{15}S_{18}$	12	- 6 V_{DC}	$S_1S_4S_5S_8S_9S_{12}S_{13}S_{15}S_{17}$ $S_1S_3S_5S_8S_9S_{12}S_{13}S_{16}S_{17}$ $S_2S_4S_5S_8S_9S_{12}S_{13}S_{16}S_{18}$
4	5 V_{DC}	$S_2S_3S_6S_7S_{10}S_{11}S_{13}S_{15}S_{17}$ $S_2S_4S_6S_7S_{10}S_{11}S_{14}S_{15}S_{17}$ $S_1S_3S_6S_7S_{10}S_{11}S_{14}S_{16}S_{18}$ $S_1S_3S_5S_7S_{10}S_{11}S_{14}S_{15}S_{18}$	13	- 5 V_{DC}	$S_1S_4S_5S_8S_9S_{12}S_{14}S_{16}S_{18}$ $S_1S_3S_5S_8S_9S_{12}S_{13}S_{16}S_{18}$ $S_2S_4S_5S_8S_9S_{12}S_{13}S_{15}S_{17}$ $S_2S_4S_5S_8S_{10}S_{12}S_{13}S_{16}S_{17}$
5	4 V_{DC}	$S_2S_3S_6S_7S_{10}S_{12}S_{14}S_{16}S_{18}$ $S_2S_4S_6S_7S_{10}S_{11}S_{14}S_{16}S_{18}$ $S_2S_4S_6S_8S_{10}S_{11}S_{14}S_{15}S_{18}$ $S_1S_3S_6S_7S_{10}S_{11}S_{13}S_{15}S_{17}$ $S_1S_3S_5S_7S_{10}S_{11}S_{14}S_{15}S_{17}$	14	- 4 V_{DC}	$S_1S_4S_5S_8S_9S_{11}S_{13}S_{15}S_{17}$ $S_1S_3S_5S_8S_9S_{12}S_{13}S_{15}S_{17}$ $S_1S_3S_5S_7S_9S_{12}S_{13}S_{16}S_{17}$ $S_2S_4S_5S_8S_9S_{12}S_{14}S_{16}S_{18}$ $S_2S_4S_6S_8S_9S_{12}S_{13}S_{16}S_{18}$
6	3 V_{DC}	$S_2S_3S_6S_7S_9S_{11}S_{13}S_{15}S_{17}$ $S_2S_4S_6S_7S_{10}S_{11}S_{13}S_{15}S_{17}$ $S_2S_4S_6S_8S_{10}S_{11}S_{14}S_{15}S_{17}$ $S_1S_3S_6S_7S_{10}S_{12}S_{14}S_{16}S_{18}$ $S_1S_3S_5S_7S_{10}S_{11}S_{14}S_{16}S_{18}$	15	- 3 V_{DC}	$S_1S_4S_5S_8S_{10}S_{12}S_{14}S_{16}S_{18}$ $S_1S_3S_5S_8S_9S_{12}S_{14}S_{16}S_{18}$ $S_1S_3S_5S_7S_9S_{12}S_{13}S_{16}S_{18}$ $S_2S_4S_5S_8S_9S_{12}S_{14}S_{16}S_{18}$ $S_2S_4S_6S_8S_9S_{12}S_{13}S_{15}S_{17}$
7	2 V_{DC}	$S_1S_3S_5S_7S_9S_{11}S_{14}S_{15}S_{18}$ $S_2S_3S_6S_8S_{10}S_{12}S_{14}S_{16}S_{18}$ $S_2S_4S_6S_7S_{10}S_{12}S_{14}S_{16}S_{18}$ $S_2S_4S_6S_8S_{10}S_{11}S_{14}S_{16}S_{18}$ $S_2S_4S_6S_8S_{10}S_{12}S_{14}S_{15}S_{18}$ $S_1S_3S_6S_7S_9S_{11}S_{13}S_{15}S_{17}$ $S_1S_3S_5S_7S_{10}S_{11}S_{13}S_{15}S_{17}$	16	- 2 V_{DC}	$S_2S_4S_6S_8S_{10}S_{12}S_{13}S_{16}S_{17}$ $S_1S_4S_5S_7S_9S_{11}S_{13}S_{15}S_{17}$ $S_1S_3S_5S_8S_9S_{11}S_{13}S_{15}S_{17}$ $S_1S_3S_5S_7S_9S_{12}S_{13}S_{15}S_{17}$ $S_1S_3S_5S_7S_9S_{11}S_{13}S_{16}S_{17}$ $S_2S_4S_5S_8S_{10}S_{12}S_{14}S_{16}S_{18}$ $S_2S_4S_6S_8S_9S_{12}S_{14}S_{16}S_{18}$
8	V_{DC}	$S_1S_3S_5S_7S_9S_{14}S_{15}S_{17}$ $S_1S_3S_5S_7S_9S_{11}S_{13}S_{15}S_{18}$ $S_1S_3S_5S_7S_9S_{11}S_{14}S_{16}S_{18}$ $S_1S_3S_5S_7S_{10}S_{12}S_{14}S_{16}S_{18}$ $S_1S_3S_6S_8S_{10}S_{12}S_{14}S_{16}S_{18}$ $S_2S_3S_5S_7S_9S_{11}S_{13}S_{15}S_{17}$ $S_2SS_4S_6S_7S_9S_{11}S_{13}S_{15}S_{17}$ $S_2S_4S_6S_8S_{10}S_{11}S_{13}S_{15}S_{17}$ $S_2S_4S_6S_8S_{10}S_{12}S_{14}S_{15}S_{17}$	17	- V_{DC}	$S_2S_4S_5S_7S_9S_{12}S_{14}S_{16}S_{18}$ $S_1S_3S_5S_7S_9S_{12}S_{14}S_{16}S_{18}$ $S_1S_3S_5S_7S_9S_{11}S_{13}S_{16}S_{18}$ $S_2S_4S_5S_7S_9S_{11}S_{13}S_{15}S_{17}$ $S_2S_4S_6S_8S_9S_{11}S_{13}S_{15}S_{17}$ $S_2S_4S_6S_8S_{10}S_{12}S_{13}S_{15}S_{17}$ $S_2S_4S_6S_8S_{10}S_{12}S_{14}S_{16}S_{17}$
9	0	$S_1S_3S_5S_7S_9S_{11}S_{13}S_{15}S_{17}$ $S_2S_4S_6S_8S_{10}S_{12}S_{14}S_{16}S_{18}$			

The number of switches required for 15-level cross H bridge is reduced by42.8% per phase when compared to 15-level cascaded H bridge and number of switches required for 17-level cross H bridge is reduced by43.7% when compared to 17-level cascaded H bridge per phase this can be observed from Table 3. The losse of 15-level cross H bridge is reduced by 24.1% per phase when compared to 15-level cascaded H bridge and the losse of 17-level cross H bridge is reduced by 24.8% per phase when compared to 17-level cascaded H bridge this can be observed from Table 4.

Table 3. Number of switching devices vs output voltage levels

OUTPUT VOLTAGE LEVELS	No. of Switching Devices			
	Cascaded H-Bridge MLI		Cross H- Bridge MLI	
	1-Phase	3-Phase	1-Phase	3-Phase
15 LEVEL	28	84	16	48
17 LEVEL	32	96	18	54

Table 4. Total losses of switches vs output voltage levels

OUTPUT VOLTAGE LEVELS	Total losses of switches(w)			
	Cascaded H-Bridge MLI		Cross H- Bridge MLI	
	Single Phase	Three Phase	Single Phase	Three Phase
15 LEVEL	17.13	51.39	12.99	38.97
17 LEVEL	19.08	57.24	14.33	42.99

5. RESULTS

In this paper simulation of 15-level and 17-level cross H bridge and cascaded H bridge multilevel inverters is carried in MATALB/SIMULINK environment with seven and eight separate DC sources of 10V

to get 70V and 80V maximum output voltage respectively. The switch IGBT (FGA15N120ANTD) is considered for calculating the switch losses and the Permanent Magnet Synchronous Motor of rating of 0.5hp connected as load. Comparison of losses of cross H Bridge and Cascaded H bridge topologies is shown in Table 4.

5.1. 15-level cascaded H-Bridge inverter fed PMSM

Figures 5-8 represents stator current Phase-A, three phse inverter voltage, speed of motor and THD of 15- Level Cascaded H-Bridge MLI respectively

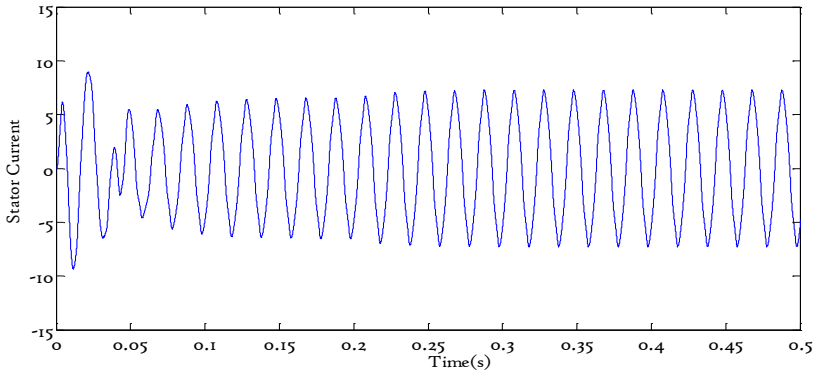

Figure 5. Stator current of Phase-A

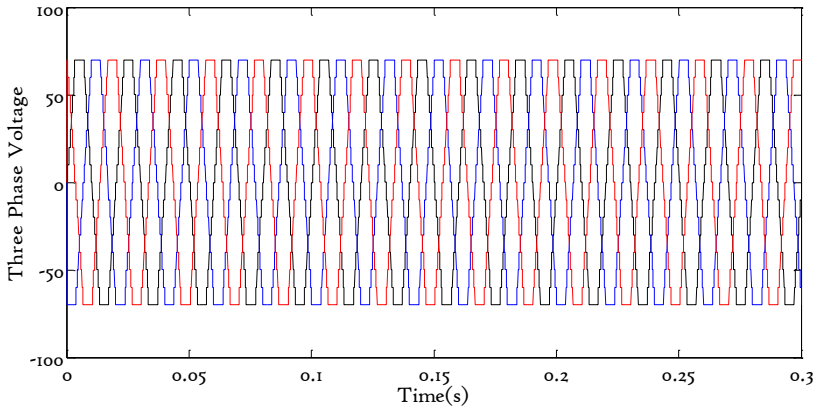

Figure 6. Three phase 15-level cascaded H-Bridge inverter output voltage

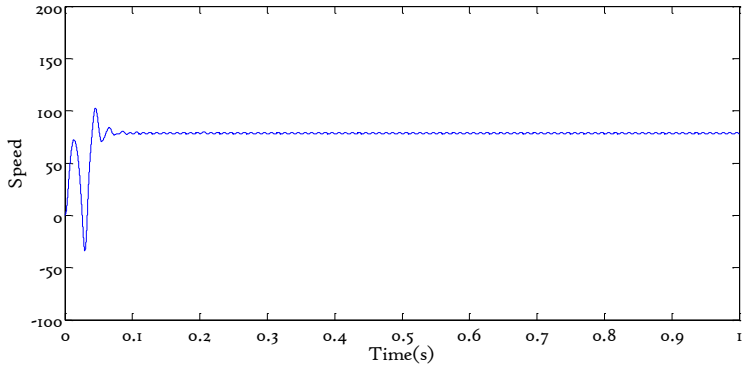

Figure 7. Speed of PMSM

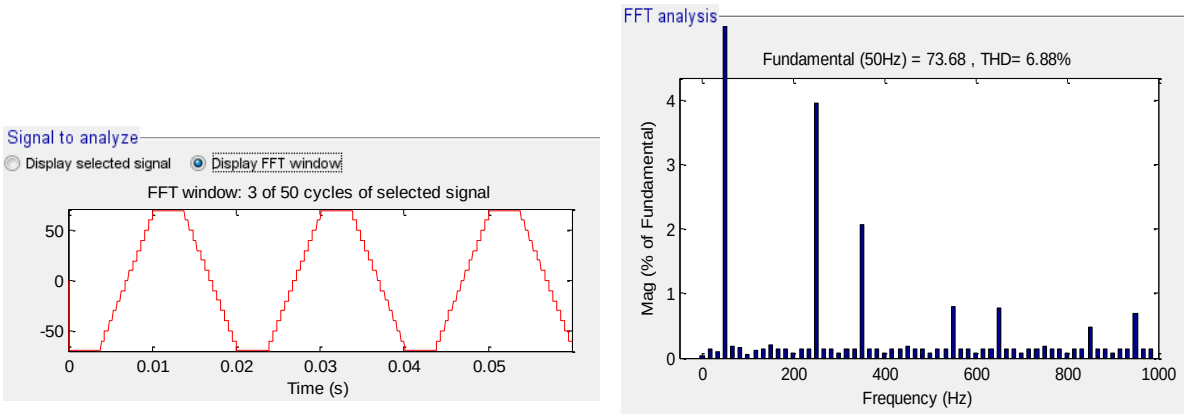

Figure 8. Total harmonic distortion of 15- level cascaded H-Bridge MLI (Phase A)

5.2. 15-level cross H-Bridge inverter fed PMSM

Figures 9-12 represents stator current Phase-A, three phse inverter voltage, speed of motor and THD of 15- Level Cross H-Bridge MLI respectively. The Total Harmonic Distortion of 15- Level Cross H-Bridge is reduced by 3.48% when compared to 15-level cascaded H-Bridge the same can be observed from Figure 8 and Figure 12.

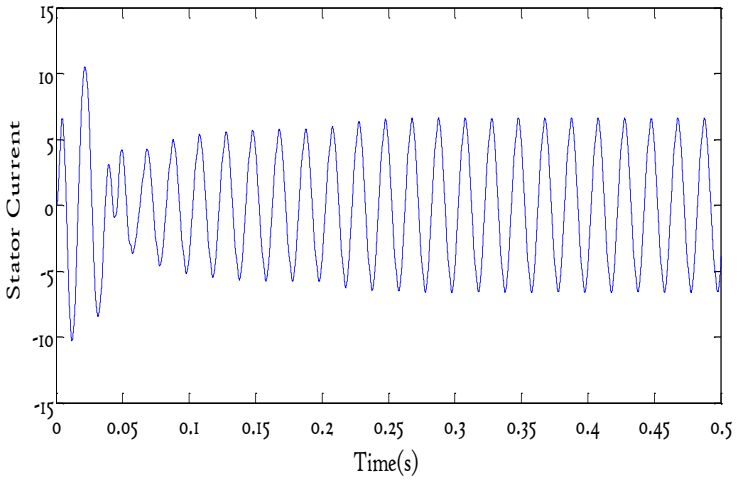

Figure 9. Stator current of Phase-A

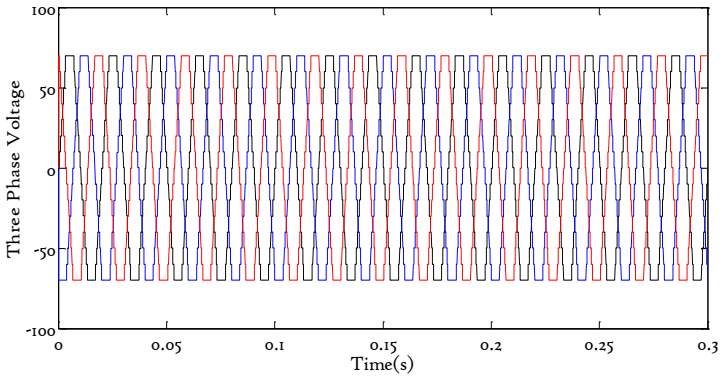

Figure 10. Three phase 15-level cross H-Bridge inverter output voltage

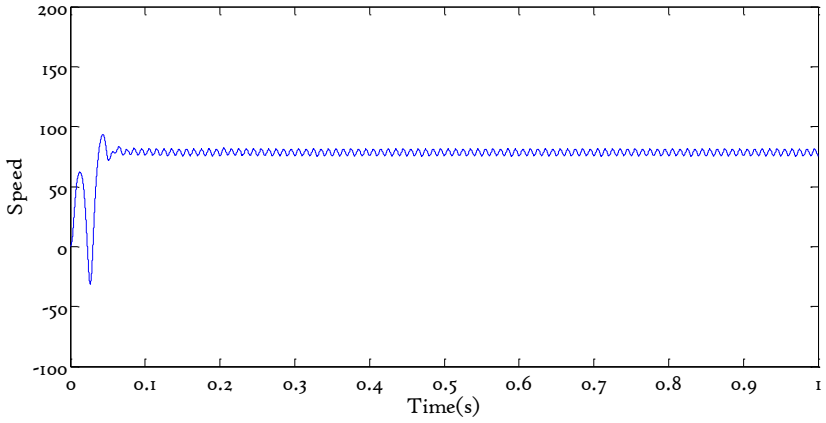

Figure 11. Speed of PMSM

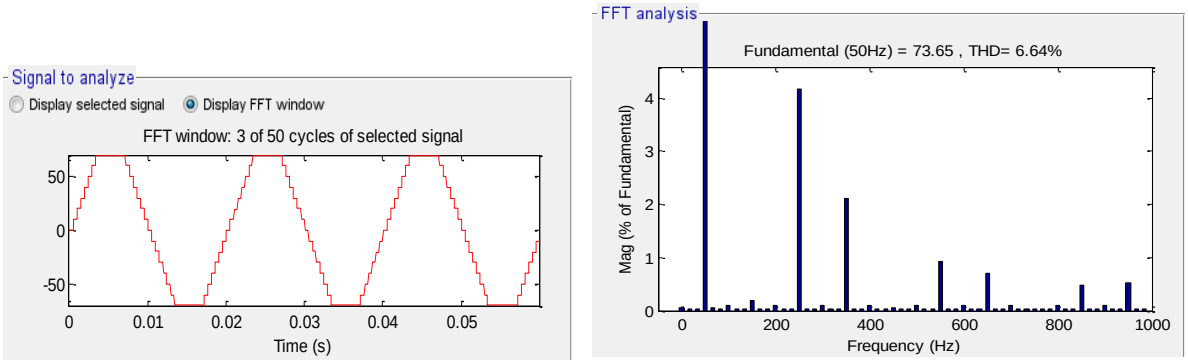

Figure 12. Total harmonic distortion of 15 level cross H-Bridge MLI (Phase A)

5.3. 17- level cascaded H-Bridge inverter fed PMSM

Figures 13-16 represents stator current Phase-A, three phse inverter voltage, speed of motor and THD of 17- Level Cascaded H-Bridge MLI respectively.

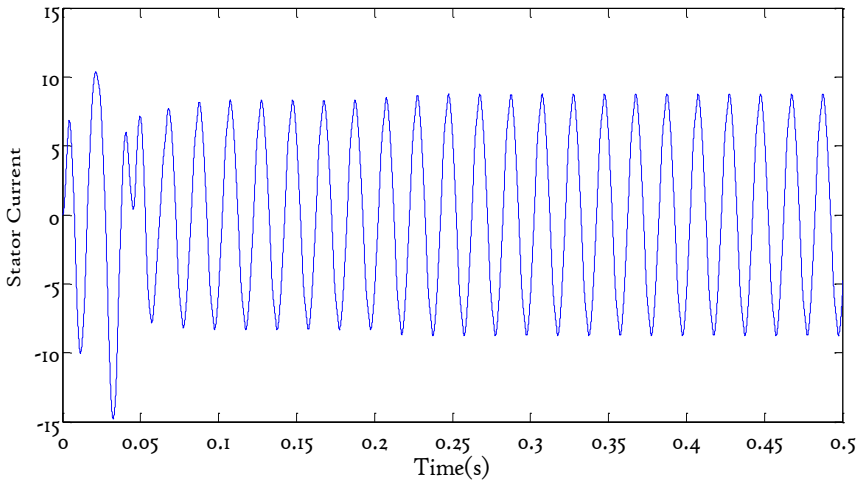

Figure 13. Stator current of Phase-A

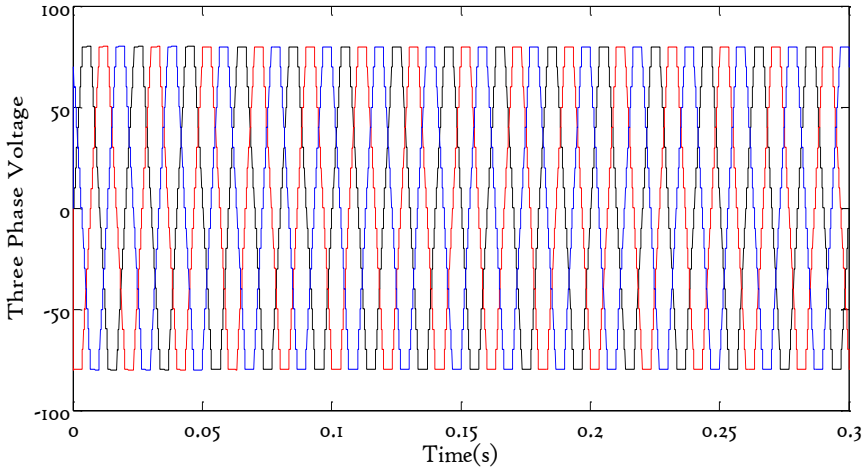

Figure 14. Three phase 17-level cascaded H-Bridge inverter output voltage

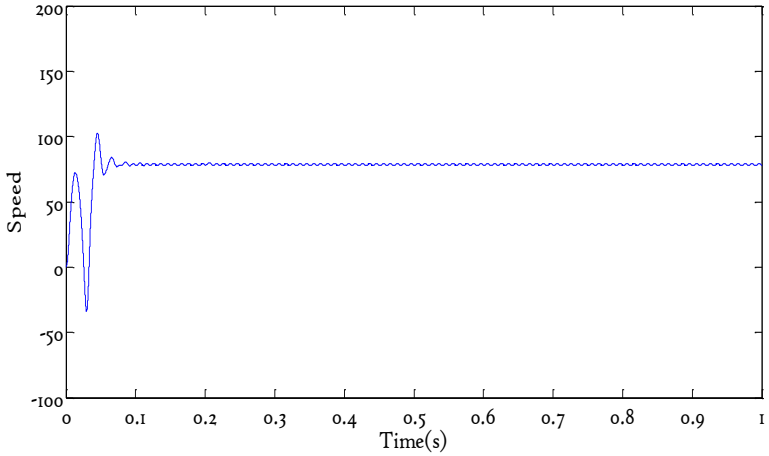

Figure 15. Speed of PMSM

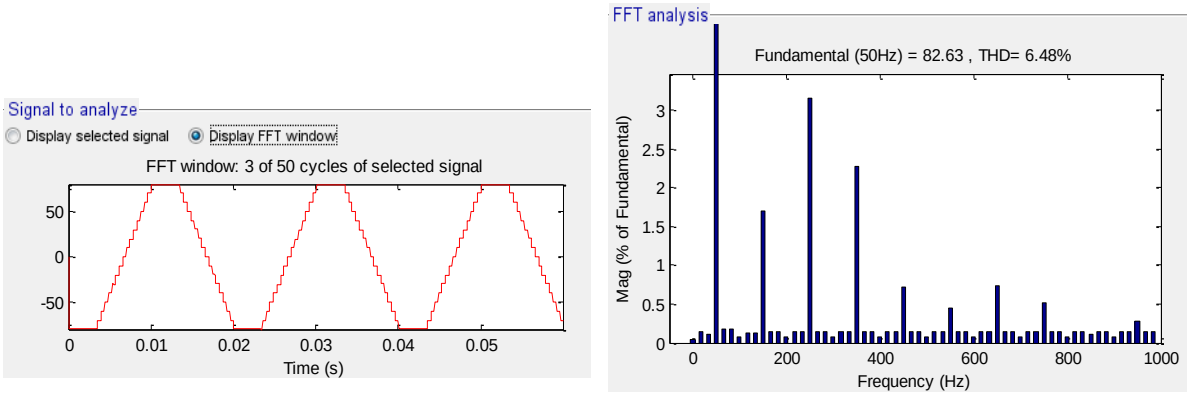

Figure 16. Total harmonic distortion of 17 level cascaded H-Bridge MLI (Phase A)

5.4. 17- level cross H-Bridge inverter fed PMSM

Figures 17-20 represents stator current Phase-A, three phse inverter voltage, speed of motor and THD of 17 Level Cross H-Bridge MLI respectively. The Total Harmonic Distortion of 17- Level Cross H-Bridge is reduced by 3.39% when compared to 17-level cascaded H-Bridge the same can be observed from Figure 16 and Figure 20.

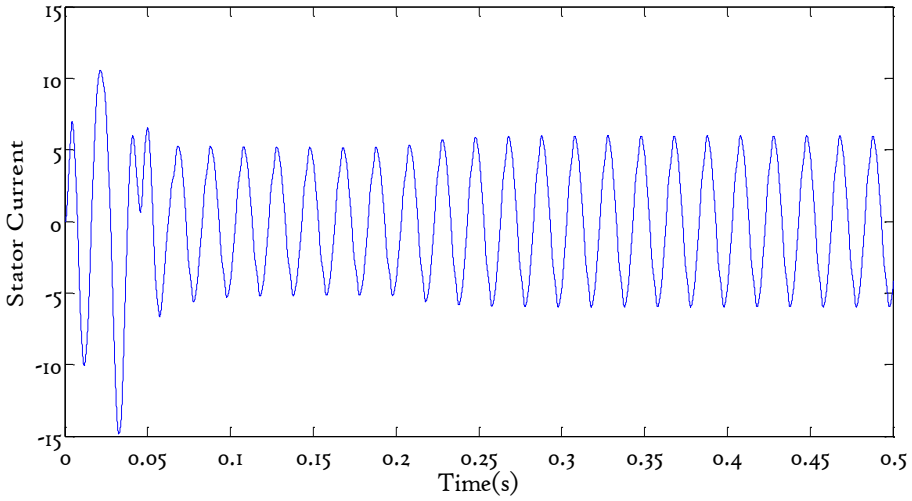

Figure 17. Stator current of Phase-A

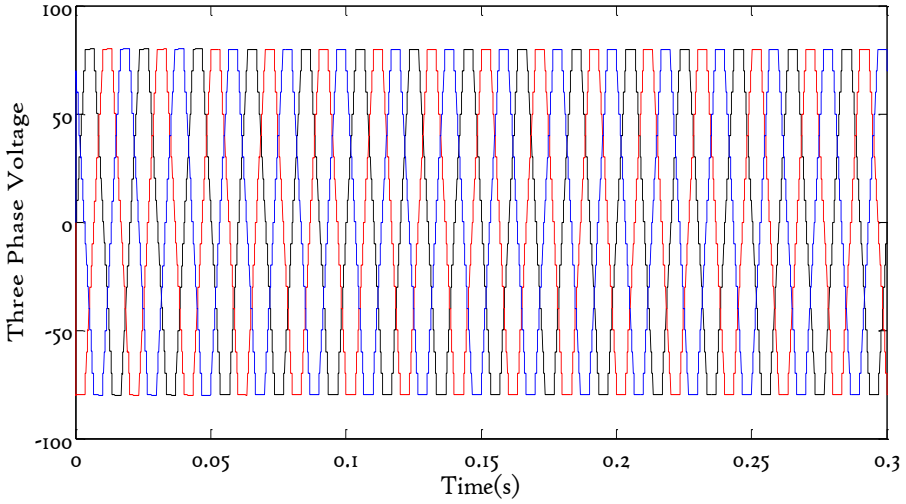

Figure 18. Three phase 17-level cross H-Bridge inverter output voltage

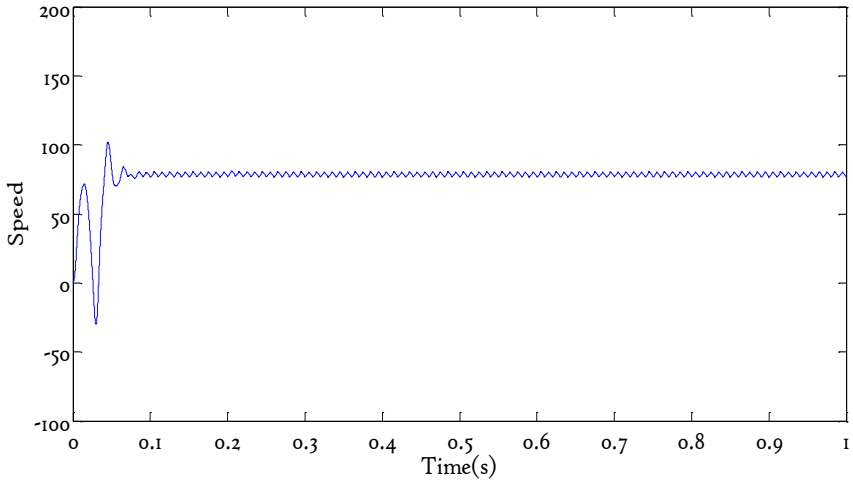

Figure 19. Speed of PMSM

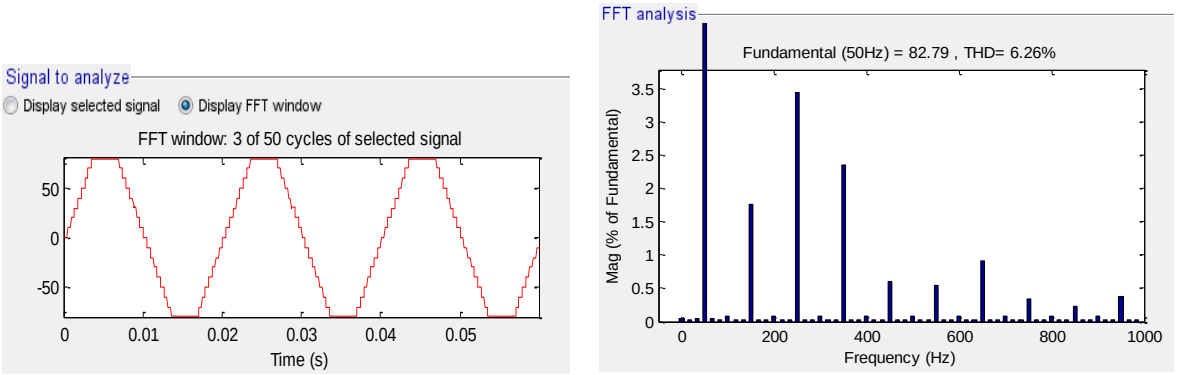

Figure 20. Total harmonic distortion of 17 level cascaded H-Bridge MLI (Phase A)

6. CONCLUSION

Nowadays, multilevel inverter topologies are best choice for many industrial applications owing to their advantages like low EMI, high efficiency and high reliability. This paper presented the comparative analysis of 15 and 17- level cascaded and cross H-Bridge multi-level inverter fed PMSM drive. The intention in this paper is to endow with superior quality of voltage (output) with little THD by evaluating the discussed multilevel converter topologies. From the analysis it is clear that the number of switches required, THD and switch losses of cross H-Bridge configured multilevel inverters is less when compared to cascaded H bridge configuration.

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