

An ultra-low complexity of 2:1 multiplexer block in QCA technology

Ali H. Majeed

Department of Electrical Engineering, University Kufa, Iraq

Article Info

Article history:

Received Jul 23, 2020

Revised Oct 17, 2020

Accepted Nov 29, 2020

Keywords:

Multiplexer
Nanotechnology
QCA MUX
QCA technology
QCA designer

ABSTRACT

The limitations related to CMOS such as power consumption and parasitic capacitance lead scientists to search for new technologies. Quantum-dot cellular automata (QCA) is a CMOS alternative technology that uses charges instead of voltage level for binary representation. In QCA, many metrics are used for circuit differentiation such as delay, complexity and area. In this work, a new simple block of 2:1 QCA-Multiplexer is proposed. The proposed block is more efficient than previous designs by 43%, 53%, 50% and 72% in terms of area, complexity, delay and cost. QCADesigner software is used to design and verify the proposed circuit.

This is an open access article under the [CC BY-SA](https://creativecommons.org/licenses/by-sa/4.0/) license.



Corresponding Author:

Ali H. Majeed
Department of Electrical Engineering
Faculty of Engineering, University of Kufa,
Kufa, Iraq
Email: alih.alasady@uokufa.edu.iq

1. INTRODUCTION

The transistors inside a chip will double every 1.5 to 2 years according to Moore's law [1]. Therefore, the complexity will increase in terms of wiring and power consumption. In the recent era, a new transistor less model for a binary representation technique called Quantum-dot cellular automata (QCA) has been discovered by Lent's teamwork [2]. This technology is proposed to become an alternative for current CMOS technology [3]. The brick unit in QCA is a quantum cell, which has a square shape that contains four holes and two free electrons as shown in Figure 1 [4].

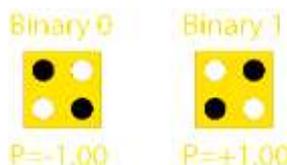


Figure 1. QCA cell configurations

The information can be encoded by the configurations of the electron's charge inside the quantum cell [5]. In QCA, there is no current flow. A couple of electrons inside the cell change their position based on the principle of the electron's interaction. QCA technology is the ideal solution for bypassing transistor-based devices as it has many limitations in terms of power consumption and speed [3]. QCA technology has many interesting features such as low power consumption, high frequency processing and low feature size [6]. The current trend in the digital system is to reduce the complexity of the circuit; in this case, QCA would be handy. In this work, a new structure of 2:1 QCA-MUX is proposed. The proposed gate is superior in terms of area, complexity (cell count) and cost.

2. BACKGROUND

The basic blocks in QCA are the majority gate that consists of 5 cells arranged as in Figure 2 (a) and the inverter (NOT gate), which is presented in two forms shown in Figure 2 (b). The majority gate gives high output whenever most input is high and low elsewhere. The majority gate has a special ability where if one of its input cells is fixed to logic 0, the gate now work as AND gate, and if the fixed cell is logic 1 then it works as OR gate. Therefore, any logic circuit can be performed using the inverter and majority gate [7]. The majority gate is also presented for 5 inputs as in [8-12], and the reliability of this gate is studied in [13].

The QCA gates are connected by a set of cells arranged like a chain. This chain works as a wire connector in QCA where the polarity of the input cell is propagated through this chain depending on the principle of the electron's repulsion as depicted in Figure 2 (c) [14]. For stability and synchronization issues, QCA technology requires a clock signal for controlling the barriers between the dots. The clock signal passes through more than one state to ensure the signal flow from input to output without error [15]. The QCA circuit can be divided into 4 zones where each zone has 4 states as shown in Figure 3.

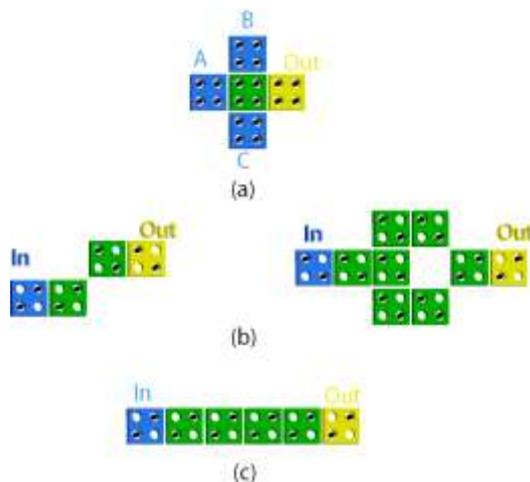


Figure 2. The basic unit in QCA (a) Majority gate (b) NOT gate and (c) QCA wire

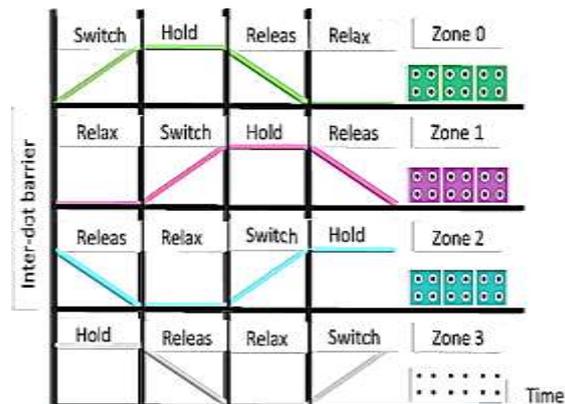


Figure 3. The QCA clock signal in 4 regions

3. RELATED WORK

A Multiplexer is a digital logic gate that receives many signals as input and provides only one as output. The output signal represents one of the input signals that is chosen to be output depending on the selector. The selector signal size of $2n$ input signals is n bit as illustrated by Figure 4 [16]. If n equals 1, the minimum size of the multiplexer is obtained. This gate is important in many circuits such as memory circuits and high-level multiplexers. The functionality equation of 2:1 MUX can be expressed as in (1).

$$2:1 MUX_{out} = \bar{S}I_2 + SI_1 \quad (1)$$

In the QCA world, the researchers are looking for optimality for designing circuits. The optimality is in terms of cell count, area, delay and cost. In the literature, many structures of 2:1 multiplexers were presented as shown in Figure 5. It is clear that the complexity (cell count and area) of all four structures is different and it

is the center point that all researchers are still aiming for shooting on it. Therefore, finding an optimal structure is worthwhile and this work will focus on it.

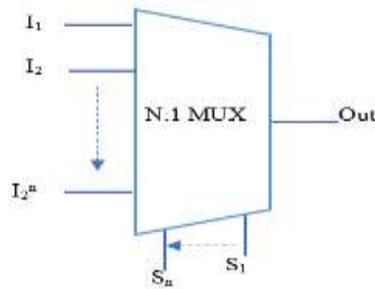


Figure 4. The block diagram of $n \times 1$ Multiplexer

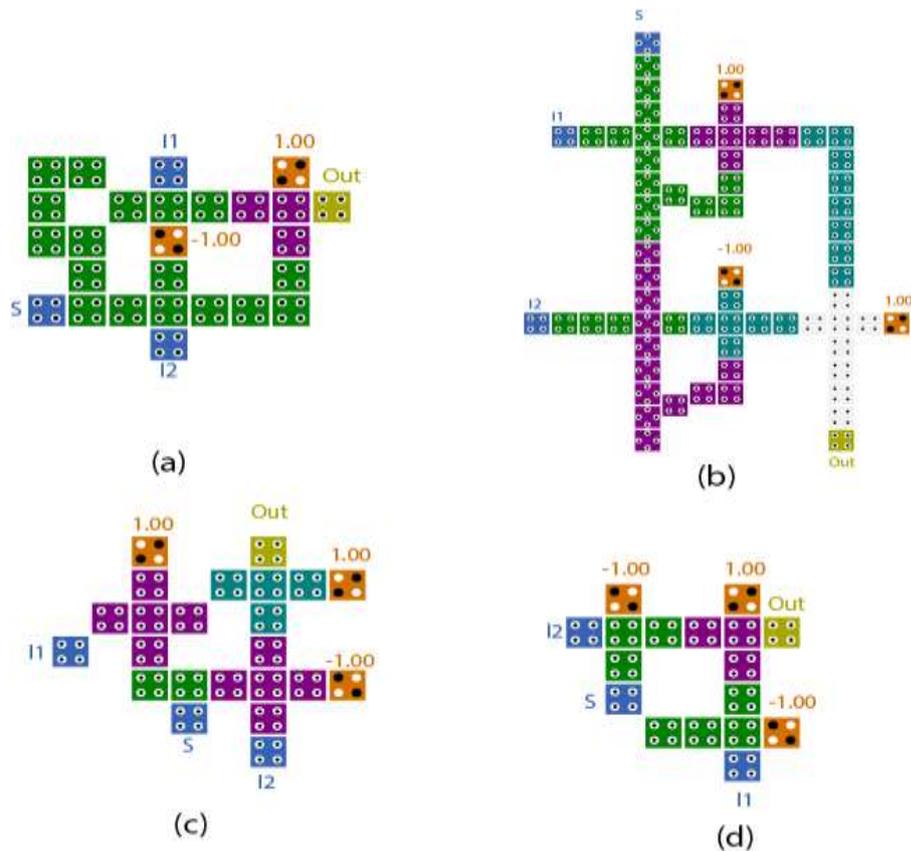


Figure 5. Previous structures of 2:1 QCA-MUX presented in (a) [17], (b) [18], (c) [19] and (d) [5]

4. PROPOSED DESIGN

As mentioned in the last section, the researchers in QCA paid attention to designing the Boolean function with minimum complexity. The basic gates such as AND, OR, NOT and the auxiliary gates such as XOR and MUX are important and widely used in logic circuit design. This paper presents a low complexity of 2:1 MUX. The proposed gate is constructed with only 9 cells and area of 5684 nm². The proposed QCA layout of 2:1 MUX is illustrated in Figure 6.

QCADesigner software [20] is the common tool in QCA technology used to design and verify the QCA circuit. This tool is adopted in this work and the proposed gate is verified in both simulation engines available (bistable and coherence). The output cell changes its state depending on all the electrons in the circuit. The state of a cell is determined by following by (2). The lowest energy state is the most stable.

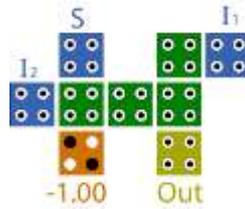


Figure 6. The proposed QCA structure of 2:1 MUX

$$E_{(i,j)} = \frac{k \cdot Q_i Q_j}{r(i,j)} \tag{2}$$

Where:

$E_{(i,j)}$: Kink energy between the two charges i and j .

Q : Electron charge (1.6×10^{-19}).

r : Distance between the charges.

k : Constant value (9×10^9).

Thus, the kink energy can be calculated by following formula given by (3). The entire potential energy can be found by summing the energies for all system charges as expressed in (4) [21].

$$E_{(i,j)} = \frac{23.04 \times 10^{-29}}{r(i,j)} \text{ (J)} \tag{3}$$

$$U_{Ti} = \sum_{j=1}^N E_{i,j} \tag{4}$$

5. SIMULATION RESULT

As mentioned before, the most common tool in QCA technology is QCADesigner. In this work, the QCADesigner V 2.0.3 tool is adopted as its most recent version to design and simulate the proposed circuit. Figure 7 shows the output result of the proposed 2:1 QCA-MUX block. It is clear from this figure that when $S=0$, the output is the same as the signal presented at $I1$ and when $S=1$, the output is the same as the signal presented at $I2$.

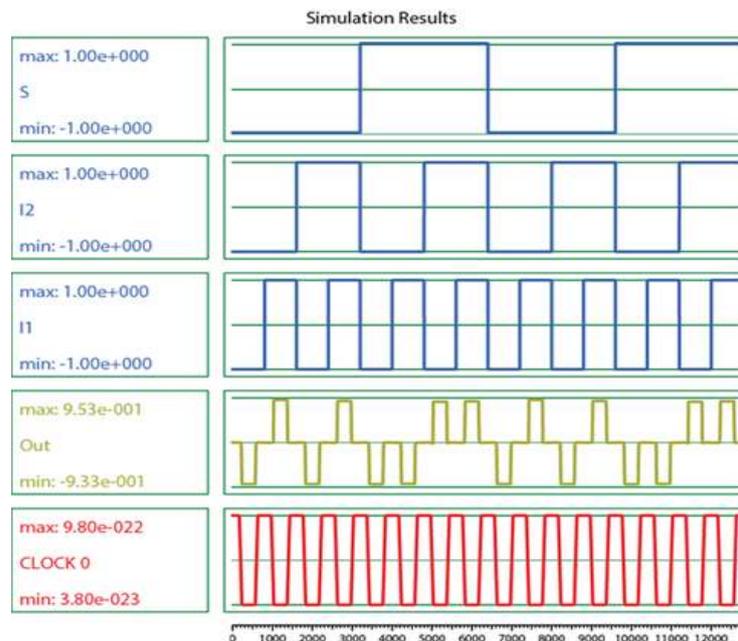


Figure 7. The simulation result for the proposed QCA-MUX

6. RESULT COMPARISON

The output simulation demonstrates that the proposed block is free of error and has high polarization value as shown in the output signal. Moreover, the proposed circuit has a noticeable area of 5684 nm² and the complexity of only 9 cells. The power of the proposed block over previous counterparts in all metrics is indicated in Table 1. The QCA circuit cost is also calculated by multiplying area by latency (delay) [22]. The proposed design has high thermal stability is as shown in Figure 8.

Table 1. Result comparison table

Design	Area	Complexity	Clock phases (delay)	Cost (Area*Delay)
[23]	0.07	56	4	0.28
[24]	0.06	36	4	0.24
[20]	0.03	27	3	0.09
[25]	0.02	19	2	0.04
[26]	0.01	15	2	0.02
[27]	0.01	19	2	0.02
Proposed block	0.0057	9	1	0.0057

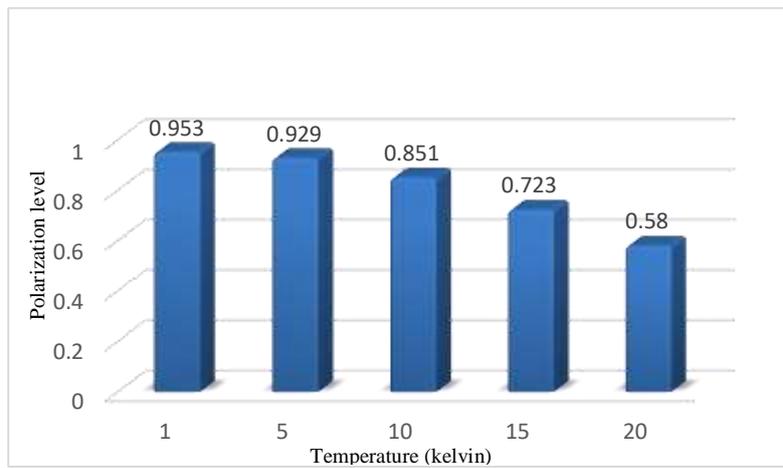


Figure 8. The level of polarization for the proposed gate output signal

7. CONCLUSION

In this paper, a new low cost and highly efficient 2:1 QCA-MUX is proposed. The proposed gate is low complexity with only 9 cells and 5684 nm² of area. The output signal indicates that the proposed gate is error-free with a high polarization level. The thermal stability of the proposed gate indicates its robustness. The proposed block shows an improvement in the percentage by 43%, 53%, 50% and 72% in terms of area, complexity, delay and cost. The QCA Designer tool has been used to prove circuit work and verify the result.

REFERENCES

- [1] M. Zahmatkesh, S. Tabrizchi, S. Mohammadyan, K. Navi, and N. Bagherzadeh, "Robust coplanar full adder based on novel inverter in quantum cellular automata," *International Journal of Theoretical Physics*, vol. 58, no. 2, pp. 639-655, 2019.
- [2] C. S. Lent et al, "Quantum cellular automata," *Nanotechnology*, vol. 4, no. 1, pp. 49-57, 1993.
- [3] M. Ali Hussien, Z. Mohd Shamian, and A. Esam, "Quantum-dot cellular automata: Review paper," *International Journal of Integrated Engineering*, vol. 11, no. 8, pp. 143-158, 2019.
- [4] M. Ali Hussien, Z. Mohd Shamian, A. Esam, and N. Danial Md, "A Content-Addressable Memory Structure using Novel Majority Gate with 5-input in Quantum-dot Cellular Automata," *International Journal of Integrated Engineering*, vol. 12, no. 4, pp. 28-38, 2020.
- [5] J. Das and D. De, "Optimized multiplexer design and simulation using quantum dot-cellular automata," *Indian Journal of Pure and Applied Physics*, vol. 54, no. 12, pp. 802-811, 2016.
- [6] A. H. Majeed, E. Alkaldy, M. S. bin Zainal, and D. Bin Md Nor, "Synchronous counter design using novel level sensitive T-FF in QCA technology," *Journal of Low Power Electronics and Applications*, vol. 9, no. 3, p. 27, 2019.

- [7] A. H. Majeed, M. S. B. Zainal, E. Alkaldy, and D. M. Nor, "Full adder circuit design with novel lower complexity XOR gate in QCA technology," *Transactions on Electrical and Electronic Materials*, pp. 1-10, 2020.
- [8] Ali H. Majeed, E. Alkaldy, MSB Zainal, and Danial BMD Nor, "A new 5-input Majority Gate Without Adjacent Inputs Crosstalk Effect in QCA Technology," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 14, no. 3, pp. 1159-1164, 2019.
- [9] S. S. K. Navi, R. Farazkish, and M. R. Azghadi, "Five input majority gate, a new device for quantum-dot cellular automata," *Journal of Computational and Theoretical Nanoscience*, vol. 7, no. 8, pp. 1546-1553, 2010.
- [10] R. Akeela and M. Wagh, "A five-input majority gate in Quantum-dot Cellular Automata," *Technical Proceedings of the 2011 NSTI Nanotechnology Conference and Expo, NSTI-Nanotech 2011*, vol. 2, 2011, pp. 978-981.
- [11] T. N. Sasamal, A. K. Singh, and A. Mohan, "An efficient design of Quantum-dot Cellular Automata based 5-input majority gate with power analysis," *Microprocessors and Microsystems*, vol. 59, pp. 103-117, 2018.
- [12] A. Majeed, E. Alkaldy, and S. Albermany, "An energy-efficient RAM cell based on novel majority gate in QCA technology," *SN Applied Sciences*, vol. 1, no. 11, p. 1354, 2019.
- [13] E. Alkaldy and K. Navi, "Reliability study of single stage Multi-input majority function for QCA," *International Journal of Computer Applications*, vol. 83, no2, 2013.
- [14] E. Alkaldy, A. H. Majeed, M. S. bin Zainal, and D. Bin Md Nor, "Optimum multiplexer design in quantum-dot cellular automata," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 17, no. 1, pp. 148-155, 2020.
- [15] A. H. Majeed, B. Salih, M. S. bin Zainal, and D. Bin Md Nor, "Power efficient optimal structure CAM-Cell in QCA technology," *Indian Journal of Science and Technology*, vol. 12, no. 37, pp. 1-6, 2019.
- [16] H. Majeed Ali, E. Alkaldy, S. Zainal Mohd, K. Navi, and D. Nor, "Optimal design of RAM cell using novel 2:1 multiplexer in QCA technology," *Circuit World*, vol. 46, pp. 147-158, 2019.
- [17] R. Sabbaghi-Nadooshan and M. Kianpour, "A novel QCA implementation of MUX-based universal shift register," *Journal of Computational Electronics*, vol. 13, no. 1, pp. 198-210, 2014/03/01 2014.
- [18] V. Mardiris, C. Mizas, L. Fragidis, and V. Chatzis, "Design and simulation of a QCA 2 to 1 multiplexer," *Presented at the Proceedings of the 12th WSEAS international conference on Computers*, Greece, 2008, pp. 572-576.
- [19] D. Mukhopadhyay and P. Dutta, "Quantum Cellular Automata based Novel Unit 2:1 Multiplexer," *International Journal of Computer Applications*, vol. 43, no. 2, pp. 22-25, 2012.
- [20] K. Walus, T. J. Dysart, G. A. Jullien, and R. A. Budiman, "QCADesigner: a rapid design and Simulation tool for quantum-dot cellular automata," *IEEE Transactions on Nanotechnology*, vol. 3, no. 1, pp. 26-31, 2004.
- [21] S.-S. Ahmadpour, M. Mosleh, and S. R. Heikalabad, "A revolution in nanostructure designs by proposing a novel QCA full-adder based on optimized 3-input XOR," *Physica B: Condensed Matter*, vol. 550, pp. 383-392, 2018.
- [22] J. Maharaj and S. Muthurathinam, "Effective RCA design using quantum dot cellular automata," *Microprocessors and Microsystems*, vol. 73, p. 102964, 2020.
- [23] V. A. Mardiris and I. Karafyllidis, "Design and simulation of modular $2n$ to 1 quantum-dot cellular automata (QCA) multiplexers," *I. J. Circuit Theory and Applications*, vol. 38, no. 8, pp. 771-785, 2010.
- [24] S. Hashemi, M. R. Azghadi, and A. Zakerolhosseini, "A novel QCA multiplexer design," in *2008 International Symposium on Telecommunications*, 2008, pp. 692-696.
- [25] B. Sen, M. Dutta, M. Goswami, and B. K. Sikdar, "Modular Design of testable reversible ALU by QCA multiplexer with increase in programmability," *Microelectronics Journal*, vol. 45, no. 11, pp. 1522-1532, 2014.
- [26] H. Rashidi, A. Rezai, and S. Soltany, "High-performance multiplexer architecture for quantum-dot cellular automata," *Journal of Computational Electronics*, vol. 15, no. 3, pp. 968-981, 2016.
- [27] J.-C. Jeon, "Designing nanotechnology QCA-multiplexer using majority function-based NAND for quantum computing," *The Journal of Supercomputing*, 2020.

BIOGRAPHIES OF AUTHORS



Ali H. Majeed received B.Sc in electrical engineering in 2006 from University of Kufa, Iraq. He takes M.Sc. in electronic engineering from University of technology, Iraq in 2012. Currently he a Ph.D. candidate at UTHM University, Malaysia. His research interests focused on nanoelectronics, circuits and systems.