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A novel pipelined carry adder design based on half adder

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ABSTRACT

A new design of binary parallel adder circuit is presented in this paper. The pipeline technique is applied to implement a group of a half adder (HA) blocks to architect the proposed adder. The pipelined carry adder (PCA) method is suitable for carrying out the desired adder by using the HA circuits of XOR and AND gates. The applied technique reduces the critical path delay by 27% compared with the ripple carry adder (RCA) and relatively lowers logic gates by 55% compared with the carry look-ahead adder (CLA). The coded design of the proposed circuit is implemented and simulated on the Cyclone IV FPGA kit platform. Results show that the circuit needs a 7.69 η Sec delay time to provide the output values. The suggested PCA circuit is more attractive than the conventional ripple carry adder for future electronic applications.

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1. INTRODUCTION

Various electronic devices have been rapidly developed in recent years with the emergence of new methods and techniques to improve the circuits in these devices. An adder is a combinational circuit which is important in improving arithmetic circuits. The structure of the full adder circuit explains the summation of three bits. A group of full adder circuit is serially connected to obtain the computation of the N-bit parallel numbers.

The critical path delay is determined by the longest pathway through the adder circuit. Therefore, the critical path delay of N-bit adders is determined by three gate delays of the first bit adder and to ripples in two gate delays of each of the next adders [1], explaining why it is called 'ripple carry adder (RCA)' [2], [3]. The critical path delay is calculated using (1).

$$c_{out} = 2N + 1 \quad (1)$$

where N is the number of the bit adder.

The delay time of parallel adders hinders the use of RCA. Thus, various techniques and methods have been used to minimize the path delay. A commonly used method in addition to the RCA, is the carry look-ahead adder (CLA). This method is based on calculating the result quickly for each stage [4], [5], considering that the carry-in of the previous stage will have 0 or 1 and the critical path delay is achieved only after two gate delays (Figure 1). The fast-calculating feature of the CLA is applied in [6], [7] to use 32-bit and 64-bit CLAs, respectively. The designed CLA circuit in [6] can switch between the approximate and exact modes in error-resilient and execute applications. The disadvantage of the CLA method is the exponentially increasing AND-OR gates with the growing bit number. The critical path delay of the 8-bit

CLA in (2) declares how the path delay requires multi-bit OR-AND gates to achieve the correct carry-out value.

$$C_{out} = g_7 + p_7 g_6 + p_7p_6g_5 + p_7p_6p_5g_4 + p_7p_6p_5p_4 g_3 + p_7p_6p_5p_4 p_3 g_2 + p_7p_6p_5p_4 p_3 p_2g_1 + p_7p_6p_5p_4 p_3 p_2p_1g_0 + p_7p_6p_5p_4 p_3 p_2p_1p_0C_0 \quad (2)$$

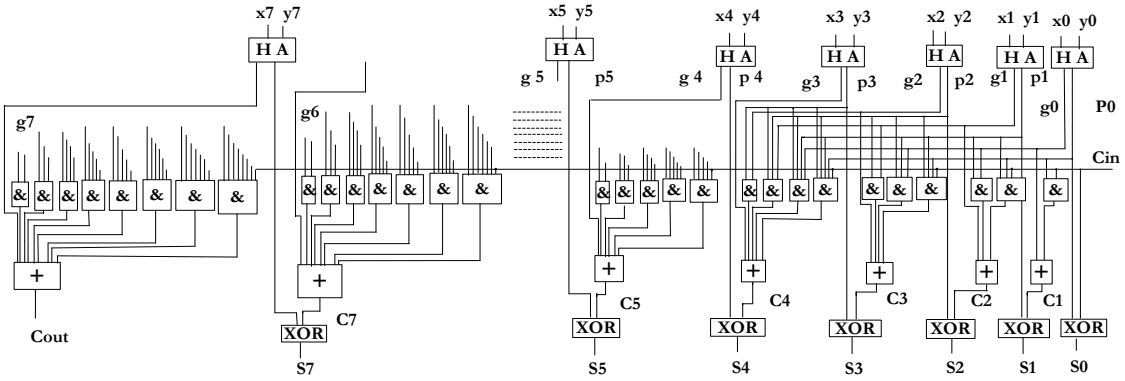


Figure 1. Block circuit diagram of the 8-bit CLA

Another method is used to architect the parallel adder by inserting two rows of RCAs, namely, carry select adder, with carry-in input for 0 and 1 [8], [9]. A 2×1 multiplexer is used for each bit to provide the sum output, as shown in Figure 2. The critical path output of both RCAs is joined to the multiplexer to select the carry out of the couple RCAs.

Pipelined technique is used to improve the processing of system performance by parallel feeding data inputs to the systems [10]-[13], and efficiently reduced the requested time delay. Deep learning, is a function of artificial intelligence (AI), and it's a part of the machine learning methods that use the stochastic computing to imitate the human brain for processing data. In recent years, this technique is rapidly developed and used for the optimized implementations in various fields such as image classifications [14], computer vision and speech recognition. Deep learning technology also used to optimize the electronic logic circuit using Markov decision process (MDP) [15], and for the analog circuit as in [16].

Deep and machine learning algorithms are a good solution to optimize the power, delay and area efficient of parallel prefix adder design with wide (32-bit, 64-bit) ranges [17], [18] such as Brent–Kung, Kogge-Stone and Sklansky adders. As the proposed sample design is a small bit circuit (8-bit adder), the artificial intelligence methods become not useful to use in this design.

This paper presents a new design of binary parallel adder circuit. The proposed adder is prepared by implementing the pipeline stages of half adder (HA) circuits to architect two samples of 8-bit pipelined parallel adder. Then, the HA circuit of the suggested design is configured based on 3-, and 4-transistors complementary metal-oxide-semiconductor (CMOS) logic gates in order to reduce the increasing of the number of CMOS transistors proportional with growing N-bits adder. The research paper is organized as follows: section 1 provides the introduction. Section 2 describes the design circuit. Section 3 contains the results and discussion. Section 4 ends with a conclusion.

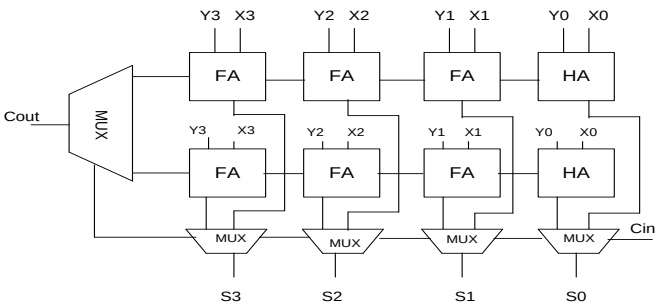


Figure 2. Block circuit diagram of carry select adder

2. DESIGN CIRCUIT OF PIPELINED CARRY ADDER

A novel method of binary parallel adder circuit is designed based on the HA circuits to provide the critical path delay with minimum gate delay. Pipelining connects the HA to the XOR inputs of the other HA blocks in the next level. The proposed pipelined carry adder (PCA) method can enable the circuit to provide the sum outputs of the parallel adder through the stages, whereas the critical path carries out as the group of the all stages in the OR gate. Figure 3 shows that the presented PCA needs only HA circuits to architecture the desired parallel adder. The path delay time is calculated by the number of stages with one OR gate.

It can be formulated by (3).

$$c_{out} = N + 1 \tag{3}$$

Where N is the binary digit bits. In (3) shows that the path delay of carry output required N-bit delays, farther one more gate delay time. This describes, why the delay time of the proposed method is about 27% time less than that in the RCA.

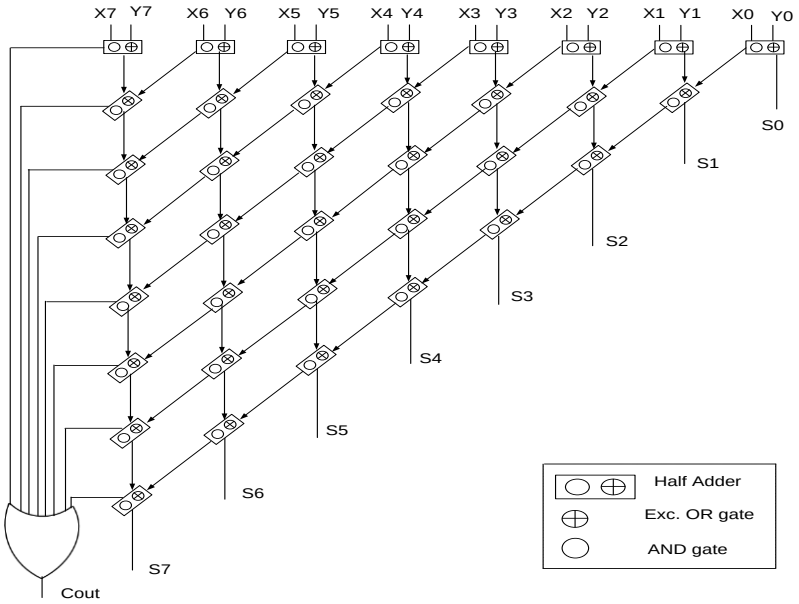


Figure 3. Circuit diagram of the proposed 8-bit pipelined carry adder

2.1. Modified pipelined carry adder (PCA)

The proposed PCA design circuit relatively reduces the carry out path-delay compared with the RCA. This advantage is accompanied by increasing the number of HA circuits proportional to increasing the number of bit adders. Calculation of the HA circuits used is based on (4).

$$No.of\ HA\ blocks = \frac{N}{2}(N+1) \tag{4}$$

The proposed design is modified by partitioning the given bit numbers into a small circuit of two and three bits (Figure 4) to avoid the cumulative increase in the HA circuit with the wider PCA bit adder while preserving the desired path delay. The proposed modification technique can slightly increase the path delay time, but can greatly reduce the number of HA circuits by up to 45%. As an example, the 8-bit PCA (Figure 3) requests 36 blocks of HA circuits, whereas the modified circuit of the same desired bit adder requires only 20 HA circuits with an additional AND gate to each mini circuit (Figure 4).

As an example of the proposed 8-bit PCA circuit in Figure 4, the summation of two parallel bits of 10010101 and 11010101 is clearly described in Figure 4. The appearing (0 and 1) digit numbers in the dashed circles describes the exact operating process. The result will be 101101010 (149+213=362 in decimal). The effect of the suggested new modification technique to the PCA design will clearly demonstrate how this technique can relatively reduce the number of HA circuits, especially with wider (16-bit, 32-bit) parallel adders compared to the RCA or CLA.

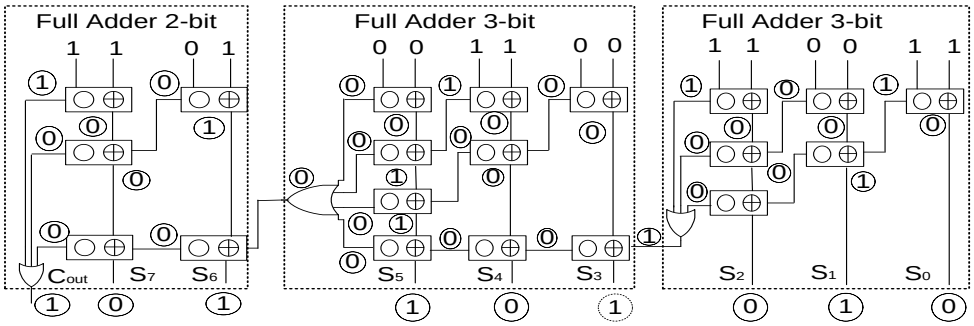


Figure 4. Description of the sum of two parallel bits in PCA

2.2. Configuration of HA circuit based on CMOS gates

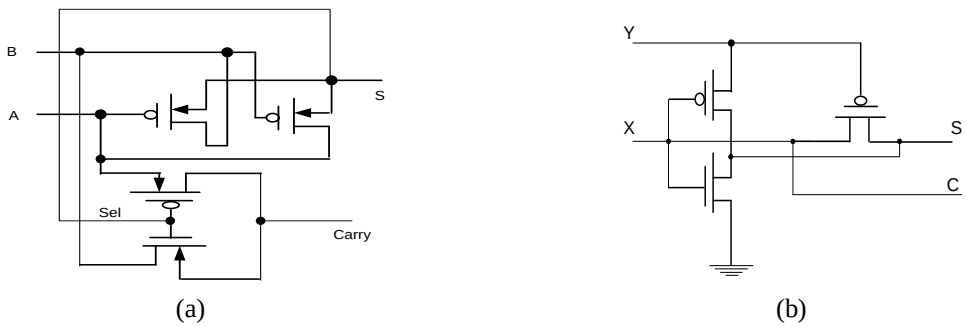
In recent years, the complementary metal-oxide-semiconductor (CMOS) technology has become the first choice for the fabrication of electronic circuits and devices. CMOS is a metal-oxide-semiconductor field-effect transistor (MOSFET) manufacturing process which uses the n- and p-types in a logic circuit which is complementary connected. The proposed PCA is designed based on HA circuits; therefore, the circuit performance must be improved by minimizing the transistor counts of the XOR CMOS logic.

The basic half adder circuit block consists of the XOR and AND logic gates. The XOR gate was early manufactured in 8-transistors based on CMOS logic [19], 6- transistors [20], [21] and 4-transistors [22], [23]. The power consumption of the circuit decreases when the number of transistors used is reduced. Hence, designers aim to use a small number of transistors to build the XOR gate. Preparing a CMOS 3-transistor XOR gate is a good choice as in [24]-[26]. Given that the proposed 8-bit PCA is designed based on HA, the desired circuit is generated by a mini-number transistor XOR gate. Only two transistors are used in the optimized 2-bit XOR CMOS gate configuration [27]. The circuit diagram of the 2-T XOR gate is shown in Figure 5(a). Using the multiplexer case, the 2-bit AND gate with two transistors [25] can be found as in the Figure 5(b).

The above explanation details enable the construction of the 4-transistor half-adder circuit, as shown in Figure 6(a). The HA circuit is also constructed as a managed circuit of the XOR and AND gates based on CMOS logic. The provided circuit decreases the power consumption of HA. Only three transistors are needed to obtain the desired HA circuit [28], as shown in Figure 6(b).

(a) (b)

Figure 5. 2- transistors circuit diagram of (a) XOR gate and (b) MUX AND gate



(a) (b)

Figure 6. Half adder circuit diagram-based No. of transistors: (a) 4-transistor and (b) 3- transistors

For the proposed 8-bit PCA to use the suggested 3-transistor HA, the circuit must be partitioned into three parts based on the diagram circuit in Figure 4. The proposed model full circuit is shown in Figure 7. The figure defines that the CMOS logic includes 86 n- and p-type MOSFET transistors. This is the result of the 20 of 3-transistor HAs, two 3-bit and one 4-bit OR gates.

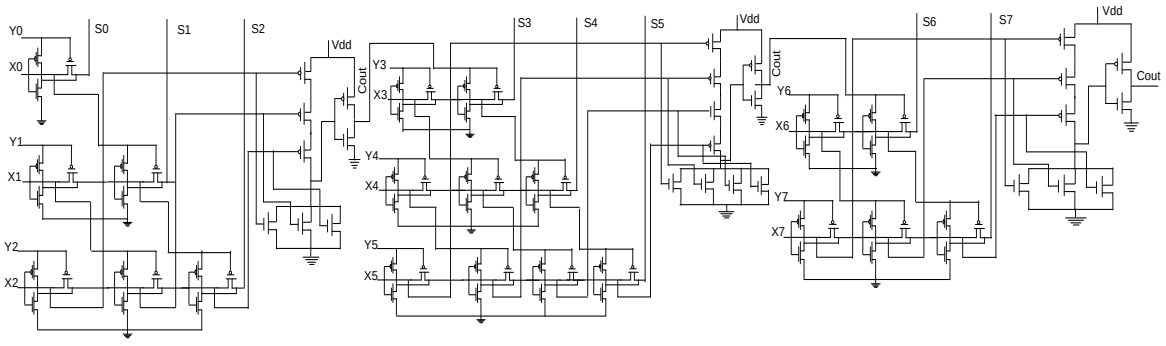


Figure 7. 8-bit PCA circuit diagram-based CMOS logic

3. RESULTS AND DISCUSSION

The calculation of two binary values provides a result (00, 01, 10 or 11). The HA is a suitable circuit to obtain the given result. For the summation of multi binary digit bits, then the circuit diagram of the parallel adders is complicated to overcome the carried out value of each two binary bits, which is the critical pathway. The designers applied multiple methods and various techniques to reduce the critical path delay and therefore enhance the circuit's performance while preserving correct results. As shown in Figure 7, the block circuit diagram of the proposed PCA design was structured with the three OR gates based on the groups of 20 HA (3-transistor) circuit.

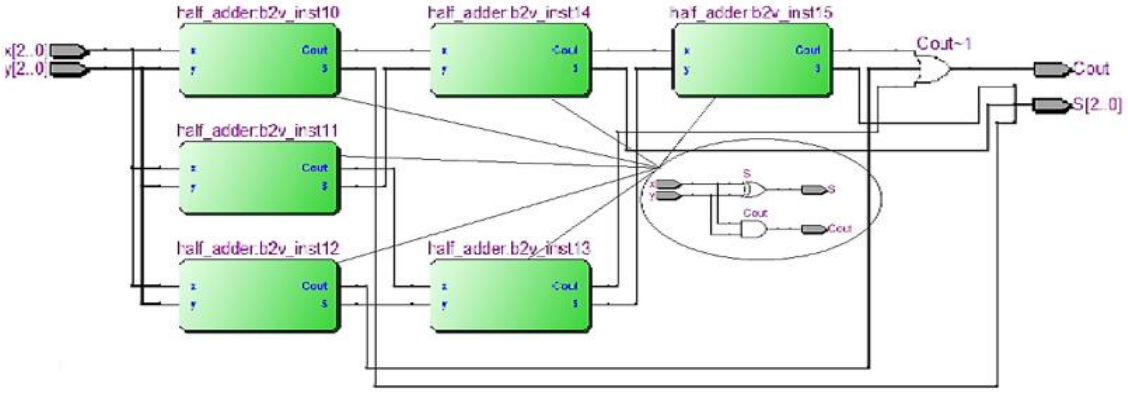
In addition to the number of count transistors, a comparison of the proposed PCA and the other parallel adders in terms of gate delay and logic gates is given in Table 1. Table 1 shows the advantage of the proposed design compared to the RCA in terms of gate-delay units. In specific, a gate delay reduction of 27% can be achieved by the PCA and a logic gate reduction of 55% can be achieved by the CLA. The CLA has a low gate delay time, but its number of logic gates exponentially increases with increasing wide bit numbers. The number of transistors of the proposed design circuit compared with the different techniques described in Table 1 shows clearly lower transistor counts. The 3-transistor circuit could be used to architect the proposed design, which could reduce the transistors amount and power usage of the circuit.

Table 1. Comparison of the proposed PCA with other reported works

Parameter 8-bit	Gate delay	Logic gates	Technique	No of Transistors
RCA	15	37	CMOS	128 [29]
				224 [30]
CLA	3	68	TG logic	176 [31]
			CMOS	408 [32]
			m-GDI	110 [32]
CSA	15	52	Static CMOS	354 [33]
This work	11	43	3-Trans. CMOS	86
			4-Trans. CMOS	126

The modified PCA design circuit has been coded, synthesized and elaborated in Quartus II software. The register transfer level viewer of the proposed design circuit and the portioned 3-bit adder is shown in Figures 8(a) and (b). The coded design circuit of the modified 8-bit PCA was implemented on the Cyclone IV-GX FPGA kit platform and simulated using ModelSim software to verify the functionality of the proposed design. The gate level simulation result is shown in Figure 9.

(a)



(b)

Figure 8. The created register transfer level viewer for: (a) 8-bit PCA and (b) portioned 3-bit adder

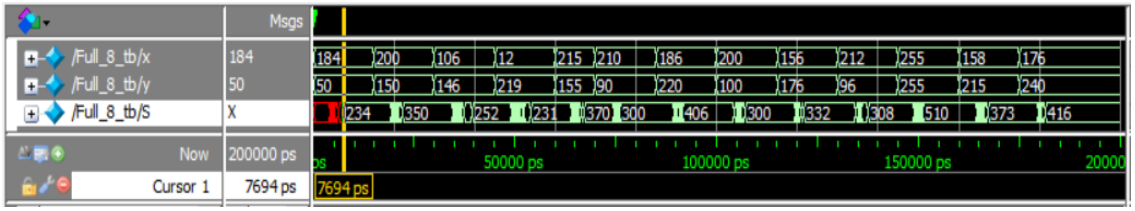


Figure 9. Gate level simulation of the 8-bit PCA adder

4. CONCLUSION

A novel method of the PCA circuit is designed and implemented in this paper. The proposed design circuit is an architect based on the HA circuits. The 8-bit PCA is proposed in two design circuits. The pipelined PCA circuit is architected based on the HA blocks to provide the correct sum with a short path delay. The second modified PCA is established by partitioning the 8-bit into small circuits of two-bit and three-bit adders to reduce the HA block circuits. The modified PCA circuit was coded Verilog HDL code, elaborated in Quartus II software and then implemented and simulated on the Cyclone IV-GX FPGA platform software, to verify the functionality results of the circuit. The proposed PCA is easy to design because of the use of the HA circuit with a lower number of transistors compared with the other works. The design relatively reduces the critical path delay by 27% of the PCA and lower logic gate by 55% of the CLA.

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