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Study of Small Signal of 4H-SiC Static Induction Transistor

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Abstract

Silicon carbide (SiC) SITs were fabricated using home-grown epi structures. The gate is a recessed gate - bottom contact (RG - B). We designed that the mesa space 2.5 μm and the gate channel is 1.5 μm. One cell has 400 source fingers and each source finger width is 50 μm. 0.5 mm gate periphery SiC SIT yielded a maximum drain current density of 160 mA/mm at a drain voltage of 80 V and a gate voltage of 2.5 V. The device blocking voltage with a gate bias of -16 V was 400 V. Packaged 0.5-mm devices were evaluated using amplifier circuits designed for class AB operations. Small signal of SIT was studied. the maximum stable gain (MSG) were 11.2 dB at 500MHz and 7.85 dB at L band 1 GHz with V_{ds} = 80V and V_g = 2V.

***Keywords**: SiC, SIT, MSG, RF*

1. Introduction

4H-SiC is one of the potential semiconductors for high power electronic device applications because 4H-SiC offers three key operating characteristics for high pulsed power: wide band gap (3.2 eV), to allow the device operate at higher junction temperatures, and therefore longer life than silicon for reduced field costs. High breakdown field (3 MV/cm) allows for high voltage operation to increase the power output from the same current. High thermal conductivity (4.9 W/cm·K) provides higher power density for higher peak power in the same-sized package as with silicon [1, 2]. From figure 1, we can know that SiC is 10 times higher than that of Si and GaAs at breakdown voltage. Then, high output power due to high breakdown voltage [3].

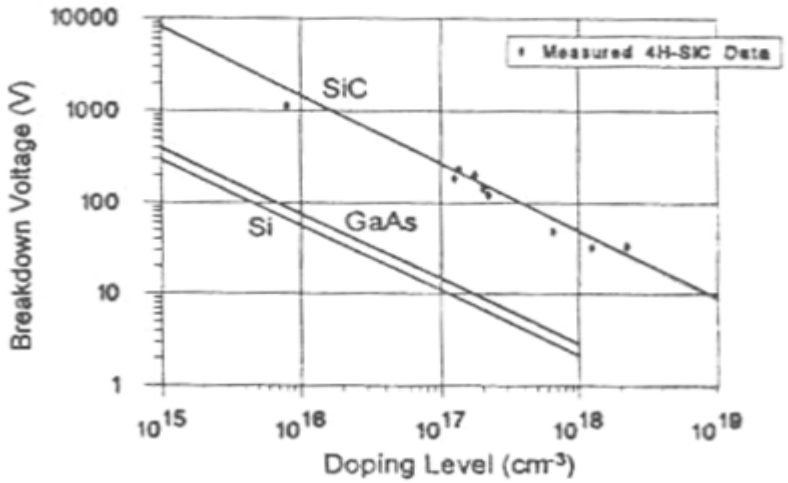

Figure 1. Measured breakdown voltage of p-n junction diodes as a function of doping, and the theoretical maximums for Si and GaAs (Gallium arsenide)

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The historic silicon amplifiers are limited by heat dissipation due to the potential for thermal runaway during long pulses (> 300 μs) and high peak powers. Silicon RF transistors—whether BJT, VDMOS or LDMOS—are not able to offer the combination of increased peak power performance and extended pulse (> 300 μs) characteristics for the next generation of radar systems [4]. As Figure 2 was shown, SiC SIT has RF power from 100 W up to 1000 W and has application frequency spans from MF up to S-band.

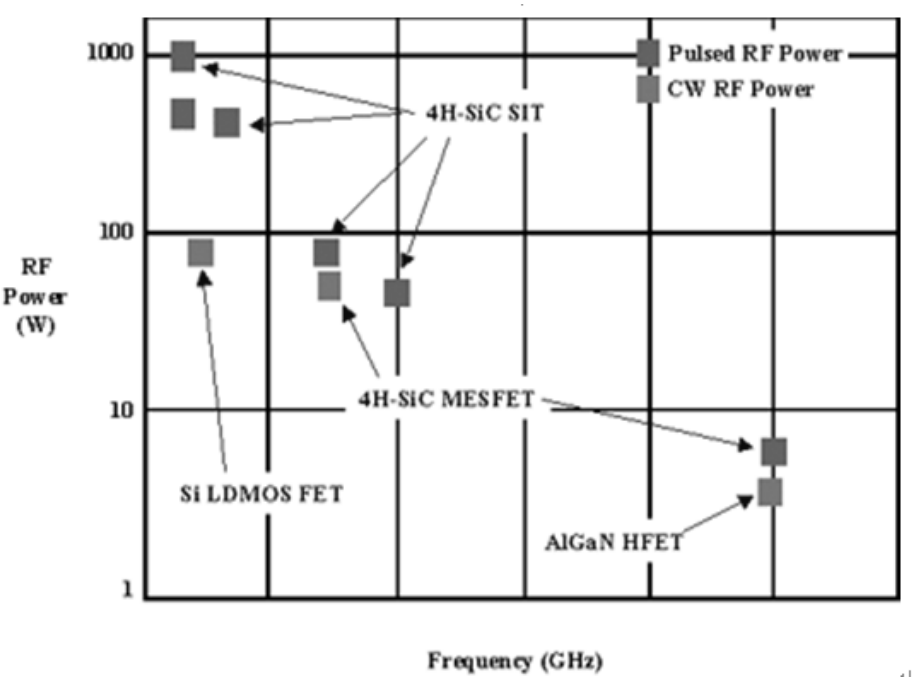


Figure 2. A comparison of SIT with other relevant SiC microwave devices

The SIT was formed with Schottky gate contact that reduces the work temperature and radiation limits. The ion-implanted p-n junction employment instead the Schottky gate contact enhances these limits essentially. High power 4H-SiC SIT has vertical short channel FET structure. Current flows vertically by modulating the internal potential of the channel using surrounding gate structure. Characteristics were similar to a vacuum-tube diode. The cross sections schematic of the ion implanted p-n junction gate SIT was shown in Figure 3. SiC SIT devices with 550 W output power have been fabricated on SiC epitaxial wafer for UHF band applications. At 500 MHz and 90 V drain to source voltage, a 28 cm gate periphery SiC SIT exhibited an output power of 550 W with a gain of 11.3 dB under pulsed RF operation [5].

The work described in this paper is the study of I-V characteristics and the small signal parameter of a 0.5 mm SiC SIT with one gate tub having 10 source fingers.

2. Experimental Details

SiC is grown homo-epitaxially on Si-axis orientated n-type 4H-SiC substrates placed on the susceptor. On the base of n+ substrate we created n+ buffer layer with concentration 1×10^{18} cm^{-3} and width 0.5 μm, which is covered by n- epilayer with concentration 3×10^{16} cm^{-3} and width 3.5 μm, which is covered by n+ top layer with concentration 2×10^{19} cm^{-3} and width 0.2 μm. Low resistance and capacitance considerations set the high-frequency SIT drift layer thickness in the 2.5 to 3.5 μm range. The epilayer cross section schematic is shown by Figure 4.

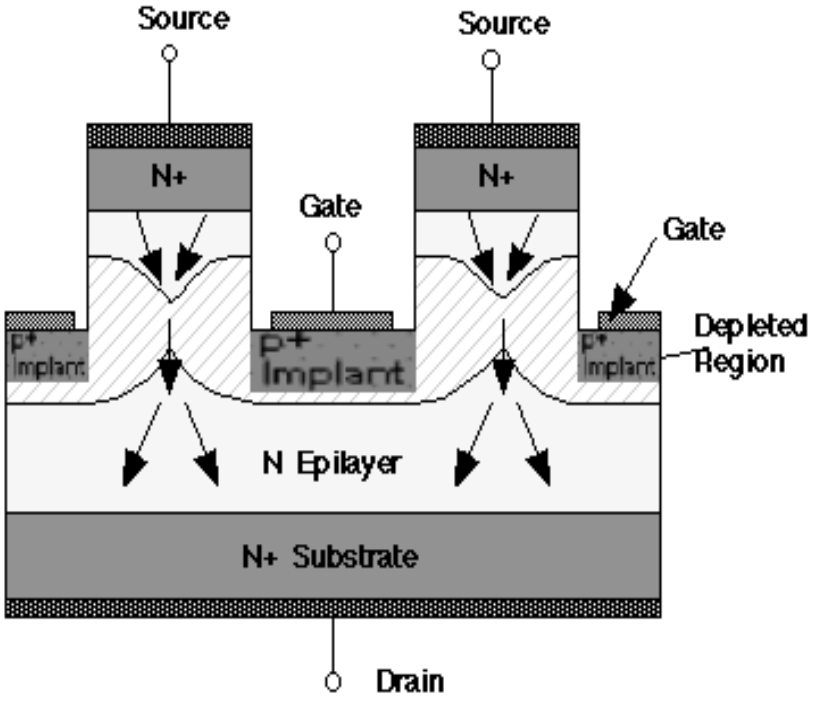


Figure 3. Ion implanted p-n junction SIT

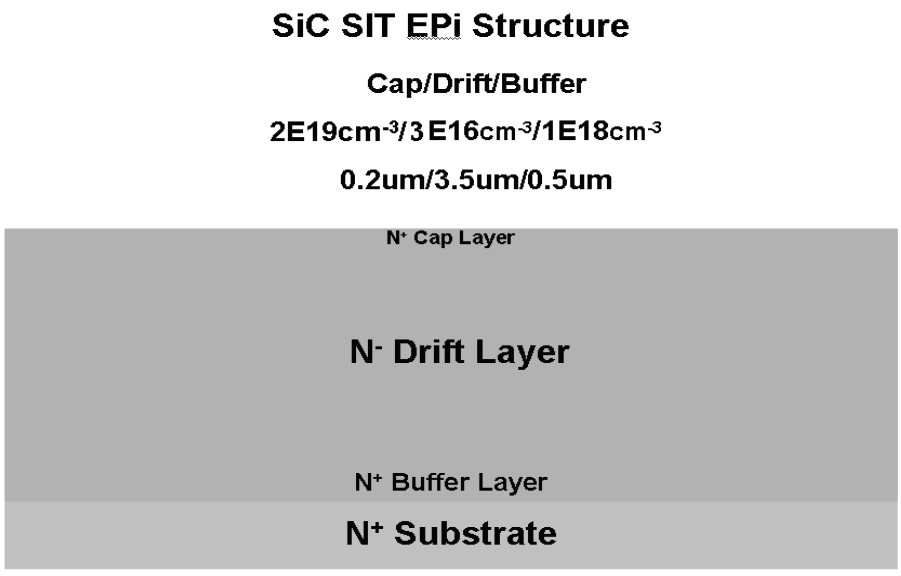


Figure 4. SiC SIT epilayer structure

The SiC SIT structure is rather complicated from a processing point of view. The device requires stepper lithography to produce rows of closely spaced mesas which are defined by inductively coupled plasma (ICP). A nickel mask is defined on the SiC to act as an etch stop during the ICP etching of a pillar of SiC. The recessed gate SIT has been fabricated in SiC. Because of difficulty in deep ion implantation (p-type dopant Al implanted at energy of 380 keV has a peak range of only 0.42 μm into SiC) and the lack of diffusion at temperatures below 1850

℃, the recessed gate structure has been favored in SiC. The gate may be a recessed gate - bottom contact (RG - B) or a recessed gate - sidewall and bottom contact (RG - SB). Because the RG - SB contact provides a longer gate length, we choose the RG - B contact. A PECVD oxide coating is applied to the mesas and etched away from the 0.5 μm gate contact region in order to leave behind an oxide sidewall passivation between the source n+ contact layer and the gate electrode. We designed that the mesa space 2.5 μm and the gate channel is 1.5 μm [6].

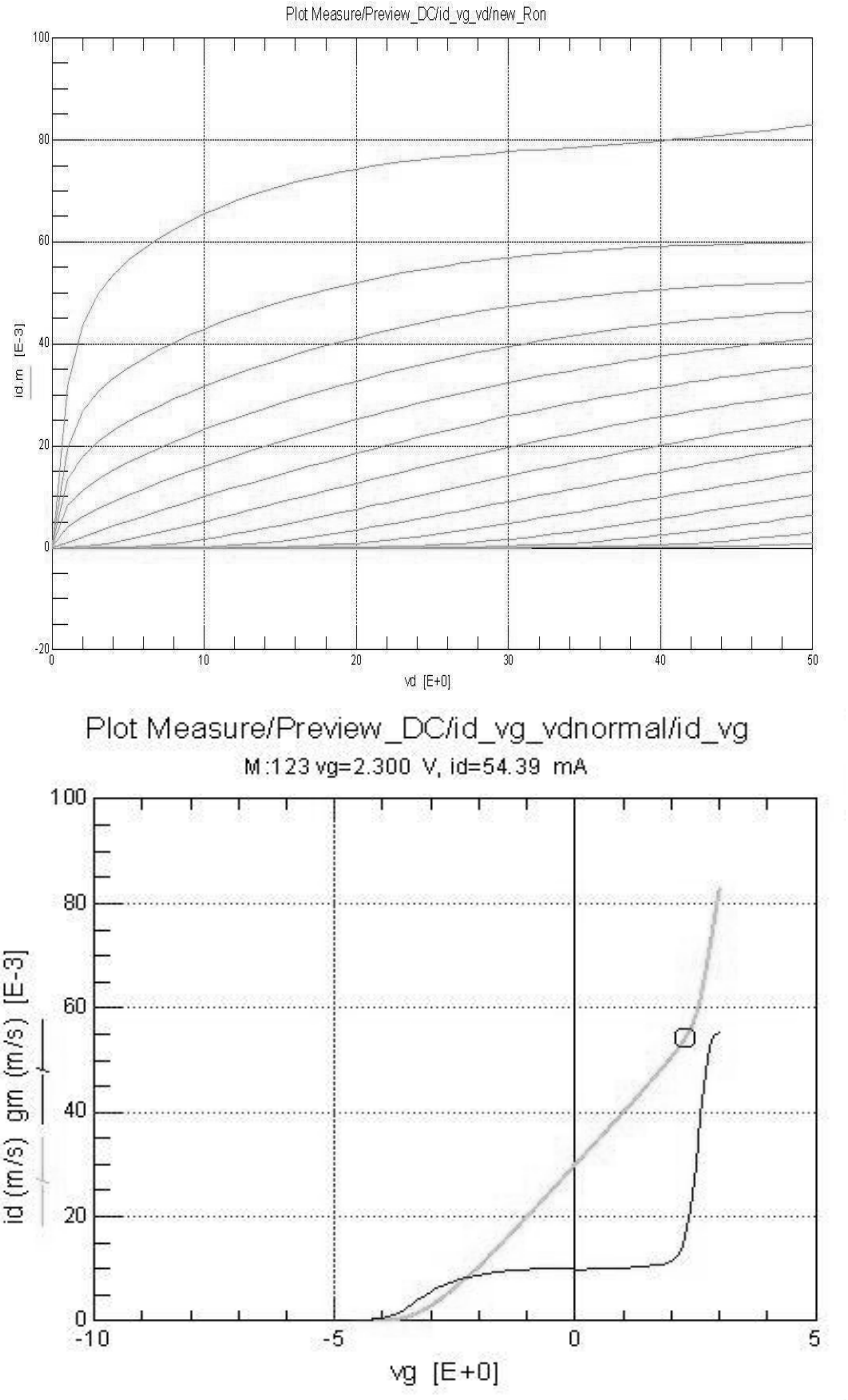


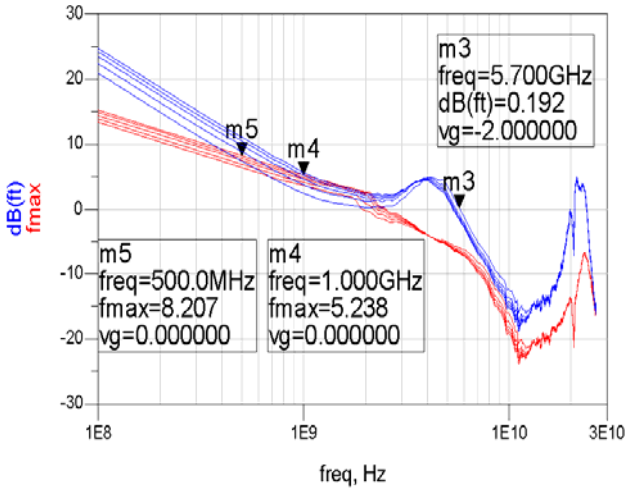
Figure 6. 0.5 mm SiC SIT I_d-V_g and G_m-V_g curve with measurement condition V_d = 50 V

The 0.5 μm wide source ohmic contacts must be aligned to the tops of these 1.0 μm wide mesas. The 0.5 μm gate ohmic contacts must be aligned to the bottom of these 1.5 μm wide channels. The gate metal formation step starts with an evaporated Ti/Pt/Au layer, formed with photo-lithography and a lift-off process. One cell has 400 source fingers and each source finger width is 50 μm. The device's gate must wrap around the base of each mesa without shorting to the source contact. Because of the device's geometry all the source contacts must be tied together via air-bridging which ultimately extends to a source contact pad via an air-bridge. SITs are completed by adding a layer of oxide passivation and depositing metal interconnection for the source electrode. The backside drain contact is formed first by evaporation and annealing of 100 nm Ni.

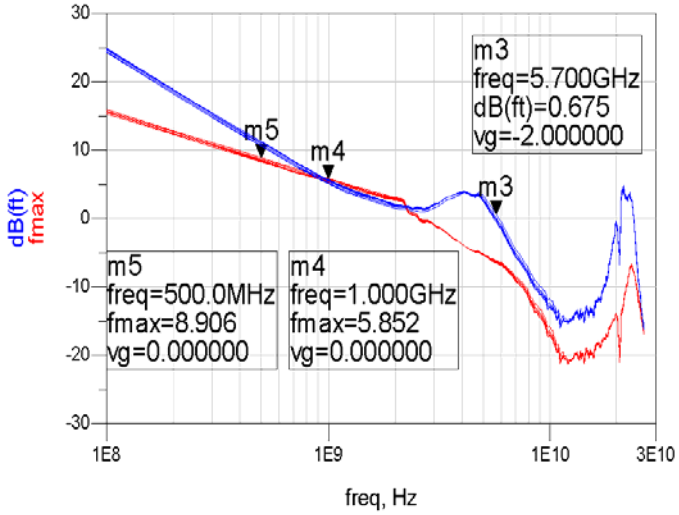
3. Results and Analysis

From Figure 6, we can know that the 0.5 mm SiC SIT yielded a maximum current density of 160 mA/mm was achieved with V_d = 50 V and V_g = 2.5 V. The threshold voltage of V_g= - 4 V. The maximum transconductance (G_m) was 22 mS/mm at a drain voltage of 50 V and a gate voltage of 2 V. The device blocking voltage with a gate bias of -16 V was 400 V.

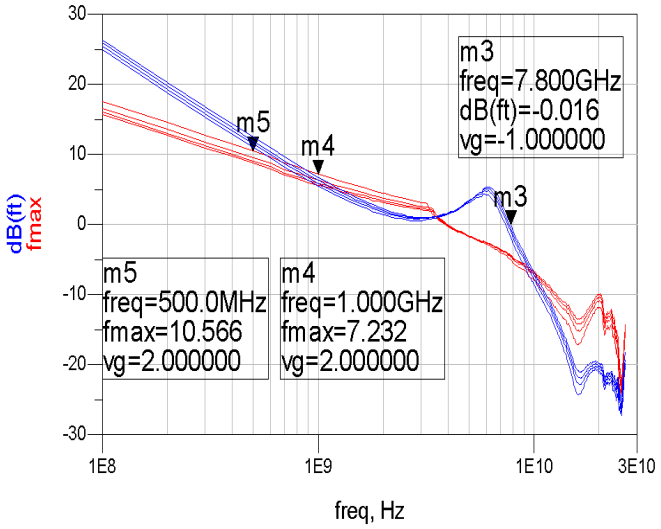
A total of one chip is attached to a 0.3 mm thick BeO substrate in a 1.5 mm thick CuW flanged package. The test fixture was designed based on the measured impedance. Figure 7 illustrates the performance of small signal. A limitation of current SiC SITs is that the MSG, which is the maximum gain that can be obtained when designed for unconditional stability, is limited to about 13 dB at 1 GHz. Small-signal radio-frequency (RF) characteristics of the SITs were measured from 0.5 to 29.9 GHz using a vector network analyzer. The measured devices had ten gate fingers with each gate width of 500 μm, for a total width of 0.5 mm. The bias was V_{ds} = 50 V or 80 V, and I_{ds} = 30 mA or 50 mA, a class AB condition that is normally used for high-efficiency power operation. The maximum small-signal gain was calculated from the s-parameters and is shown in Figure 7. It is shown in Figure 7a that V_{ds} = 50 V the SIT device shows MSG of 8.2 dB at 500MHz and 5.2 dB at 1 GHz. When the V_{ds} = 80 V, the MSG increases 0.7 dB at 500 MHz and 0.6 dB at 1 GHz, as shown in Figure 7b. Reducing C_{gd} will increase the gain (MSG) and will also improve the ease of use of the device. An effective way to reduce this capacitance is to lift off the gold wire between the gate and the drain, and the source. When the V_{ds} = 50 V and V_g = 2V, the MSG increases 1.6 dB at 500MHz and 1.4 dB at 1 GHz, as shown in compared Figure 7c with Figure 7b. Compared Figure 7d with Figure 7c, the MSG increases 0.7 dB at 500MHz and 0.6 dB at 1 GHz with V_{ds} increased to 80V and the same V_g = 2V.



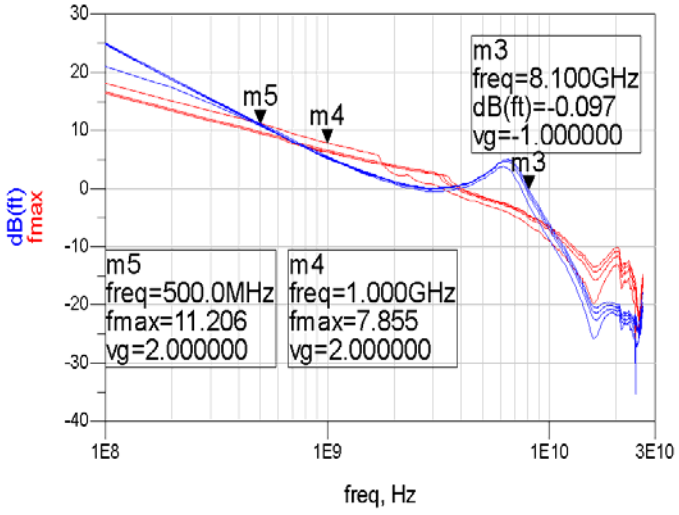
a: V_d = 50V, before Reducing C_{gd}



b: V_d = 80V, before Reducing C_{gd}



c: V_d = 50V, after Reducing C_{gd}



d: V_d = 80V, after Reducing C_{gd}

Figure 7. (a, b, c, d) 0.5 mm SiC SIT small signal measurement

4. Conclusion

SiC SITs have been shown to be appropriate for applications from UHF to S-band frequencies [7]. RF performance data of a pulse SiC SIT has been presented. This device operates at a high voltage of 80 Volts, exhibiting good small signal characteristics and high power gain, the SIT device shows MSG of 11.2 dB at 500MHz and 7.855 dB at 1 GHz. Channel currents of 300 mA/cm and blocking voltages of 400 V were measured. Because of the 400 V breakdown voltage, we can improve the device's performance by increasing the operating voltage from 50 V to 100 V. Improvements to these results are expected by packaging more 4H-SiC SIT cells.

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