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Hyper-chaotic LÜ System Simulation Design of Digital Circuit Based on DSP Builder

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Abstract

In order to overcome sensitive defects of components deviations and environment defects in analog circuit design, a novel four-dimensional hyperchaotic systems is constructed based on LÜ system. Basic nonlinear dynamics characteristics are analyzed to the new system. By optimizing the design of sampling frequency selection, gain adjustments, parameter configuration etc., the hyperchaotic circuit runs stably while the signal amplitude is reasonably controlled. Curves of the digital chaotic sequence show smooth without jagged shape. The circuit can be applied to other digital realization of chaotic systems with commonality and expandability. Its experimental results fully consistent with phase space structures of the continuous chaotic system, which shows the development of chaotic systems based on FPGA is feasible and practical.

Keywords: *hyperchaotic system, digital circuit, DSP Builder, FPGA, simulink*

1. Introduction

As the first chaotic model, Lorenz equation [1] became the chaos research paradigm. The positive Lyapunov exponent of classic low dimension chaotic system is relatively small, and the complexity of the system is not enough, as a result, it will be constrained in the practical application because of the narrow bandwidth. The chaotic systems brought by feedback extension system dimension have two or more positive Lyapunov exponents, the phase space trajectories are separated in more directions, and possess more complex in dynamical behavior, which would better meet the practical needs in spectrum spread, secret communication and radar synchronization control etc. In recent years, researchers explored hyperchaotic system effectively and made a large number of achievements [2-4].

The chaotic signal generated by the analog circuit of discrete components, is influenced by temperature, working voltage and the parameters etc, thus virtually limited the practical application of analog chaotic circuit. FPGA is a digital signal processing technology based on semi-custom by integrated chip, it support the hardware description language as the compiler through EDA software to design IC chip [5]. The system generated by this technology is less vulnerable to interference from other factors, in addition, it can be erased repeatedly and the improvement of the algorithm is very easy as well. The algorithm of the continuous chaotic system need floating-point operations, however, the computational accuracy is limited by computer digit bits. FPGA can simultaneously operate floating-point and fixed-point algorithm, and also it can divided into four formats: single precision, extended single-precision, double precision and extended double precision, according to IEEE-754 floating-point standard format. If the FPGA operate floating-point algorithm, it must set different floating-point multiplier and the corresponding module individually to meet the needs of the different realities, and this approach would result in long development cycle and higher complexity since the number of bit is limited. As for the fixed-point arithmetic of FPGA, the number of digit is less and users could set it freely according to the system requirement. Generally, fixed-point arithmetic is several times higher than computational accuracy, what's more important is, its configuration is more flexible, and development cycles are shorter. For this parameter-control sensitive chaotic systems, digitize the signal and use the fixed-point operational capability of FPGA for its extensibility will bring broad prospects for development. In fact, correlative literature had implemented the chaotic

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systems [6-8], but due to the complexity of the kinetic characteristics of hyperchaotic systems, digital circuit design of the hyperchaotic system is rarely reported in these literatures [9].

This essay investigated the generalized LÜ system in terms of its dynamic characteristics, and used optimized discrete equations in designing hyperchaotic digital systems, under DSP Builder development environment, the experimental simulation results of digital circuit are fully consistent with the conventional numerical computation one. Further more, it provides a reliable basis for the rapid development of FPGA hardware.

2. Study on Dynamics Behavior of System

2.1. LÜ System Expansion

In 2002, LÜ Jinhu obtained a new three dimensional autonomous chaotic system-LÜ system[10] in chaotic anti-control method, and later became a member of the generalized Lorenz systems. The classic system is a typical three-dimensional autonomous nonlinear systems, which can be expressed as:

$$\begin{cases} \dot{x}(t) = a(y(t) - x(t)) \\ \dot{y}(t) = -x(t)z(t) + cy(t) \\ \dot{z}(t) = x(t)y(t) - bz(t) \end{cases} \tag{1}$$

In above equation, constants a; b and c are system control parameters, $x(t), y(t), z(t)$ are state variables of the system. When the system parameters $a = 36, b = 3, c = 20$, LÜ system is in a chaotic state.

Extend one-dimension of the LÜ system variable and then feedback to the original system, equation (1) will be constituted the 4D system, which can be expressed in the following form[11]:

$$\begin{cases} \dot{x}(t) = a(y(t) - x(t)) + w(t) \\ \dot{y}(t) = by(t) - mx(t)z(t) \\ \dot{z}(t) = -cz(t) + mx(t)^2 \\ \dot{w}(t) = dy(t) \end{cases} \tag{2}$$

In above equations, the constants a, b, c, d, m are the system parameters, compared with 3D LÜ system, the four-dimensional system increases one-dimensional state and make system variable feedback in the first equation. The nonlinear function differ from 3D LÜ system, the xy in the third differential equation is replaced by x^2.

2.2. The 4D LÜ System Performance Analysis

2.2.1. Existence of Dissipativity and Attractors

In equation (2), the 4D LÜ system is a dissipative system, its divergence is:

$$\nabla V = \frac{\partial \dot{x}}{\partial x} + \frac{\partial \dot{y}}{\partial y} + \frac{\partial \dot{z}}{\partial z} + \frac{\partial \dot{w}}{\partial w} = -(a - b + c - d) \tag{3}$$

$$V(t) = V(0)e^{-(a-b+c-d)} \tag{4}$$

When $(a - b + c - d) > 0$, and $t \to \infty$ each volume element containing the system trajectory contract in the speed of the exponent $-(a - b + c - d)$, the volume element of the initial volume $V(0)$) shrink to a volume element, namely one attractor at the time t.

2.2.2. Equilibrium Point and Stability

The Jacobian matrix of 4D LÜ system is:

$$J_0 = \begin{bmatrix} -a & a & 0 & 1 \\ -mz & b & -mx & 0 \\ 2mx & 0 & -c & 0 \\ 0 & d & 0 & 0 \end{bmatrix} \quad (5)$$

It's clear that the 4D system has a unique equilibrium point $S_0(0,0,0,0)$, the eigenvalues of the 4D system matrix at the equilibrium point are $\lambda_1 = -a, \lambda_2 = b, \lambda_3 = -c, \lambda_4 = 0$. Four eigenvalues are real numbers: one is greater than zero, one is equal to zero, and the other two are less than zero. Thus the equilibrium point is an unstable saddle node.

When the parameters $a = 10, b = 5, c = 3, d = 0.6, m = 4$, the Lyapunov exponents of system (2) are LE1 =0.218367, LE2=0.1924, LE3=-0.4060, LE4=-7.87804. In this 4D system, there are two positive Lyapunov exponents greater than zero, which indicates system (2) is in hyperchaotic state. At this point, the Lyapunov dimension is:

$$D_L = j + \frac{1}{\left|\sum_{i=1}^{k} LE_i\right|}\sum_{i=1}^{j} LE_i = 2 + \frac{LE_1 + LE_2}{|LE_3 + LE_4|} \quad (6)$$

($j = 1,2, k = 1,2$)

j, k is the number of positive and negative Lyapunov exponent, respectively.

$$D_L = 2 + \frac{0.218367 + 0.1924}{|-0.4060 - 7.87804|} = 2.0496 \quad (7)$$

From above, it's obvious that the Lyapunov dimension of the chaotic system is the fractal dimension, which further validate the system (2) is hyperchaotic system.

2.2.3. Computer Simulation of Phase Space

The hyperchaotic system performance has been studied in the reference [11], the details need not be given here. In order to compare with the next experiment results of digital circuit design, this article simulated hyperchaotic system with Matlab software. The phase space trajectories of the hyperchaotic system are shown as follows:

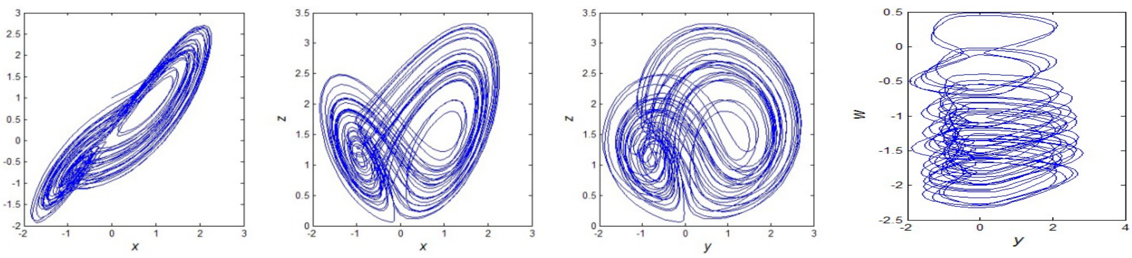


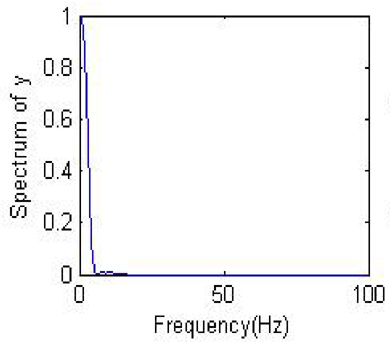
Figure 1. Chaotic dynamical trajectories of four-dimensional LÜ system

3. The Generate Rules of Digital Chaotic Signal

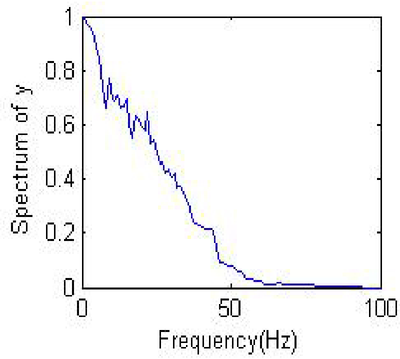
3.1. Discretization of the Hyperchaotic System

For discredited continuous system, the value of the sampling frequency f_s must be reasonable. According to the Nyquist sampling theorem, the sampling frequency f_s should be at least two times greater than the signal cut-off frequency in order to maintain the same dynamic characteristics of the discrete system with the original system. However, the chaotic system is extremely sensitive to initial conditions, dynamic characteristic is random and unpredictability, require a higher demand to sampling frequency accordingly. Chaotic system's time-domain waveform is nonperiodic, the solution sequence is extremely sensitive to the initial value, and its spectrum is continuous. In fact, the low frequency signal with relatively low amplitude has very little value in research, which can be extracted directly through simple method as low-pass filtering. And the physical characteristics of the hyperchaotic system are more complex compared with the general chaotic system.

Figure 2 is a bandwidth comparison chart of classic 3D Lorenz system and system (2) after the normalized processing through the fast Fourier transform respectively. The figure only takes the vector y of the two systems.



(a) 3D Lorenz chaotic system



(b) 4D hyper-chaotic $L\ddot{u}$ system

Figure 2. Comparison chart of the spectrum bandwidth of chaotic systems

The signal spectrum bandwidth of low-dimensional chaotic system is below 10Hz, while the hyperchaotic system is about 10~100Hz orders of magnitude[12]. As can be seen from Fig.2, the 4D hyperchaotic system is significantly larger than the 3D Lorenz system bandwidth, the bandwidth in (a) is only 4~5Hz or so, while in (b) it could reach 55Hz. The cut-off frequency of hyperchaotic system's spectral bandwidth is higher, in the process of its discrete; the sampling frequency could reach at least about 10 times of the chaotic system's.

3.2. Defects of Discrete Simulation Algorithm

Digital simulation of continuous systems based on digital integration, common methods of solving differential equations are Newton's method, the Euler method, Adams method or Runge-Kutta method. But these methods are calculation-intensive, time-consuming and can not self-start, therefore not suitable for hardware implementation. As for Euler method, its calculation accuracy is low and stability is poor. We designed digital chaotic circuit based on the FPGA fixed-point arithmetic and discrete chaotic system in a universal and fast digital differential algorithm as follows:

$$\frac{dx}{dt} = f(x_1, x_2, \cdots; x_k) = \lim_{\Delta T \to 0} \frac{x_{k+1} - x_k}{\Delta T} \quad (7)$$

Among which ΔT represents sampling time, the deformation of it is:

$$x_{k+1} = \dot{x}(t) / f_s + x_k \quad (8)$$

In above equation, $f_s = 1/\Delta T$ is sampling frequency. The discrete algorithm is relatively simple, its calculation is mainly on addition and multiplication and the computation and storage capacity are relatively small, it's suitable to realize in digital system. Literature[13-14] produced a classic Lorenz chaotic attractor. But in this kind of circuit, the sampling frequency of iterative equations is directly involved in the discrete transform operation, resulting in the difficulty in adjustment. And when the sampling frequency is getting bigger, it will directly affect the nonlinear state of chaotic system, which would make the experimental results dissatisfying. Since this kind of system has a low sampling frequency, which is only 100Hz, and its accuracy is limited, the phase space appeared jagged trajectory.

3.3. Optimized First-Order Discretization Equation

In order to overcome these shortcomings, this article optimized the discrete equations for digital circuit design of hyperchaotic system. Differential equations of LÜ hyperchaotic system(2) was discrete by first-order difference Eq.(7), the optimized iterative equation is as follows:

$$\begin{cases} x_{k+1} = [a(y_k - x_k) + w_k] / f_s + x_k \\ y_{k+1} = (by_k - mx_k z_k) / f_s + y_k \\ z_{k+1} = (-cz_k + mx_k^2) / f_s + z_k \\ w_{k+1} = y_k / f_s + w_k \end{cases} \tag{9}$$

It is worth noting that the sampling frequency f_s in equation(9) can act on linear and nonlinear term of chaotic systems simultaneously, and it will become a global gain in next digital circuit design. Thereby optimizing the circuit design, which would be easy to control the signal and limit the amplitude f_s become a global gain blocks, not directly with the vector multiplication, reducing the use of the multiplier module, thereby increasing the computing accuracy of the nonlinear term of system. More importantly, by adjusting the gain block can directly adjust the sampling frequency of the system, to facilitate the observation of test results. Theoretically, a higher sampling frequency is able to reflect the dynamic characteristics of the hyperchaotic system, the larger the frequency is, the more accurate the discrete system could reflect the original system's dynamic characteristics. But in fact is not always the case, the test below will describe it in detail, conversely, if the frequency is too small, it's impossible to get the correct simulation results.

4. Digital Circuit Design of the Hyperchaotic System

According to the characteristics of discrete chaotic system (8) and also for the purpose of facilitate further development of hardware, this article use the latest of Matlab/Simulink R2010a and the Quartus II 9.1/DSP Builder, 9.1SP2 software platform in chaotic system digital circuits designing. DSP Builder is an extension module library of Simulink, call the unit in the library directly could complete the circuit design of system-level and algorithm level, and avoid involving the underlying hardware-level design and hardware description language programming [15]. Thus, it can shorter the development cycle and lower the cost.

4.1. Hyperchaotic Circuit DSP Builder Development Environment Configuration

In the existing literature, the digital circuit of chaotic systems is still using some of the modules in Simulation. But in this paper, in order to facilitate FPGA development practice further in the Quartus II, each module of the digital circuits are taken from the Altera DSP Builder Blockset. Quartus II can not processed the Simulink mdl model file directly, so it need signal compile modules to convert system-level mdl file into a general hardware language described VHDL file, thereby create and design practical digital circuit. When the chaotic system implemented in the finite precision digital systems, will inevitably lead to degradation of dynamic characteristic of original chaotic systems, and the generated chaotic sequences have many short-period chaotic trajectories, namely short-cycle problem[16]. About this problem, it asks for higher demand on the circuit design and sampling frequency choosing. Section 5 in this article will focus on the detail study of the choice of sampling frequency.

4.2. Optimization Design of Hyperchaotic Digital Circuit

In this hyperchaotic digital circuit design, the source of the signal is unit pulse module (Single Pulse), in addition, it has data selector (Mutiplexer), Altera bus module (AltBus), common gain (Gain), multiplier (Product), parallel adder (Parallel Adder Subtractor) and constant module (Constant). The unit pulse module (Single Pulse) can produce a stable 0/1 bit stream pulse signal and not affected by other external factors, it's very appropriate to be source of this system. Meanwhile, to ensure the accuracy of each vector, the circuit uses a bus width of up to 32 bits.

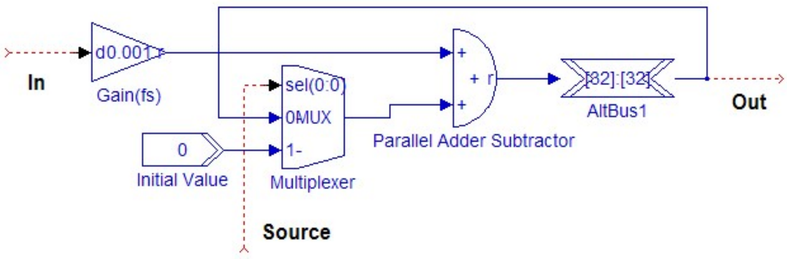


Figure 3. Digital integrator that can adjust the sampling frequency flexibly

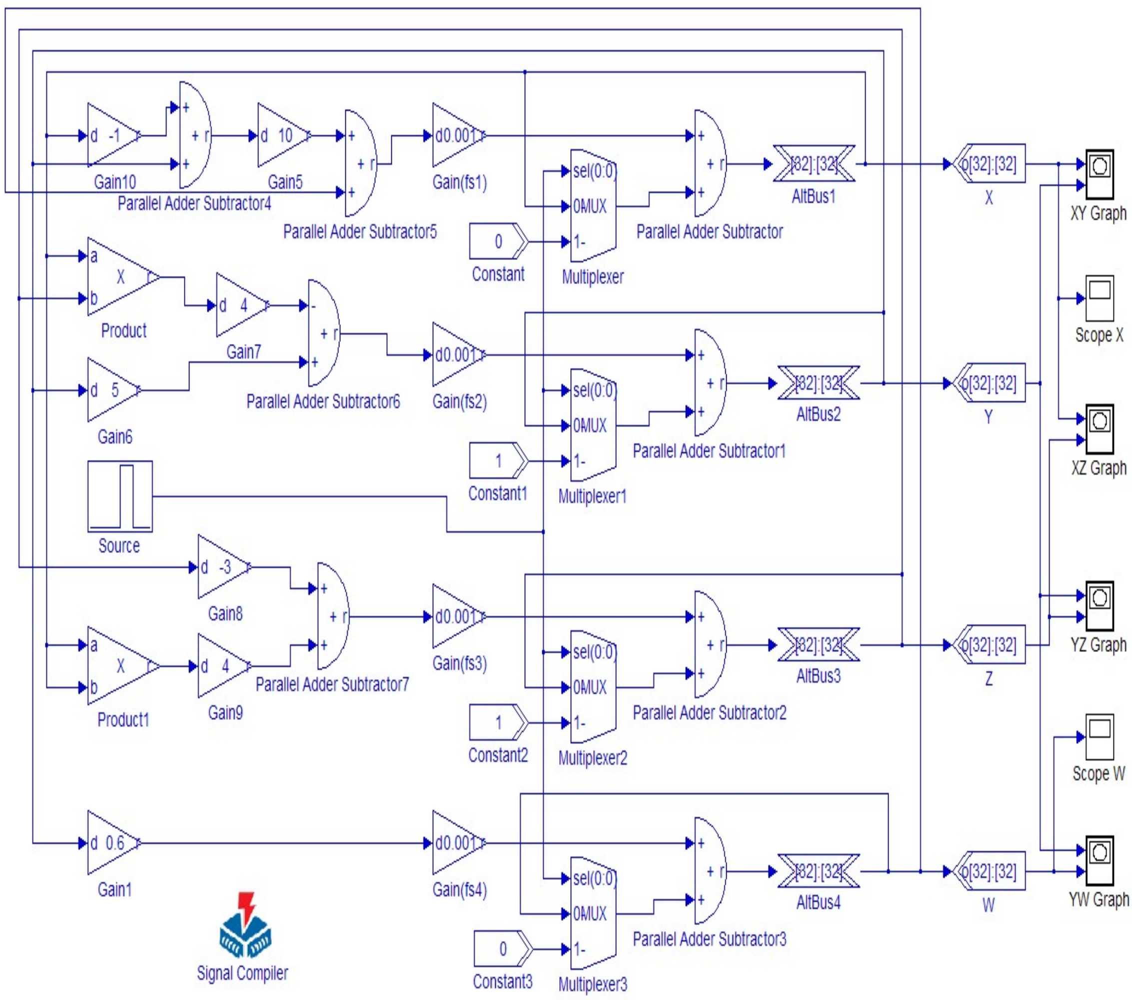


Figure 4. Digital circuit of hyperchaotic system based on DSP Builder

The sampling frequency of the digital chaotic systems is the reciprocal of the value of Gain Block Gain (f_s). The initial value can be set by the constant module (Constant). Figure 4 is the diagram of chaotic digital circuit designed by DSP Builder. We can see from the figure that the sampling frequency f_s=1000Hz and the system initial value is (0,1,1,0). This circuit is a feedback network, signal x, y, z and w is feedback to the data selector and constitutes a digital integrator circuit; XY=XZ=Y Z=YW Graph is the module in Simulink, mainly for viewing the x, y, z, w signal phase space trajectories obtained through simulation. At the same time, Scope module can monitor real-time chaotic sequence waveform of each vector. Save the file in mdl file format after the circuit design is completed, and start the FPGA simulation of hyperchaotic attractors in Simulink.

5. Experimental Results of Chaotic Digital Circuit

5.1. Comparison Test under Different Sampling Frequencies

By optimizing the circuit design, increasing the sampling frequency, the phase space trajectories of the discrete system do not appear jagged in the experiment, nor do the short cycle chaotic trajectories. Figure 5 is the chaotic time sequence of x, w vector that observed through digital circuit oscilloscope. The chaotic time sequence of each vector can be used directly for the chaotic modulation or chaotic encryption. As comparative studies, when adjusting the sampling frequency, compare the each space's phase diagram of the digital chaotic LÜ systems (9). Sampling time of the system is controlled by the gain, and it could be adjusted flexibly when bus bandwidth is enough. Thereby it is easy to control the precision and avoid the problem of short periodic orbits and jagged trajectories. The experiment monitored circuit system's operating conditions by simulating the oscilloscope and the phase space trajectories diagram, and the results turn out to be satisfying.

In the experiment, when the sampling frequencies of digital chaotic circuits are different, the hyperchaotic phase space trajectories are not the same as well. Through observation we could find that it's impossible to obtain the correct experimental results when the sampling frequency is low (f_s =100Hz). When the sampling frequency (f_s =500)Hz gets higher, the chaotic trajectory is more clear, stable and can better reflect the dynamical behavior of chaotic systems. But the magnitude of the signal is devious and the convergence state of the chaotic trajectory is not ideal neither. However, when the sampling frequency increased to a certain extent (f_s =1000Hz), we can obtain phase diagram consistent with the simulation. At that time, the trajectory of the discrete chaotic systems is clear, stable and chaotic signal amplitude is the same with the original continuous system; the experimental results are fully consistent with the Matlab simulation.

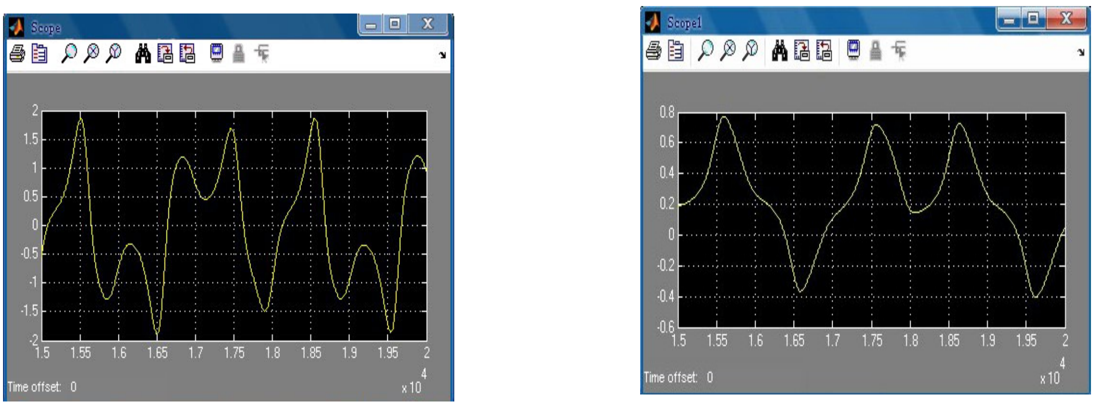
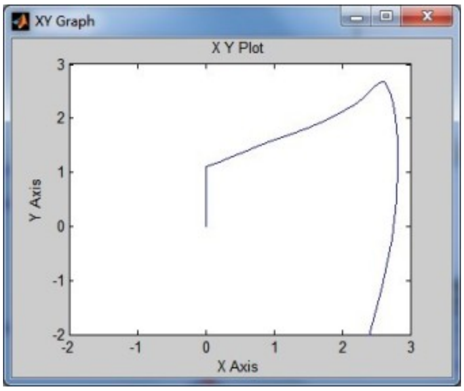


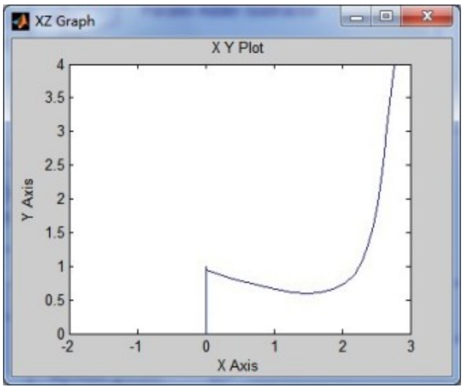
Figure 5. Chaotic time series of x and w vector

(1) when f_s =50Hz

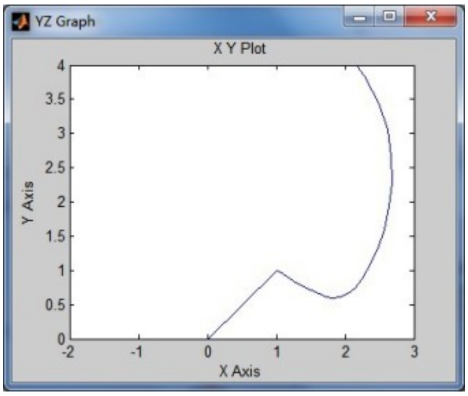
Figure 6 shows that when the sampling frequency is 50Hz, you can not get the phase diagram of super chaotic attractor, and at the same time, the chaotic signal trajectory is divergent and uncontrollable. This article has discussed the digital chaotic system requirements on the sampling frequency in Section 3.1. In view of the hyperchaotic system spectral bandwidth, the complexity of the dynamic characteristics and other reasons, we can not get the ideal experimental results when the sampling frequency is too low.



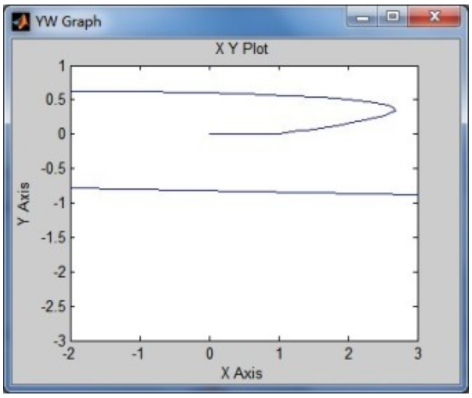
(a) $x-y$



(b) $x-z$



(c) $y-z$

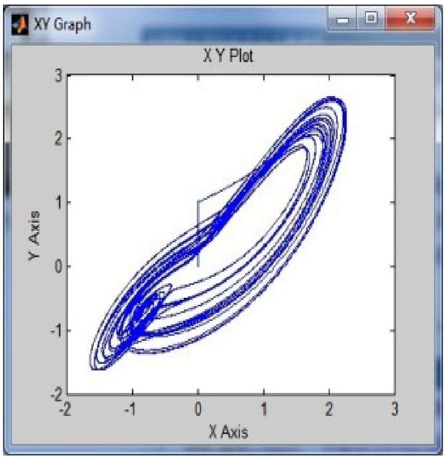


(d) $y-w$

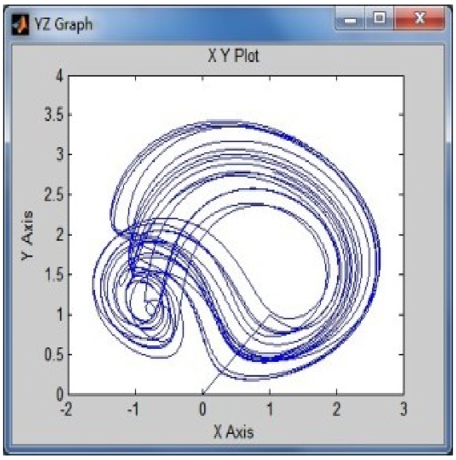
Figure 6. Plane phase diagram of digital hyper-chaotic system attractor (f_s =50Hz)

(2) when f_s =250Hz

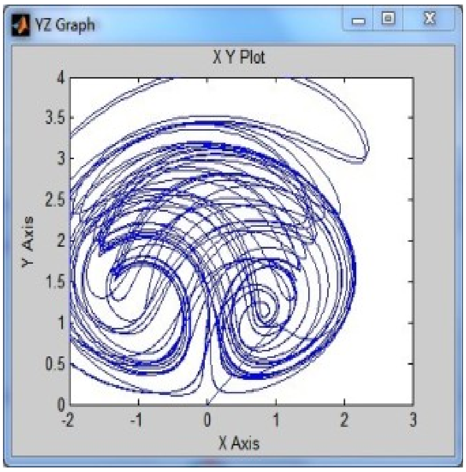
Figure 7 shows that when the sampling frequency is 250Hz, we are able to obtain the phase diagram of hyperchaotic attractor. However, through observation we can find that there is a big difference between the chaotic attractor and the obtained simulation results. Although the attractor has generated, its track is still in divergent trend. Compared with Figure 1, the deviation of the phase diagram is mainly reflected in the shape of chaotic attractor and the amplitude of chaotic signal. In the simulation of Figure 1, the amplitudes of each chaotic signal vector are $x \in (-2,3), y \in (-2,3), z \in (0,3.5), w \in (-2.5,0.5)$, which has a significant difference with those of Figure 7.



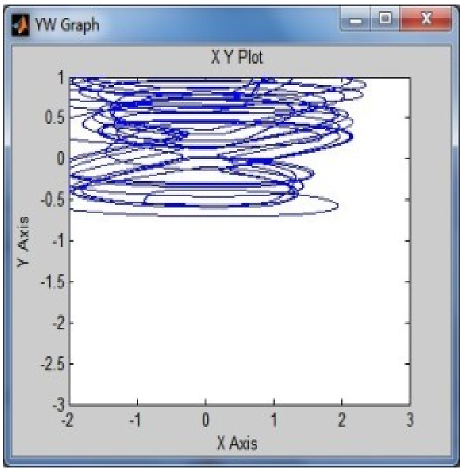
(a) $x-y$



(b) $x-z$



(c) $y-z$



(d) $y-w$

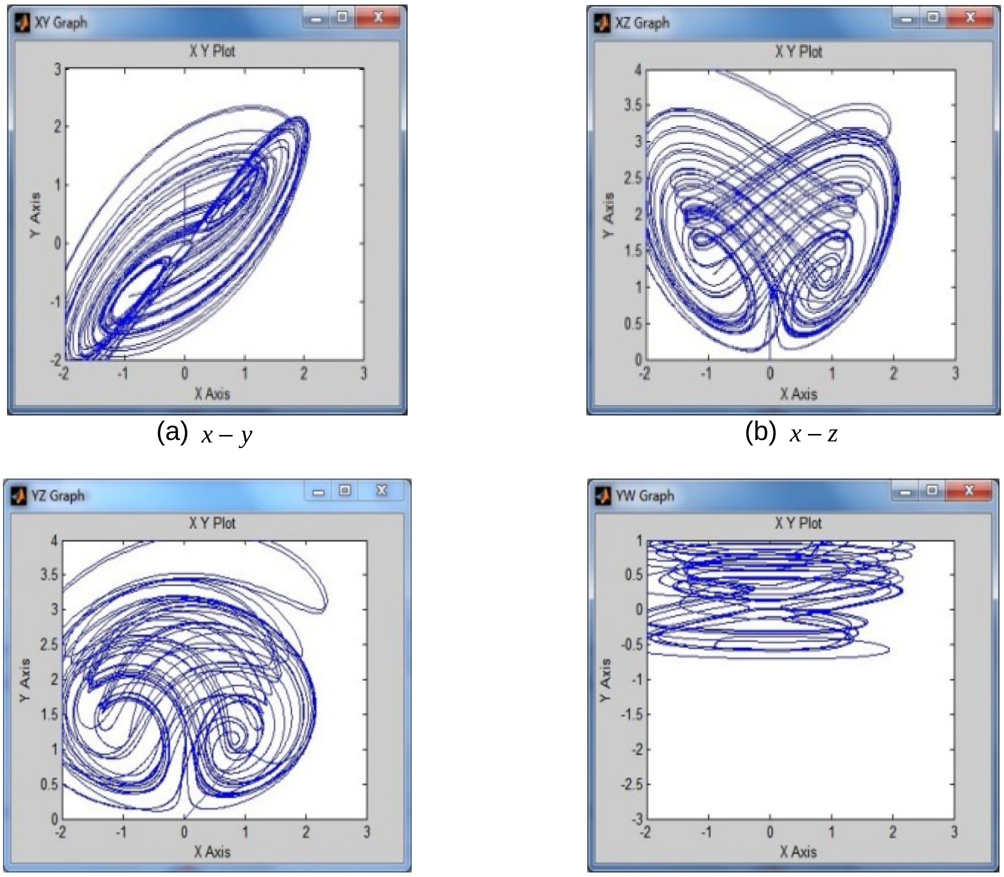
Figure 7. Plane phase diagram of digital hyper-chaotic system attractor (f_s =250Hz)

(3) when (f_s =750)Hz

Figure 8 shows the obtained attractor when the sampling frequency is 750Hz. In this situation, the signal amplitude is pretty much the same with Figure 1, the shape of the attractor is also somewhat similar, but is more symmetry. However, the chaotic attractor trajectory fitting phenomenon appeared, namely quasi-periodic rail, what's more, the chaotic dynamics characteristics degrade compared with the original continuous system. Therefore, the experimental results obtained in the conditions are still not ideal.

(4) when f_s =1000)Hz

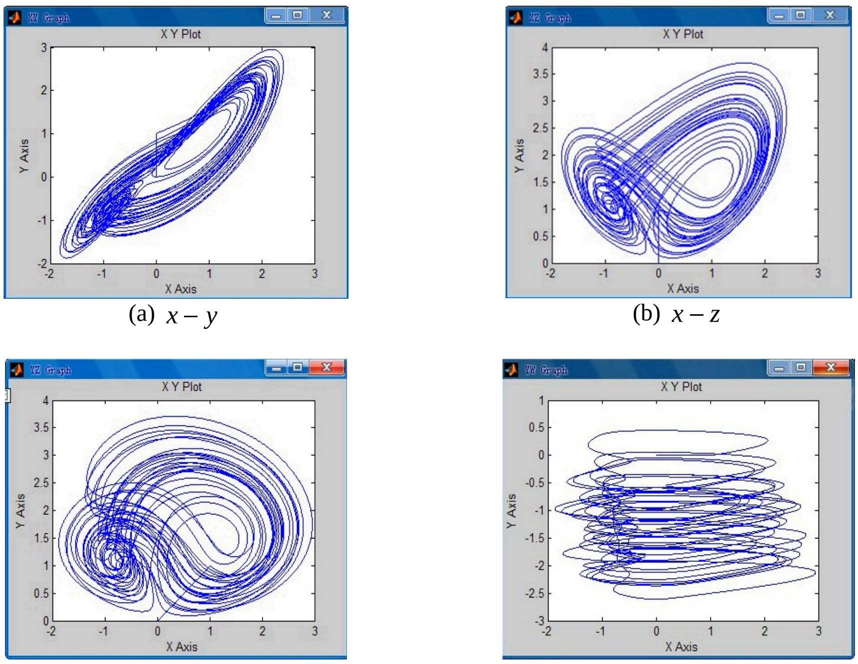
Figure 9 shows the ideal plane phase diagram of digital chaotic signal when the sampling frequency is 1000Hz. Through observation we could find that: shape of the digital phase diagram's hyperchaotic attractors in Figure 9 is exactly the same of the simulation in Figure 1. The magnitude of each vector is about, almost entirely consistent with the simulation results. Considering the error between the digital chaotic systems after sampling and the original system, the experimental results at this time is ideal, so as to achieve the expectations of the design of the hyperchaotic digital circuits.



(a) $x-y$ (b) $x-z$

(c) $y-z$ (d) $y-w$

Figure 8. Plane phase diagram of digital hyper-chaotic system attractor (f_s =750Hz)



(a) $x-y$ (b) $x-z$

(c) $y-z$ (d) $y-w$

Figure 9. Plane phase diagram of digital hyper-chaotic system attractor (f_s =1000Hz)

If the sampling frequency got higher, the observed attractor will be closer to the program simulation results shown in Figure 1. However, with the sampling frequency increasing, the step of the simulate operation will become shorter, and computation will increase in the order of magnitude, resulting in the timing of running a digital system is too long. Therefore, the premise of select sampling frequency is to ensure that the chaotic dynamics characteristics are not degraded. Table 1 is the simulation time consumed by the different sampling frequency system, under the same attractor phase diagram of expected and the original continuous system (2).

In summary, through comparison, the experimental results are the most ideal and most practical when the sampling frequency f_s is 1000Hz. In the existing literature ,when the digitized sampling frequency of 3D Lorenz chaotic system reached 100Hz, it's able to obtain attractor phase diagram , but still not ideal. But as for hyper-chaotic LÜ system, the sampling frequency have to reach 1000Hz to get the desired results, which consistent with the generated rules of digital chaotic signals in Chapter Two. Literature on chaotic digital rarely involve the exploration and experiment on the effect of sampling frequency on chaotic dynamics. In the general discussion, it just has the phase diagram of attractors, even if the signal amplitude and trajectory are mentioned, it did not give the analysis and interpretation. In this article, by comparing the testing and analysis, it demonstrated the importance and impact that sampling frequency imposed on the digitized hyper-chaotic system.

Table 1. the simulation time-consuming of digital chaotic system comparison and the corresponding phenomena under the conditions of different sampling frequency

Sampling frequency (Hz)	Time consuming (s)	Chaotic attractor representation analysis
50	-	The phase diagram trajectory is divergent and unpredictable, cannot get chaotic attractor. No discussion on the significance of simulation time.
100	0.01	The phase diagram trajectory is divergent and unpredictable, cannot get chaotic attractor. No discussion on the significance of simulation time.
200	6	The phase diagram shows the chaotic attractor appeared, but its trajectory is divergent, chaotic dynamic characteristics degenerate. The signal amplitude and shape of the attractor have a great difference with the original continuous system, simulation consumed time is very short.
250	8	The phase diagram shows the chaotic attractor appeared, but its trajectory is divergent, chaotic dynamic characteristics degenerate. The signal amplitude and shape of the attractor have a great difference with the original continuous system, simulation consumed time is very short.
500	18	chaotic attractor appears in the phase diagram, but the track overlaps and have quasi-periodic movement . The signal amplitude is almost the same with the original continuous system, but the dynamic changing trend between them varied greatly, the simulation consumed time is short.
750	32	the chaotic attractor appears in the phase diagram, close to the original system . But the track overlaps and have quasi-periodic movement. The signal amplitude is almost the same with the original continuous system, so are the dynamic changing trends between them, the simulation consumed time is average.
1000	80	Obtained the phase diagram that almost the same with the original continuous system, the magnitude and the dynamic changing trend consistent with the original system. Simulation consumed time is average. The experimental results are satisfying, and there is a good balance point between the theoretical requirements and practical needs.
2000	600	Obtained the phase diagram that almost the same with the original continuous system, and similar with the attractor phase diagram trajectory which under the condition of 1000 Hz. Frequency doubled while the simulation consumed time increases by more than ten times, thus have little practical value.

In summary, through comparison, the experimental results are the most ideal and most practical when the sampling frequency f_s is 1000Hz. In the existing literature ,when the digitized sampling frequency of 3D Lorenz chaotic system reached 100Hz, it's able to obtain attractor phase diagram, but still not ideal. But as for hyper-chaotic LÜ system, the sampling frequency have to reach 1000Hz to get the desired results, which consistent with the generated rules of digital chaotic signals in Chapter Two. Literature on chaotic digital rarely involve the exploration and experiment on the effect of sampling frequency on chaotic dynamics. In the general discussion, it just has the phase diagram of attractors, even if the signal amplitude and trajectory are mentioned, it did not give the analysis and interpretation. In this article, by comparing the testing and analysis, it demonstrated the importance and impact that sampling frequency imposed on the digitized hyper-chaotic system.

5.2. The Configuration and Expansion of Hyperchaotic Digital Circuit

By simulating circuit to design chaotic system, the redesign of the same type of system is also very complex for it must replace components. Traditional operational amplifier, analog multiplier, and resistance are limited, there are errors and in practical application, the results are not ideal. Yet in this article digital circuits have following advantages:

(1)By Gain changing, we can re-configure the linear and nonlinear parameters of chaotic system's differential equations, and also be able to adjust the system sampling frequency conveniently. Meanwhile, the constant module can adjust the system initial value.

(2)The circuit has few types of modules and its structure is very simple, but stability and scalability of it are high. By changing and adjusting the adder and multiplier, it still can be applied to other digitized chaotic systems.

(3)The digital circuit fully adopt the latest DSP Builder module, thus, it could do simulation tests in Matlab and generate VHDL code through compiling and further more, burn rewritable FPGA hardware by the Quartus II software. Development costs are relatively low, which enables convenient development.

6. Conclusion

This article is based on modern digital signal processing technology; it improved digital circuits through optimized discrete equations, designed and implemented the digital circuits of the hyperchaotic LÜ system. The circuit system can operate on real numbers, the discrete chaotic signal is stable and through the directly adjustment of the gain block and constant module can achieve the parameter configuration of chaotic system. The circuit can also be applied to the digital realization of other chaotic systems. Sampling frequency of the digital circuit is controlled by the gain and can be flexibly adjusted; the accuracy is improved by an order of magnitude than the relevant literature system. It also eliminated the jagged trajectory and avoided the problem of short periodic orbits. Experimental results are very satisfactory; the phase diagram gained by circuit running is exactly the same with Matlab simulation. All the digital circuits in this article adopted the latest Altera DSP Builder module; they can be converted to VHDL language via compiling, and use with Altera QuartusII. Thereby enable the rapid development of FPGA hardware, which have some theoretical and practical value.

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