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The Realization of LED Display System Based on the Embedded

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Abstract

In this paper, a design of LED display control system based on ARM and FPGA is proposed, according to module structure characteristics of the RGB three colors LED display and the dynamic scanning display of the LED display which is achieved by FPGA technology, this system uses ARM chip S3C2240 as the control core. with the help of the programmable logic device auxiliary, it completed the data storage and update, display refresh, animation, cycle display; and achieved communication through Ethernet and PC; the system supports text's and picture's display of full color LED screen which is separated in 256 grayscale, and a remote data transmission.

Keywords*: full color LED display, embedded, gradation control, FPGA, driving circuits*

1. Introduction

LED display technology combines computer technology, microelectronic technology and information processing together in a body, having advantages of displaying abundant colors, wide dynamic defense, high brightness, long life, stable and reliable operation and so on, now the technology is becoming the most competetive display medium of the new generation [1]. In today's world, LED display has been widely applied in the banking, securities trading, highway signs, airport, advertising and other fields [2]. From the business perspective, it is not necessarily advanced technology can be workable in the market, for example the FPGA as the core of the LED display control system design ,it is more complex to realize. And at the same time, due to the need for high performance FPGA chip, the cost is much higher. While it is not flexible enough using the processing chip of 32 bits as the core of the LED display control system, when the LED screen size is changed, that will lead to drastically alter in the design of the system.

This paper presents a new type project of LED color display control technology based on embedded. aimed at the existing problems in the LED asynchronous display system, combined with the main function and technical index of LED synchronous display system, it puts forward technical scheme to solve the key problems. Taking use of The characteristics of the ARM processor portable operating system, controller with LCD and graphics interface system, the paper regards the ARM system as a video source, using ARM+FPGA technology, it adopts ARM9 chip as the main control unit, FPGA chip as the scanning control unit, and it can simplify circuit structure effectively, and can improve the reliability and flexibility of the whole control system [12].

2. Composition and Working Principles of the System

2.1. Working Principles of Full Color LED Display Screen

The color synthesis principle of full color LED display screen is similar with the color TV sets'. It selects red, green and blue as three primary colors of image, and each pixel consists of LED constitute which has red, green, blue three colors, and it can realize the synthesis of a variety of colors by controlling the LED brightness. As the area of LED color screen is generally larger than $1m^2$, and it is often used in the occasions of remote viewing, so the three kinds

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colors of LED of each group of pixels still belong to the same space on the vision [3], when they emit light at the same time, they can be mixed into a different color. Therefore LED with different brightness in three colors can produce a variety of color effects.

LED electronic display screen has many independent arranged pixels. The separability of pixels leads to that controlling and driving of LED light can only be proceed in digital mode [4]. Emitting state of these pixels is controlled by the controller synchronously, and drove independently. Full color display of Video means that the brightness of red, green, blue, three kinds of color of every pixel is controlled separately, and those must be completed in the specified scanning time synchronously. Large screen is composed of tens of thousands pixels, this makes the system raise very high requirements for the overall data transfer rate. For every pixel point it is obviously not realistic to provide it with a conventional D/A, so we must find a solutions of reducing system complexity greatly and the highest performance as far as possible.

The average brightness feeling of man to one pixel can depend on its bright/dark duty ratio. That is to say, as long as we changes the pixels' bright/dark duty ratio, we can achieve the control of brightness. In terms of The LED electronic display screen, it means to turn the data represented pixel brightness into the pixel luminescence time (D/T conversion).

Set screen refresh cycle as T_s, control the data of arbitrary pixel brightness as N bits $D=\sum_{i=0}^{n-1} b_i 2^i$ (where $b_i = 0$ or 1), T_{0N} is the luminescence time corresponding to the D, then the pixels bright/dark ratio is: $T_{0N} / T_S = D / 2^n = \sum_{i=0}^{n-1} b_i 2^i / 2^n$. This expression can be used to realize the prefabricated subtraction counter, but each pixel with a counter makes the display circuit extremely complex, this expression can be rewritten as: $T_{0N} = T_S \sum_{i=0}^{n-1} b_i 2^i / 2^n$, this means T_{0N} can be divided into several time segments, because when T_S is short enough , the visual effect of T_{0N} the sum of several time segments is the same with a total length of the same continuous T_{0N}.

So in general, for the N bits binary data $D=\sum_{i=0}^{n-1} b_i 2^i$, divides T_S into n segments, and selects the appropriate time partition function $f(i)$, and set the section i: $T_i = T_S f(i)$, (where $0 < f(i) < 1$, $I = 0,1,2,\cdots,n-1$). The circuit realizes to make the pixel light /dark controlled by D's position n (b_i), thereby

$$T_{ON} = \sum_{i=0}^{n-1} T_i b_i = T_S \sum_{i=0}^{n-1} f(i) b_i \quad (1)$$

Now $$d = T_{ON} / T_S == T_S \sum_{i=0}^{n-1} T_i b_i / T_S = \sum_{i=0}^{n-1} f(i) b_i \quad (2)$$

This is the bright/dark duty ratio of this pixel. As a result of the function $f(i)$ can be shared by all the pixels, as it shows above, as long as we use $f(i)$ to control each pixel point, we can achieve that all pixels of the full screen are independent of each other and their the D/T conversion of synchronization.

2.2. Design Target of the LED Display Control System

The design target of the system has the following several points:

(1) LED display system can be off-line display, using the ARM system as data source rather than the host computer;
(2) Specification of display is 128×256 columns.
(3) It can achieve grayscale display with 256 gray levels, in accordance with the specific effect of display images;
(4) It can receive the information and settings displayed on the PC through the serial port;

(5) Display primaries of LED screen are red, green, blue;
(6) The display can refresh 70 times per second.

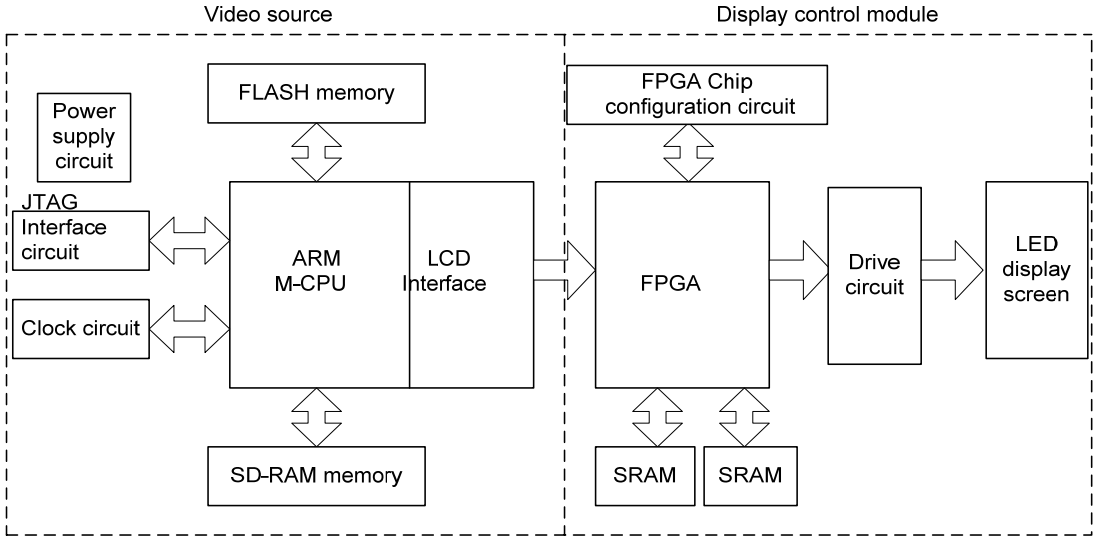

Figure 1. Block diagram of LED display control system based on ARM and FPGA

In order to realize the goal function, the system chooses 32 embedded RISC microprocessor based on ARM core and SDRAM as the control center, and selects FPAG and double RAM as scanning control module. The storage module is composed of FLASH, transferring data on Ethernet. PC transfers image data to the Ethernet interface module, the module analysis protocol and then receives data, and next transmits the data to the control core S3C2410, the control core then writes the data received to the storage module NAND FLASH. In the display process, S3C2410 transmits the data to the scanning control module based on the FPGA technology [5], by reading the data stored in the FLASH, and the module transmits image data after processed to the LED screen to display. The Block diagram of LED display control system is given in Figure 1.

As for the part of software programming and simulation, it mainly includes the design of ARM embedded software and FPGA control module.

(1) According to the design requirement, the design uses the embedded system, so as to provide a stable and reliable video source for the LED display. The S3C2410 chip is chosen as the control of the video source core. Thus in the software, the embedded Linux is chosen as operating system, which has the characters of open source, good stability, high security features.

Because the embedded operating system transplant programme has been very mature, and LCD driver and Qtopia transplantation has been applied in a large number of embedded system. So this part is abbreviated.

For the software of the entire S3C2410 system, it mainly consists of the boot loader, device drivers, embedded Linux Kernel, file system, graphical user interface system. The platform structure of system software is shown in Figure 2.

(2) The portion of FPGA control unit software receives display data and control information from the ARM system. After the display data is dealt with and reconstructed,it is sent to gray scale scanning control module, which is explained based on the weights to different gray scale information, and then the data signal and the control signal is sent to the LED display screen driving circuit. There are three parts in the LED display screen display control module, such as ARM interface buffer module, SRAM read and write control module and control module of gray scale scanning.

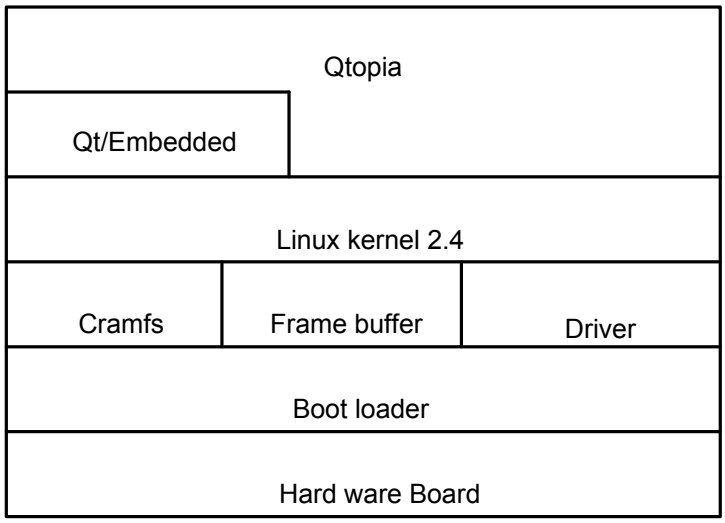

Figure 2. Structure of system's software platform

3. Design of System Hardware

3.1. Selection of Processor

S3C2410 is a processor based on ARM920T core. Considering the characteristics of S3C2410. The working frequency of S3C2410 processor can improve the speed of operation of the system greatly, the frequency can make the processor run easily on Windows CE, Linux operating system and so on, and deal with more complex information, reducing the time of software development greatly; S3C2240 has powerful internal interrupts and TCP/IP, both can be polling called; there are as many as 117 generic Programmable Multifunction I/O ports that can be connected conveniently with the Ethernet controller RTL8019AS; S3C2410 has abundant peripheral resources, this can greatly simplify the extension portion of the peripheral circuits and reduce the complexity of the system, therefore S3C2240 is selected as the CPU of the system [13].

3.2. Selection of Memory

In order to meet the needs of the large capacity and high speed data processing, and use the SDRAM controller interface provided by ARM microprocessor memory interface [10], this design adopts SDRAM of memory with the highest literacy rate in the embedded application to run as the space of data processing and display, in fact, the chip named K4S561632D is produced by SAMSUNG, it is a synchronous DRAM of 4M×16bit×4bank, whose size is 32 MB. Using 2 pieces of K4S561632D parallel construct the 32 SDRAM memory system, one is for the high 16 bits, other is for the low 16 bits, that the total width of the data bus is up to 32 bits, and the total capacity is up to 64MB. The address space was mapped in the bank6 of S3C2410, that is to say, the chip select signals of the bank6 of S3C2410 are connected to CS end of two pieces of K4S561632D. The connection of S3C2410 to one of SDRAM is shown in Figure 3.

3.2. Design of Ethernet interface circuit

Ethernet circuit module solves the problem of remote data transmission effectively [6]. The system uses a full duplex Ethernet controller RTL8019AS produced by RealTek company, the controller has plug-and-play functions. At the same time, it also supports Ethernet extension of the S3C2410, and its main features include: supporting for IEEE 802.3; a full-duplex transceiver and the speed up to 10Mb/s; the built-in 16KB SRAM used for sending and receiving buffer; supporting for the 8/16 data bus, 8 interrupt request lines and 16 I/O base address selections; supporting for 10Base5, 10Base2, 10BaseT and detecting the connection medium automatically. RTL8019AS and S3C2410 is in the jumper mode, without using EEPROM, also without the ISA bus, all of the pins connection mode is JP connected with high level, BS[4..0] are connected with ground, only using BROM; and IOS[2.. 0] are connected with ground, the internal register base address starts from 300H; using IRQ2/9 as an interrupt request pin; AUI is

connected with low level, the interface works in BNC way, using twisted pair or coaxial cable; PL1, PL0 are connected to low level, detecting Ethernet interface type automatically; after TPIN and TPOUT signal through a coupler FB202, connected to an external Ethernet through the RJ45.

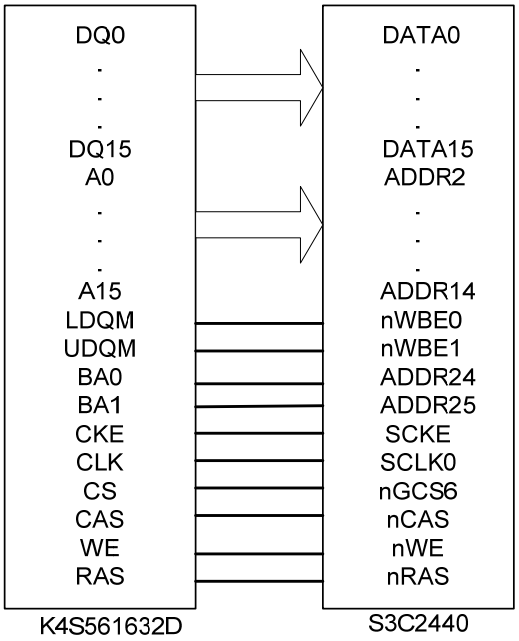

Figure 3. Interface circuits of control of the core and SD-RAM

3.3. Design of Memory Module

The memory module of screen control system needs to store binary executable code, also needs to store large amounts of text and image data, so as to provide asynchronous display of picture source. It is required that picture and text data will not be lost when the system is out of power, and it needs a larger storage space, so this system decides to adopt the FLASH memory. S3C2410 supports the start of NAND Flash and NOR Flash, since the NAND Flash has advantages of a large capacity, a lower price than the NOR Flash and so on. This design uses the combination of the NAND Flash and SDRAM, so it can achieve a great cost performance [7]. The memory module of the system selects NAND FLASH memory K9F1208 of Samsung Corp which has the characters of a large capacity, a high reliability. K9F1208 is NAND Flash memory whose size is 512Mb (64M×8bit) produced by Samsung. The reading and writing of the chip's address, data and control word is conducted by multiplex 8 bit I/O interface IO[0-7], so it can be achieved to extend storage capacity without changing the design of hardware. The chip specific operations such as reading, programming, erasing is achieved by producing a corresponding command word through addressing the internal control register. Next is the mode of operation of various state signal: address operation, as the write signal WE and the chip selection signal CE are effective, is conducted by enabling ALE effective to latch the address data; data operation, as the write sign WE and the chip selection signal CE are effectively, is conducted to latch in the rising edge of signals; the command word operation, as writing the signal WE and the chip selection signal CE are effective, is conducted by enabling CLE to latch. The interface circuit of S3C2410 and NAND FLASH is shown in Figure 4.

3.4. Design of Scanning Control Module

Scanning control module is the important component of the LED display control system, because the display of the LED screen is conducted in contact to tell, while it complete scan of image's tell in real-time, accept new data, in order to update the screen, so there must be processing circuit of cache of tell data, to prevent from losing data in the scanning process [8].

The module consists of a FPGA and a double RAM. As implement RGB data buffer output by the S3C2410, and under control of a synchronization signal, finish the read and write operations of double RAM named table tennis operation. The so-called table tennis operation is that while FPAG read data from X RAM , write data into Y RAM, in turns it also establishes, in this way it improves the data processing speed of FPGA, realizes the accept of image tell scaning and new data at the same time.

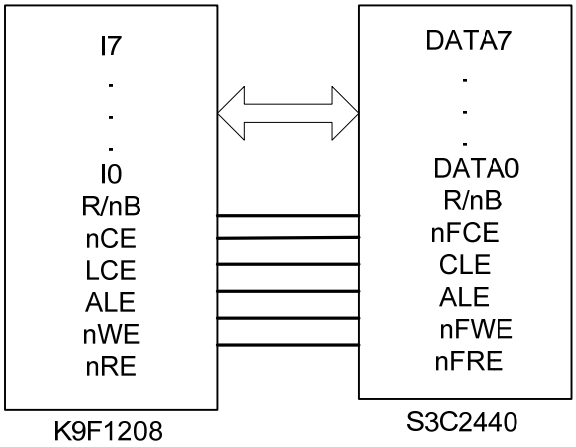

Figure 4. Interface circuits of S3C2410 and NAND FLASH

Among them, FPAG in the module selects Cyclone EP1C6Q240C8, which is a cost-effective FPGA launched by Altera, whose voltage is 3.3V, core voltage is 1.5V, and high working frequency is 200MHz ,which has 185 I/O pins; the FPAG adopts 0.13 μM technology, SRAM technology of copper, and its density is 5980 logical unit, it contains 20 RAM block (M4K module) whose size is 128×36, and RAM total space reaches 92160, besides, the RAM block inside can realize Real double port, simple double port and single port function, and can support shift register and ROM mode; it embed 2 phase-locked loop circuit inside, which can provide clock management ability of high performance, so that the phase-locked circuit has a clock synthesis function, the frequency of the internal clock actually operating may be different from the input clock's. Each phase locked loop can provide 3 different frequency output. EP1C6Q240C8 is characterized by simple operation, high accuracy, and strong drive ability, and it satisfies the need of design's real-time and high frequency requirements.

The resolution of system LED display screen is 128×64, and capacity of each frame of image needed is 192Kb. The system chooses IDT71V3577 type of IDT company as SRAM, whose capacity is 128K×32bit, so the system needs 2 pieces of IDT71V3577 to store a frame of images. Therefore the system uses 4 pieces of IDT71V3577 as a double RAM to store display data.

Design structure of logic circuit [11] of scanning and controlling is shown in figure 5. Address controller generates a writing address of display memory and reading address of memory, it is the read-write controller to decide whether to write the data and connect address with memory or to read data and connect read address with memory. In order to meet the need of the image display of the screen, and display the mode of control circuit design is gray scale display mode. After decode gray scale, it converts parallel data of 4 bits into the serial data of gray scale information of 16 bits which is desired LED display screen.

Due to the table tennis operation of X, Y two groups of memory, during the time of receiving a frame of parallel data, it can send the 16 bit serial data streams that have been decoded to the LED screen, the rate of inputting data is 2 Mbit/s, rate of reading out the data flow reaches 32Mbit/s. If send serial data streams whose rate is 32Mbit/s directly to the display screen [8], then the velocity of transmission is too high to handle the data. The system whose display screen area is 128×64 , adopts 8 line scanning method. The area scanned consists of 16 scanning units whose size is 8×64. If the 16 scanning units are scanned simultaneously, that

can reduce the rate of data streams. Data is written to the memory according to the time sequence, decoding gray level into serial data stream that is red, green, blue three kinds, whose rate is 32Mbit/s, so that it can been scanned and displayed. After processing the rate of the serial data flow is 32/16=2 (M bit/s), the flow can be used by displaying circuit [9]. When the time sequence is written into the memory, the data cannot be read according to the original address. It read data out according to the time sequence, These operators are controlled by read/write controller and address controller. And synchronous controller generates a clock signal, a latch signal and line scan signal.

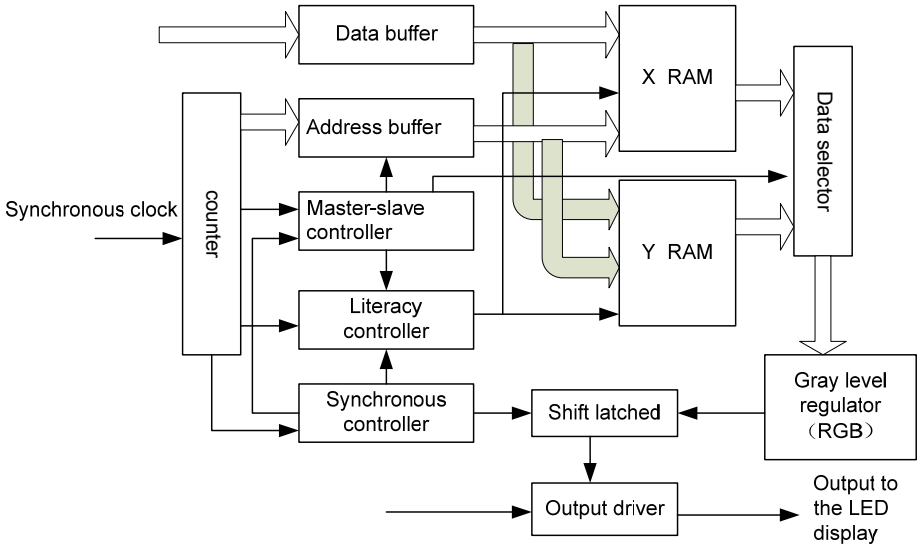

Figure 5. Principle diagram of scanning circuits

As followed is the simulation waveform diagram of read/write SRAM controll, in the picture, we can see, add_write [16:0] and add_read [16:0] are the read/write address of the memory unit which is to be operated; cs1 and cs2 are the chip select signals of SRAM1 and SRAM2; oe1 and oe2 are their read control signals; we1 and we2 are the write control signals.

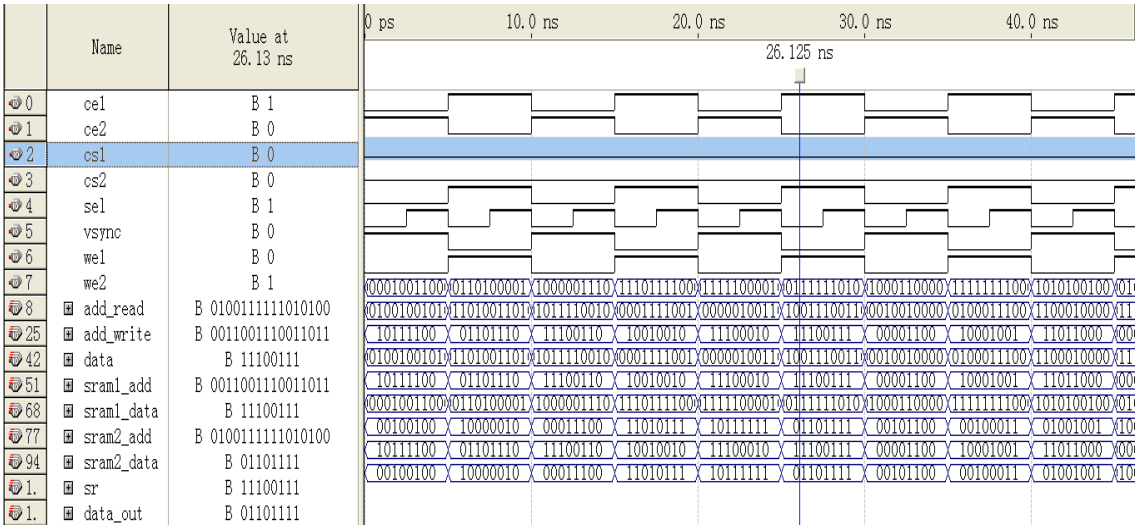

Figure 6. the simulation waveform diagram of read/write SRAM control

4. Conclusion

According to the above system design of hardware structure and simulation, the organic combination of the PC and embedded control is realized. And the display of data information on the LED display screen and the communication with Lower PC is complete and realized. The embedded control unit realizes the receiving and storage of data, the display mode transformation of data and image output, and achieves effective control of LED screen.

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