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New voltage and temperature scalable gate delay model applied to a 14nm technology

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ABSTRACT

The following work shows an innovative approach to model the timing of standard cells. By using mathematical models instead of the classical SPICE-based characterization, a high amount of CPU (Central Processing Unit) cores is saved and less amount of data is stored. In the present work, characterization of cells of a standard cell library is done in an hour whereas it is done in 650 hours with the classical method. Also, a method for validating and verification of the precision of the modelled data is presented by comparing them on a implemented circuit. The output of implementations shows less than 3% of error between the two methods.

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1. INTRODUCTION

The library of standard cells is a term used to define a group of logic blocks like INVERTER, AND, OR, etc. The power and timing specifications for each of these logic cells are also included in this library [1]. The standard cell library is used for its advantages on the circuit design like reducing the product development's time, robustness and the flexibility added to the design. Design specifications should be considered in the development of a standard cell library like timing and power, constraints, area etc it can be oriented either for high performance to be used in rapid designs or for high density to be used in low power circuits. To reach a good and optimized implementation of RTL, a well designed standard cell library is required [2-6].

Characterizing a standard cell is an important part in the development phase and must be reliable [7, 8]. By running simulations on each single cell of the library in various corners, which are also called PVTs (process, voltage, temperature), different metrics (power consumption, targets of timing and leakage) are determined. The outputs of these simulations are reported in a liberty file. It will also include the specifications of each cell as well the information on the simulation's configuration and cells characteristics like: characterization conditions details (process, temperature, voltage), units cell height, input/output pins, area etc [6]. Zimpeck et Al. evaluates the impacts of PVTs variation on timing [9].

The data in the liberty files is organized under a matrix format also called LUT (Look Up Table). This is explained by the fact that each data type, which is generally calculated by performing spice simulation on cells, depends on other parameters. If we take the transition time to illustrate that, it is determined regarding various values of load capacitance of the cell's output (represented by index 2 in Figure 1) and the slew of the cell's input (the transition time of transition of the input which is represented by index 2 in Figure 1) as shown in Figure 1. The values represented in this LUT are the outputs of the spice simulations.

```
operating_conditions (ssgip_cworstip_max_0p58v_85c) {
default_operating_conditions : ssgip_cworstip_max_0p58v_85c;
fall_transition (delay_template) {
index_1(        0.00225333 0.005222 0.011159 0.022663 0.046041 0.092797 0.186309 0.373333);
index_2(       0.000152169 0.002986 0.008654 0.019636 0.041953 0.086587 0.175857 0.354395);
values( \
                  0.0194722 0.044925 0.079879 0.157353 0.323258 0.657697  1.32594   2.6651
                  0.0194704  0.04491 0.079872  0.15752 0.323166 0.657898  1.32647  2.66147
                  0.0194533 0.044907 0.079873 0.157484 0.323183 0.657915  1.32657  2.66515
                  0.0194866 0.044919 0.079829 0.157426 0.322787 0.657852  1.32577  2.66432
                  0.0195255 0.044945 0.079837  0.15746 0.323258 0.657373   1.3277   2.6649
                  0.0195839  0.04499 0.079816 0.157439 0.322906 0.657181   1.3274   2.6634
                  0.0197445 0.045085 0.079932 0.157529  0.32275 0.657479  1.32749   2.6641
                  0.0201764 0.045281 0.079982 0.157388 0.322829 0.657588  1.32684  2.66321
            );
}
```

Figure 1. LUT table representing timing from a liberty file

The more PVTs are simulated the more resources and characterization time is needed especially with the continuous scaling of the technology. In the present case study, in order to characterize a library of standard cells containing 800 cells, 650 hours are required. This implies the use of a big amount of CPUs and storage area space that increases the costs in this part of the design flow.

A number of characterization methodologies were proposed by many researchers in the aim of increasing the precision of the models ignoring the large simulation time [10-13]. In his paper J. Jianhua et al state that the choice of input parametes (index1, index2) in the timing LUT impacts the accuracy [10]. While A. Imár et al presents timing model to improve modelisation of delay-temperature function [12]. In his work, S. Miryala et Al. present a novel model to determine the delay. However, the model is based on an inverter. This method allows to save more than half (51%) of SPICE simulations time when characterizing a logic cell without affecting the accuracy [13]. In this work the simulation's time is still consequent. In addition to that, it has been validated on one cell only, an INVERTER: results achieved on this cell may be less accurate for other cells of the standard cell library. More recently, L. Yu et al introduce a statistical method of timing characterization that reduces simulation time by 15x. The results are compared to a classical stastical method and achives more than 4% average error for all cells in the library. While this result is interesting, it seems quite high especially that tests on full circuit haven't been done [15]. Other works proposed other methodologies of standard cells characterization but they still require a high amount of running time [16-18].

In the present paper, a novel method to calculate gate timing is introduced in order to decrease significantly time and CPU resources. It relies on mathematical modelling. Rather than generating liberty files by simulating many corners, only a few of them are characterized and based on the models developed, any other corner can be generated in a short time: l hour instead of 650 hours for the classical caracterization. It represents the time of the execution of the JAVA script and the print of the results. These equations represent the physical variation of each parameter in the liberty file (internal power, timing etc). The models developed vary only with voltage and temperature. Different equations are determined for the different parameters in the liberty to obtain the best accuracy. The main target of this work is to reduce significantly the time need to generate a liberty file while lowering the costs at this stage of the standard cell design flow. Also, the accuracy achieved is less than 3% on a full circuit.

In litterature, models used impacts the precision of the characterized file. This methodology is CMOS technology independent as the physical variation of delay is not supposed to vary with technology.However, the results presented in this paper are results of simulations done on cells developped on a finFET 14nm node. The finFET transitor has been introduced as an alternative to the planar CMOS in order to fulfill Moore's law and has the advantage of minimizing the impact of short channel effects [19-21].

This work is structured as follows. In part 2, the flow used and its specifications are described in details. The last parts of this section are dedicated to the presentation and the explanation of the timing models developed including the models for the constraints of timing for sequential cells. In part 3, the methodologies used to do the comparison between a modelled liberty file and a characterized one are detailed and results are presented. Liberty files are also validated at circuit level by performing an STA (Static Timing Analysis) on an implementation of an ARM-Cortex A9.

2. RESEARCH METHOD

2.1. Proposed Timing Modelling Method

In this part, the fast characterization method developed in order to generate liberty files with a high precision is detailed. It uses initial files that have been characterized using Spice simulations, in various conditions. Each different PVT condition is also called a corner. In this work, the models are developed in a given process, a corner will designate any change of temperature or voltage.

This method uses liberty files generated by characterization in order to generate new corners by interpolation using the curve fitting methodology. Curve fitting is a technique for analysing an experimental curve, consisting of constructing a curve from mathematical functions and adjusting the parameters of these functions to approximate the measured curve. However, finding the most suitable fitting parameters is the main issue of this method. Indeed, this can lead to very complicated mathematical equations.

Parameters' dependency with the voltage and the temperature in the .lib are represented with mathematical equations. In order to avoid using very complicated mathematical models, a minimum of 8 eight characterized corners are needed to achieve a good accuracy. These initial corners are called input corners. But in order to develop the models, additional corners have been generated even if only eight of them are used to determine the parameters of models and to generate the interpolated files. The library used in this work contains a total of 800 cells.

2.2. Specifications

As previously explained, the initial PVTs used in the extraction of models parameters affects the accuracy. They have to be chosen carefully. For every single cell, eight liberty files corresponding to eight PVTs are generated by characterization. These 8 corners constitute an input to generate the results in the coming sections below: Two temperatures and four voltages. The structure of the input files should be identical and the different input corners must be chosen so that they cover the platform range of the technology node used. For each different technology, a preliminary study is done to determine the corners that give the least errors in the generated liberty files.

For the temperature, the minimal value and the maximal value defined in specifications of the technology node are taken in order to cover the whole platform range. For the voltages, the minimum value and the maximum value are also taken. The two remaining voltages are selected so that the delays differences of each successive voltages are the same. Figure 2 shows the curve of delay regarding the voltage of an Inverter cell where Δ_{t1}, Δ_{t2} and Δ_{t3} represents the delays differences. Referring to this figure, Δ_{t1}, Δ_{t2} and Δ_{t3} should be equal. Another important specification is that same conditions should be respected in the characterization of cells for all the input corners which means liberty files should have the same file structure, the same number of pins, tool versions used should be the same etc.

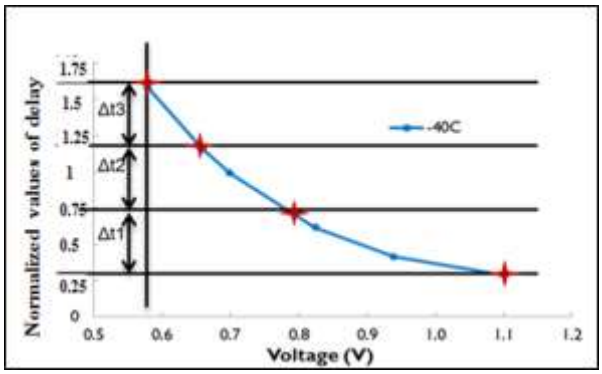


Figure 2. An Inverter delay dependency with voltage

2.3. Scaling Flow Developed

The scaling flow developed is presented in Figure 3. The cells of the library are handled separately. Liberate from Cadence Design Systems is the characterizing tool that was used to generate the input corners. The first step consists on parsing characterized .lib files in order to retrieve parameters of timing model. Once these parameters are calculated according to the mathematical equations, the interpolation of any new corner's can be done. Due to the high amount of data contained in the liberty files, automation of these different phases was mandatory, a JAVA script has been developed in order to handle all these operations.

The script checks also the consistency of the generated files and validates that the output liberty files and the input ones have the same structure. The targeted corners that the user wants to generate are given as an input of the script (Figure 3).

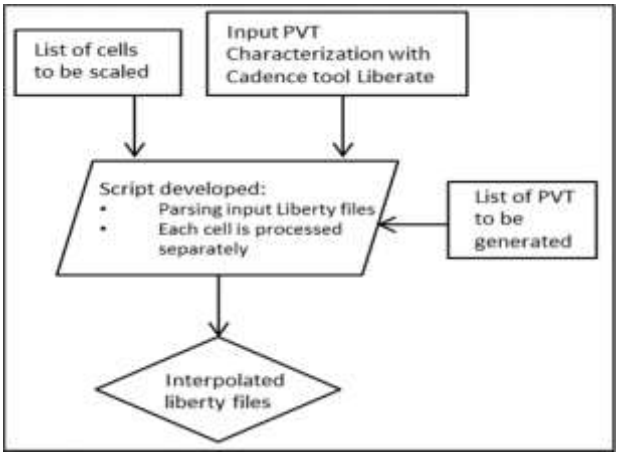


Figure 3. Flow of characterization

In the optic of increasing the precision of the scaled liberty files, fitting parameters are calculated for each set of values in the tables of liberty for each metric. To illustrate that, the timing LUT of 64 values is taken as an example in Figure 4: each fitting parameter will come in a matrix of 64 values although it is the same equation model. Once they are known, fitting parameters will be stored in order to generate new corners. The delay can be calculated by replacing the wanted PVT values (voltage and temperature) in the timing model. It has to be noted that while these parameters are dependent on the cell, the slew and the load, they are independent of the PVT.

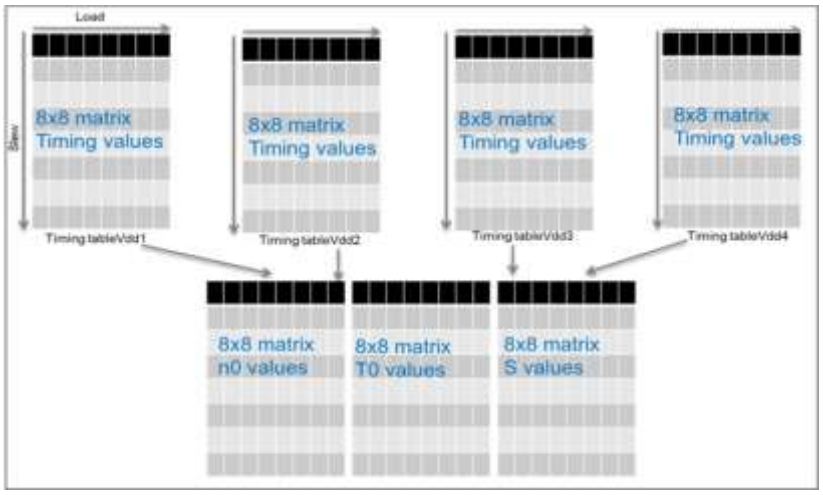


Figure 4. Model of fitting Parameters extraction

Characterizing the timing of a cell is not only calculating its delay but also determining the cell rise and fall transition, the flip flops constraints, the tri-state enable and disable times. In the next part of this paper, the developed equations for delay and rise and fall transitions will be detailed. The same model is applied to these two types of timing as their respective curves follow the same tendency. So the choice here is to only give the example of the delay. In addition to that, the equations developed for flip flops' constraints are also detailed in the next section.

2.4. Developed Timing Model

At first and in order to define the mathematical equations, a sample of each cell category (INVERTER, flip flops, NAND gates ...), is taken to validate the model. Equations are then integrated into the automated script to be deployed and tested on rest of cells of the library.

2.4.1. Model for Voltage Variation

Delay is defined as the time needed for the voltage of the output signal, to rise or to fall, to the input threshold point defined after the input signal voltage has fallen or raised to the output threshold point set [22]. Figure 5 illustrates the delay calculation. For a same cell, many delays are determined corresponding to all the input-output paths.

While Figure 6 shows the relationship between the supply voltage and the logic delay, illustrated by the most critical path of a multiplier circuit in 65 nm technology [23]. Figure 7-a shows the delay's dependency with voltage for different temperatures. Data presented in this curve are obtained from characterization in 14nm technology. In both cases, the results of the simulations show that the delay decreases exponentially by increasing the voltage.

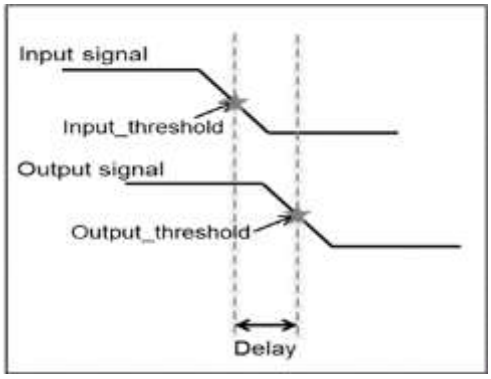


Figure 5. Delay calculation

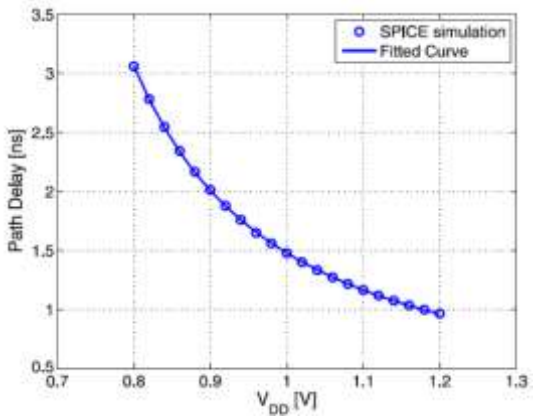


Figure 6. Relationship between the supply voltage and the logic delay in 65 nm technology [23]

The simulations results show that delay decreases with a nonlinear dependence while increasing the voltage. The physical delay dependency with voltage is represented by (1) [24]:

$$t_{gate} = \frac{V_{DD}}{b(V_{DD}-V_t)^a} \quad (1)$$

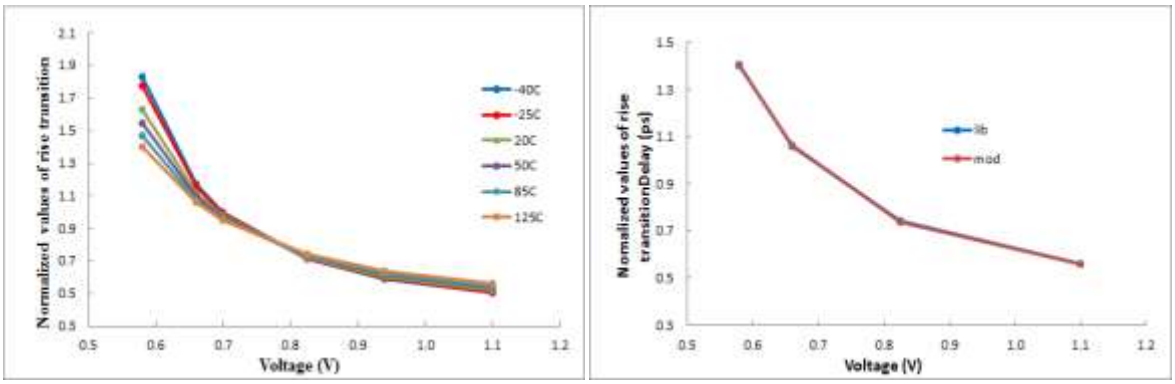
where *a* and *b* are adjustment parameters specific to the logic gate and V_t is the threshold voltage.

Initially, (1) was used to model the delay, but for the sake of precision, modifications were made to this model. On this basis, the variation of the delay with the voltage was modelled by the following (2):

$$T_d = T_0 + \frac{S}{V^n} \quad (2)$$

Where T_d represents the delay, *V* represents the voltage, and T_0, *S* and n are constants that refer to the fitting parameters that will be determined from timing data of input liberty files.

The equation of the voltage model has been developed for the same temperature, the choice can be the minimum temperature or the maximum one. In this work, it was done at T_{min} (the minimal temperature). In Figure 7-b, comparison of delay dependency with voltage from characterized data versus delay of the same gates of data calculated with the developed model at a temperature of -40°C, is shown. The two curves (the modelled curve and the simulated one) match quite well.



(a) (b)

Figure 7. a) Variation of the delay regarding the voltage and for various temperatures; b) Example of the comparison of characterized delay liberty vs modelled data at 125°C – INVERTER cell

2.4.2. Model of Temperature

The delay dependency with the temperature is linear as shown in Figure 8a. These data used to draw these curves are obtained from supplementary corners that have been characterized. These PVTs are not included in the generation of the interpolated liberty files. This linear dependency is represented by a linear function added to the voltage model to reflect the variation with temperature (3):

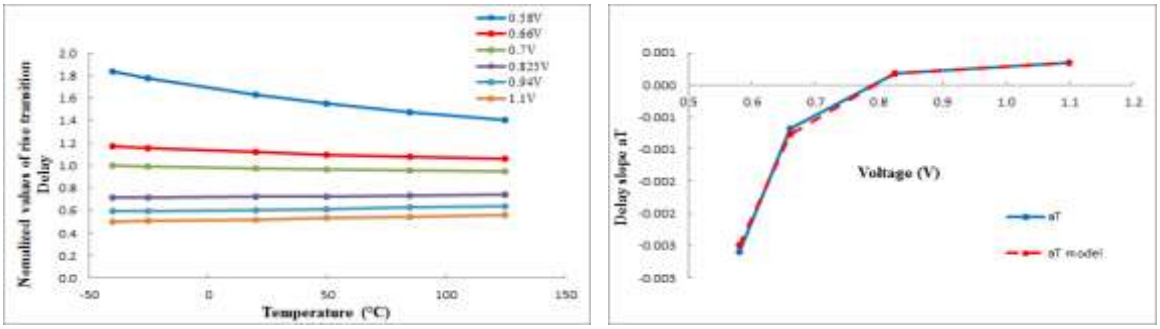
$$T_d = T_0 + \frac{S}{V^n} + a_T(T - T_{min}) \quad (3)$$

Where a_T is the slope, T_{min} is the minimal temperature allowed by the process.

The variation of a_T, the slope of temperature equation with voltage is shown in Figure 8-b. This dependency is modelled by an exponential equation as follow (4):

$$a_T = K - e^{\alpha * V + \beta} \quad (4)$$

Where K, α, β are the fitting parameters calculated by the automated script.



(a) (b)

Figure 8. a) Example of the dependence of the delay with temperature for various values of voltage; b) Variation of the slope of delay model with temperature of modelled data vs characterized data

2.5. Flip Flop's Constraints Model Equation

Flip flops have additional parameters that have to be characterized. More than the delay of the cell and transition times, timing constraints are key metrics that have to be calculated. It consists of the setup, the hold, the recovery and the removal times.

The setup time corresponds to the minimum time the data needs to stay unchanged before the clock's active edge. All transitions that occurs while the setup time, can capture a false value. The hold time refers to the minimum amount of time the data must remain unchanged after the clock's active edge. All transitions occurring while hold time will not give reliable latched data [22].

The setup and hold time are reported in liberty files under the format of matrixes of 4x4 varying with the data slew transition (slew1) and the clock slew transition (slew2). Modelling the setup and hold timing have been particularly difficult and challenging because the variation of these liberty file's metrics doesn't follow the same evolution regarding the voltage as illustrated in Figure 9. In these Figures (Figure 9-a, Figure 9-b, Figure 9-c), three the examples of variation of setup values with voltage are shown for two different temperatures. Nevertheless, developing an appropriate model for these metrics is mandatory because setup and hold times are the longest data to be simulated using spice characterization.

For this purpose, two parameters have been added in the equation of the model: the slew 1 and slew 2. The setup time is modelled regarding the slew1 and the slew2, then regarding the voltage and temperature. Figure 10 illustrates the dependence of setup time regarding slew1 in Figure 10-a and regarding slew 2 in Figure 10-b based on characterized data. The setup time has the same progression with slew1 (increases with slew1) and with slew 2 (decreases with slew2). A polynomial model fits quite well these tendencies. The adopted equation for this model is as follow:

$$T_{su} = a_{2s1} * {S_1}^2 + a_{1s1} * S_1 + a_{2s2} * {S_2}^2 + a_{1s2} * S_2 + b \quad (5)$$

Where T_{su} is the setup time, *S1* represents slew1 while *S2* represents slew2 and a_{2s1}, a_{1s1}, a_{2s2}, a_{1s2} and b represent parameters to be calculated by the script developed.

The following parameters' a_{2s1}, a_{1s1}, a_{2s2}, a_{1s2} and b dependencies regarding the voltage are modelled respectively with a polynomial and power equation as shown in the below equations (6-10):

$$a_{2s1} = b_{22} * V^2 + b_{21} * V + b_{20} \quad (6)$$

$$a_{1s1} = b_{12} * V^2 + b_{11} * V + b_{10} \quad (7)$$

$$a_{2s2} = b'_{22} * V^2 + b'_{21} * V + b'_{20} \quad (8)$$

$$a_{1s2} = b'_{12} * V^2 + b'_{11} * V + b'_{10} \quad (9)$$

$$b = b_0 + {S}/{V^n} \quad (10)$$

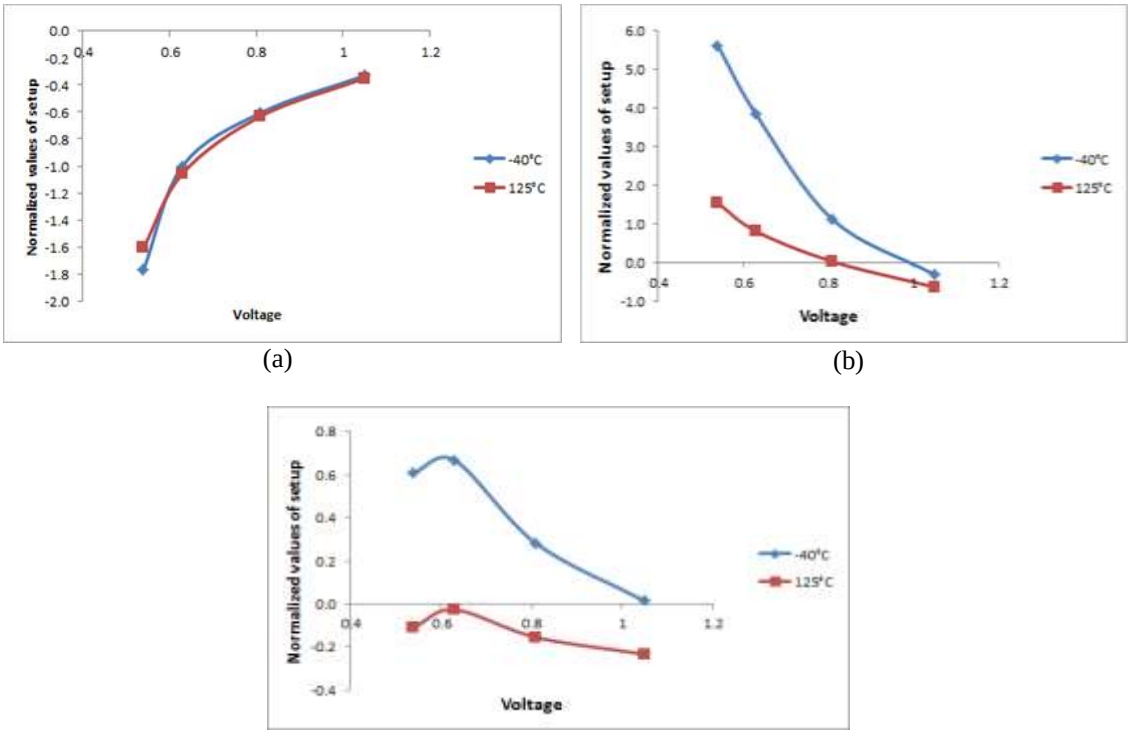
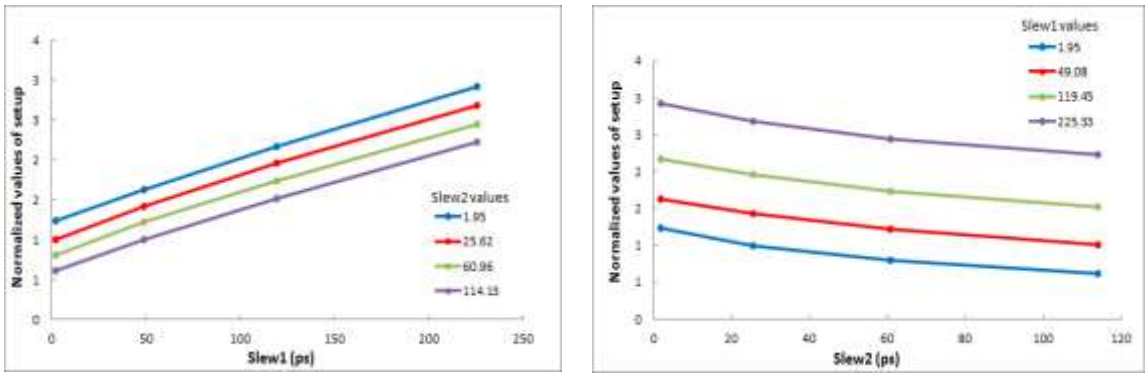


Figure 9. Variation of setup time with voltage



(a) (b)

Figure 10: (a) Variation of setup time regardind slew1, (b) Variation of setup time regarding slew2

3. RESULTS AND DISCUSSION

3.1. Cell's Level Validation

Before validating the developed models on a circuit level, timing models are first validate at cell level. After the fitting parameters are calculated using the developed tool, the same input PVTs are regenerated with interpolation method. Each corresponding value of timing of characterized liberty file and interpolated one are compared for all the standard cells of the library according to a predefined errors threshold. Errors that are checked are the absolute and the relative errors. Absolute error is defined as the difference between the values that are examined (10). Relative error is defined as the ratio of the previous determined error (absolute error) and the characterized value (11).

$$err_{absolute} = (V_{scal} - V_{char}) \quad (10)$$

$$err_{relative} = err_{absolute}/V_{char} \quad (11)$$

where Vscal represents the scaled value and Vcharac represents the characterized value.

The main purpose of introducing the absolute error is to ignore very high percentages in relative errors. These are mainely due to errors on the very small value in timings. The verification at cell level is automatized and hence is part of the characterization flow. The timing values of each cell have to meet the previous requirements in order to be scalable ("PASS"). The developed tool generates a report with the list of "PASS" and "FAIL" cells and only liberty files of cells that have a "PASS" status are interpolated.

Table 1 shows an example of the transition time error of the interpolated .lib compared to the .lib characterized for a DFFQN flip flop for a voltage of 0.58V and a temperature of -40 °C. The largest errors detected relate to the smallest values of the transition time corresponding to the first column of the Table 1. The tolerance of the absolute error (1ps in this case) has not been applied yet in the results reported in this table. After applying the absolute error, these errors will be 0%. For the rest of the table's values, the overall errors are less than 2%. This proves that the model developed for timing describe and predict data very well.

Table 1. Error of fall transition DFFQN for corner -40°C, 0,58V

-4,2%	-1,9%	-1,0%	-0,2%	-0,3%	0,0%	-0,5%	-0,4%
-4,2%	-1,9%	-1,0%	-0,2%	-0,3%	0,0%	-0,4%	-0,5%
-4,1%	-1,9%	-1,0%	-0,3%	-0,4%	0,0%	-0,4%	-0,4%
-4,2%	-1,9%	-1,0%	-0,2%	-0,3%	0,0%	-0,5%	-0,4%
-4,2%	-1,9%	-1,0%	-0,2%	-0,3%	0,1%	-0,4%	-0,4%
-4,2%	-2,0%	-1,0%	-0,2%	-0,3%	-0,1%	-0,4%	-0,4%
-4,1%	-1,9%	-0,5%	-0,2%	-0,4%	0,0%	-0,4%	-0,4%

Another validation is made at the cell level for an inverting cell and a buffer only. This validation is a correlation between an Hspice simulation and a timing analysis using the Prime Time tool based on interpolation data. Prime Time is a static timing analysis tool from Synopsys. The circuits compared are critical circuits based on a given cell with different fanouts, a buffer in the first case and an Inverter in the second. The choice to do this validation test on only two cells is due to the fact that doing this comparison on all cells would take a considerable time.

Tables 2, 3, 4 and 5 show the correlation results for the two cells used for two intermediate corners which are: (0.7V; 85 °C) and (0.9V; -25 °C) . In both cases, the difference of errors (Diff errors in the table) of the interpolated data in comparison with the characterized data are less than 2% for the worst cases. This proves that the model developed for timing is precise enough to be used at circuit level.

Table 2. Correlation between Hspice and PT simulation for a circuit based on a Buffer for a corner SS_0p70V_85 °C

	Characterized Liberty file				Modelled Liberty file		
Circuit	PT	HSPICE	Error	Diff errors	PT	HSPICE	Error
BUF_X8N_10_2_0	0,99	1,00	1,26%	-0,22%	0,99	1,00	1,49%
BUF_X8N_10_2_1	0,98	1,00	1,78%	-0,21%	0,98	1,00	1,99%
BUF_X8N_10_2_5	0,98	1,00	1,86%	-0,21%	0,98	1,00	2,07%
BUF_X8N_10_2_10	0,98	1,00	1,65%	-0,21%	0,98	1,00	1,86%
BUF_X8N_10_5_0	0,95	1,00	5,44%	-0,21%	0,94	1,00	5,65%
BUF_X8N_10_5_1	0,96	1,00	4,39%	-0,21%	0,95	1,00	4,60%
BUF_X8N_10_5_5	0,94	1,00	5,87%	-0,21%	0,94	1,00	6,08%
BUF_X8N_10_5_10	0,95	1,00	4,92%	-0,21%	0,95	1,00	5,13%
BUF_X8N_10_10_0	0,99	1,00	1,43%	-0,09%	0,98	1,00	1,52%
BUF_X8N_10_10_1	0,98	1,00	1,63%	-0,09%	0,98	1,00	1,72%
BUF_X8N_10_10_5	0,98	1,00	2,05%	-0,10%	0,98	1,00	2,15%
BUF_X8N_10_10_10	0,98	1,00	2,06%	-0,09%	0,98	1,00	2,15%

Table 3. Correlation between Hspice and PT simulation for a circuit based on a Buffer for a corner SS 0p90V_-25°C

	Characterized Liberty file				Modelled Liberty file		
Circuit	PT	HSPICE	error	Diff errors	PT	HSPICE	error
BUF_X8N_10_2_0	0,99	1,00	0,55%	-1,36%	0,98	1,00	1,91%
BUF_X8N_10_2_1	0,99	1,00	1,13%	-1,32%	0,98	1,00	2,46%
BUF_X8N_10_2_5	0,99	1,00	1,16%	-1,30%	0,98	1,00	2,46%
BUF_X8N_10_2_10	0,99	1,00	0,98%	-1,34%	0,98	1,00	2,32%
BUF_X8N_10_5_0	0,95	1,00	4,88%	-1,39%	0,94	1,00	6,27%
BUF_X8N_10_5_1	0,97	1,00	3,39%	-1,41%	0,95	1,00	4,81%
BUF_X8N_10_5_5	0,95	1,00	5,49%	-1,38%	0,93	1,00	6,87%
BUF_X8N_10_5_10	0,96	1,00	4,17%	-1,40%	0,94	1,00	5,57%
BUF_X8N_10_10_0	1,01	1,00	-0,84%	0,27%	0,99	1,00	0,56%
BUF_X8N_10_10_1	1,00	1,00	-0,49%	-0,42%	0,99	1,00	0,91%
BUF_X8N__10_10_5	1,00	1,00	-0,35%	-0,68%	0,99	1,00	1,02%
BUF_X8N_10_10_10	1,00	1,00	-0,43%	-0,53%	0,99	1,00	0,96%

Table 4. Correlation between Hspice and PT simulation for a circuit based on an INVERTER for a corner SS_0p70V_85°C

	Characterized Liberty file				Modelled Liberty file		
Circuit	PT	HSPICE	error	Diff errors	PT	HSPICE	Error
INV_X8N_10_2_0	0,9707	1,00	2,93%	0,03%	0,9710	1,00	2,90%
INV_X8N_10_2_1	0,9982	1,00	0,18%	0,03%	0,9985	1,00	0,15%
INV_X8N_10_2_5	1,0111	1,00	-1,11%	-0,01%	1,0112	1,00	-1,12%
INV_X8N_10_2_10	1,0152	1,00	-1,52%	-0,05%	1,0156	1,00	-1,56%
INV_X8N_10_5_0	0,9299	1,00	7,01%	0,19%	0,9318	1,00	6,82%
INV_X8N_10_5_1	0,9781	1,00	2,19%	0,32%	0,9813	1,00	1,87%
INV_X8N_10_5_5	1,0146	1,00	-1,46%	-0,26%	1,0172	1,00	-1,72%
INV_X8N_10_5_10	1,0419	1,00	-4,19%	-0,28%	1,0447	1,00	-4,47%
INV_X8N_10_10_0	0,9010	1,00	9,90%	-0,07%	0,9003	1,00	9,97%
INV_X8N_10_10_1	0,9337	1,00	6,63%	0,06%	0,9342	1,00	6,58%
INV_X8N_10_10_5	0,9816	1,00	1,84%	-0,24%	0,9792	1,00	2,08%
INV_X8N_10_10_10	1,0247	1,00	-2,47%	0,10%	1,0238	1,00	-2,38%

Table 5. Correlation between Hspice and PT simulation for a circuit based on an INVERTER for a corner SS 0p90V_m25 °C

	Characterized Liberty file				Modelled Liberty file		
Circuit	PT	HSPICE	error	Diff errors	PT	HSPICE	error
INV_X8N_10_2_0	0,994	1,00	0,57%	-0,72%	0,987	1,00	1,29%
INV_X8N_10_2_1	1,023	1,00	-2,32%	0,60%	1,017	1,00	-1,72%
INV_X8N_10_2_5	1,035	1,00	-3,51%	0,54%	1,030	1,00	-2,96%
INV_X8N_10_2_10	1,036	1,00	-3,63%	0,68%	1,030	1,00	-2,95%
INV_X8N_10_5_0	0,964	1,00	3,59%	-1,04%	0,954	1,00	4,64%
INV_X8N_10_5_1	1,019	1,00	-1,85%	1,24%	1,006	1,00	-0,61%
INV_X8N_10_5_5	1,054	1,00	-5,43%	1,18%	1,043	1,00	-4,26%
INV_X8N_10_5_10	1,078	1,00	-7,82%	1,22%	1,066	1,00	-6,60%
INV_X8N_10_10_0	0,926	1,00	7,39%	-1,37%	0,912	1,00	8,76%
INV_X8N_10_10_1	0,967	1,00	3,32%	-1,29%	0,954	1,00	4,61%
INV_X8N_10_10_5	1,020	1,00	-2,02%	1,56%	1,005	1,00	-0,46%
INV_X8N_10_10_10	1,066	1,00	-6,56%	1,59%	1,050	1,00	-4,97%

3.2. Validating Scaled Liberty Files at Circuit Level

The second step of the validation of the scaled liberty files is at circuit level. The choice here has been made on an ARM-Cortex A9, which is a single core processor that targets low power designs [25]. This check has been done on intermediate corners, which mean corners that have not been used in the determination of fitting parameters. A total of three PVTs have been compared. The choice here is to perform the implementation with the characterized liberty files as this step is liberty file dependent. This single implementation will be reused to make two different STA: one with the characterized liberty file and the other one with the interpolated liberty file. In this case, the comparison is made at the same conditions for the same final circuit. STA is a method of simulation in order to calculate the timing of a digital circuit using liberty. This avoids to simulate the full circuit. It also determine the maximum frequency that can be acieved while checking all timing violation on critical paths Table 6 shows the comparison between the results of sta using the two liberty files. The worst case's error does not exceed 3% for the achieved frequency. This results prove the accuracy of the developed model.

However, under real conditions of use of the modeled .lib, the implementation will not be imposed. In the following comparison, the two different liberty files were given to the STA tool. This resulted in two different implementations for each corner compared. Table 7 shows the results of these STA comparisons of liberty from characterization and interpolation for different intermediate corners. The results show up to 7.5% error. But looking more closely at the results in Table 7, it turns out that in some corners the frequency achieved with modelled liberty files is better than those obtained with characterized liberty files. In the best case the frequency has been improved by 7.5%.

Table 6. Results of STA of Scaled .lib files Vs Characterized .lib files with the same implementation

Liberty file corner	Achieved Frequency (GHz)	Error (%)
Characterized .lib (0p59V; 40°C)	0.5056	-2.66
Scaled .lib (0p59V; 40°C)	0.4921	
Characterized .lib (0p70V; 85°C)	0.5385	0.65
Scaled .lib (0p70V; 85°C)	0.5420	
Characterized .lib (0p90V; 85°C)	0.7616	1.47
Scaled .lib (0p90V; 85°C)	0.7728	

Table 7. Results of STA of Scaled .lib files Vs Characterized .lib files with different implementation

Liberty file corner	Achieved Frequency (GHz)	Error (%)
Characterized .lib (0p59V; 40°C)	0.5056	-0.5
Scaled .lib (0p59V; 40°C)	0.5033	
Characterized .lib (0p59V; 85°C)	0.5086	-0.8
Scaled .lib (0p59V; 85°C)	0.5045	
Characterized .lib (0p70V; 85°C)	0.5385	-1.1
Scaled .lib (0p70V; 85°C)	0.5328	
Characterized .lib (0p70V; m25°C)	0.5299	-1.2
Scaled .lib (0p70V; m25°C)	0.5238	
Characterized .lib (0p90V; 85°C)	0.7616	3.1
Scaled .lib (0p90V; 85°C)	0.7849	
Characterized .lib (0p90V; m25°C)	0.7886	7.5
Scaled .lib (0p90V; m25°C)	0.8475	

4. CONCLUSION

This paper presents a fast approach of generation of liberty files of a standard cell library based on mathematical interpolation. This methodology can be used to save time and achieve results with a high precision. The gain in time is considerable, it takes 1 hour to generate any new corner instead of hundreds of hours. It has been tested in real design in the objective of validating its accuracy leading in some cases to achieving a better frequency of the circuit. Still, solutions and models have to be created and deployed for the other metrics in the liberty file as for now only timing is scaled. Also the validation of this approach on other technology nodes should be done.

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