

## Regular clocking scheme based design of cost-efficient comparator in QCA

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### ABSTRACT

Quantum-dot cellular automata (QCA) gained a notable attraction in the emerging nanotechnology to get the better of power consumption, density, nano-scale design, the performance of the present CMOS technology. Many designs had been proposed in QCA for an arithmetic circuit like adder, divider, parity checker and comparator etc. Most of the designs have been facing the challenges of cost efficiency, power dissipation, device density etc. However, consideration of design automation, underlying clocking layout and integration of the sub modules are the most important which has a direct impact on the fabrication of the design. This work proposed a novel cost effective and power aware comparator design, which is an essential segment in central processing unit (CPU). The noticeable novelty of the design was the use of underlying regular clocking scheme. A new scalable, regular clocking scheme has been utilized in the coplanar design of the comparator which enables regular or uniform cell layout of QCA circuit. It also exhibited the significant improvement over existing counterparts having irregular clocking in terms of area and latency. QCADesigner was used to test and verify the functionality of the circuit and by using QCAPro the power dissipation has been analyzed.

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## 1. INTRODUCTION

Several technologies, such as carbon nanotube based field effect transistor, resonant tunneling diode and quantum-dot cellular automata (QCA) have been emerged to explain the complications CMOS technology as predicted in the proximate past [1, 2]. Among them, QCA technology furnish a favourable one to beat the limits of CMOS [3, 4]. It offers a new paradigm introduced in [5] for faster computation [6], ultra low power consuming [7, 8], work in nano-scale and information propagation by the properly of arranging cells together in place of transistors as in case of CMOS technology [9-11]. QCA does not supply voltage levels to generate logic states rather it uses an electron pair for the same [5, 12]. A QCA cell is made of four number of quantum-dots, where the diagonal placement of two electrons defines the polarization state of the cell, either -1 (logic 0) or +1 (logic 1).

The fundamental units of QCA are shown in Figure 1. Primary logic primitives, a majority gate and an inverter are found to be used in emerging nanotechnology based QCA [13-16]. Any QCA design can be realized using these two only taking with QCA wires along [17]. Several techniques (coplanar and multi-layer) for crossover structure can be realized. There are four phases of QCA clock: i. Switch (Clock 1) ii. Hold (Clock 2) iii. Release (Clock 3) and iv. Relax (Clock 4). The concept of QCA clocking is briefly described in details in [12, 18, 19].

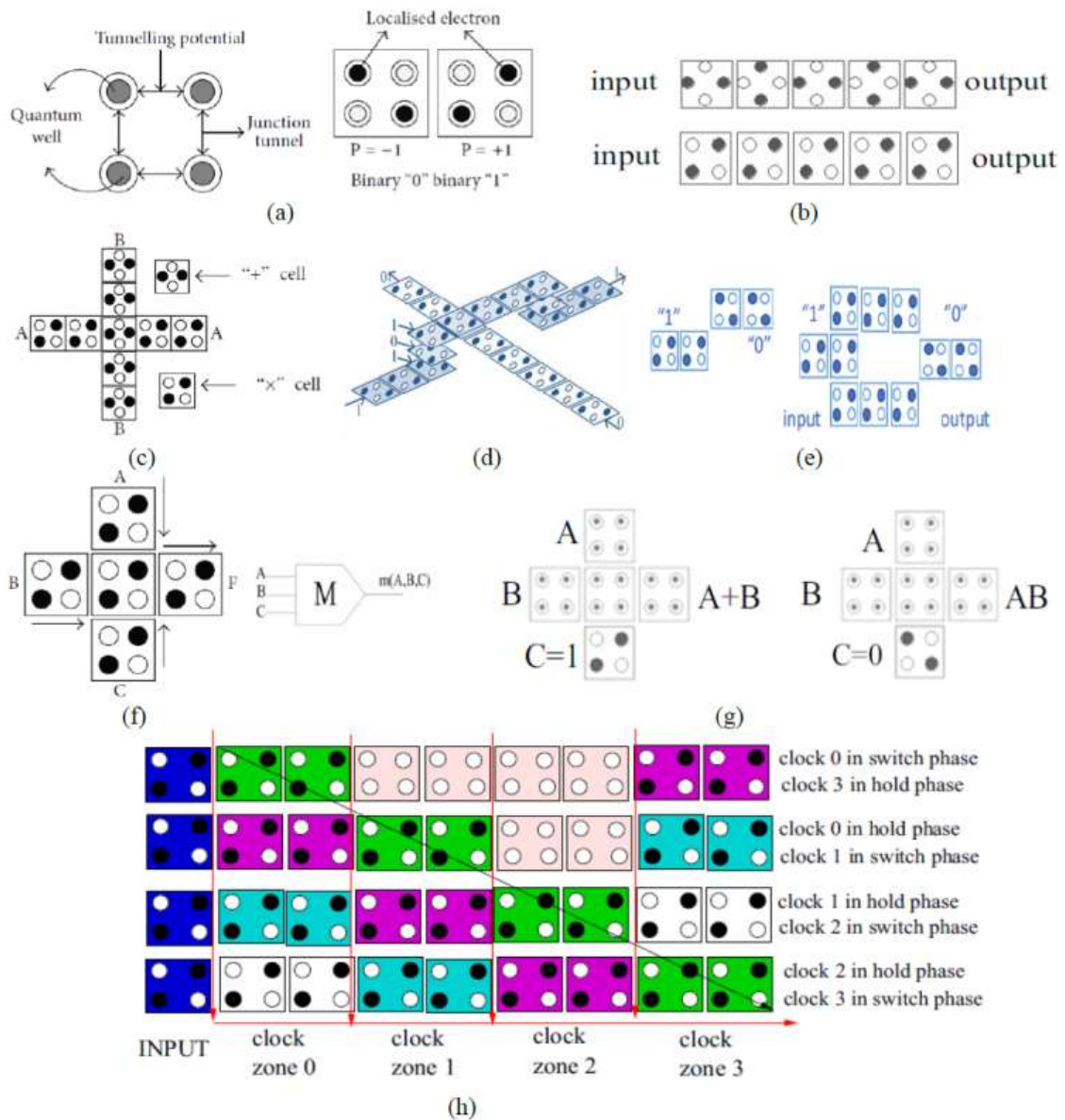


Figure 1. Basic structural components of QCA

In this regard, QCA has received a numerous attention for the past few years in the logic design specially towards arithmetic logic such as adders [20, 21], multiplexer [22-25], XOR [26-28], parity checker [29-31], comparators [32-40]. Among them, comparators have received a considerable interest as it is having an important role in the development of central processing unit (CPU) and also widely studied. Additionally, the area, speed and power consumption are the parameters mostly used in performance analysis of a circuit [41-43]. An area-delay cost estimation functions was proposed in [44] which was further revisited for appropriate QCA metrics in [45].

The significance of regular clocking scheme is unavoidable in the fabrication of logic circuit in QCA technology. The concept was initially reported in [46-48] but fails to prove its efficiency and completeness. Initially, a two dimensional clocking scheme is formally proposed but it retain the issue in realizing feedback loop [49]. The clocking in [50] have addressed the issue with an implementation approach using multilayer crossover. But, multi-layer QCA circuit did not get any significance due to its fabrication complexity. Alter-natively, a coplanar wire crossing based design with three-dimensional information flow was proposed in [51]. However, the wire crossing increases in the underlying clocking circuit due to the complex layout for clock zone 3 in [51]. These points have a notable impact on the buildability of the circuit and demands a flexible, scalable and robust clocking scheme with reduced complexity in fabrication.

On the other hand, several synthesis methodologies in QCA layout for comparator have been explored. Some of them are not robust [35, 40] and some of them are multi-layer based design [33, 34, 37] making them practically difficult to fabricate. A coplanar crossover based design layout is proposed in [32, 36, 38]. However, to the best of knowledge of the authors, no comparator has been noticed till date to have designed inculcating underlying regular clocking. Moreover, cost efficiency and power awareness of the design is important along with regular clocking for a complete real time fabrication [45, 42].

The above discussed issues, point to the concern of realistic design of digital circuit in QCA is still in infancy and needs proper research in that direction. Hence, all these factors motivate us to realise a comparator circuit in QCA incorporating a proper underlying clocking circuit. This paper proposes a power aware, cost efficient comparator without less wire-crossing using an efficient and scalable underlying regular clocking scheme which are discussed more details later in this article. The most prominent contribution of this research as follows:

A novel comparator circuit is proposed and the cost effectiveness of the proposed design is evaluated. A new regular clocking scheme is introduced and utilised in the extension of the proposed comparator. The significant challenge of the augmentation of the underlying clocking circuit is reported.

The evolution and performance analysis of the design is presented which outperform the existing works in the literature. The functionality of the proposed comparators has been verified by QCA designer and the power analysis have been carried out by QCAPro tool. The rest of the paper is organized in the following manner; The proposed comparator and its realization in QCA is being illustrated in Section 2. The next Section 3 deals with the simulated result, comparative discussion, cost efficiency and power dissipation analysis of the proposed logic. Finally, in Section 4, conclusion are drawn.

## 2. RESEARCH METHOD

The comparator design presented in [35] used two 5-input majority gate along with one 3-input majority gate. Both the 5-input majority gates used one inverted input and output besides a number of inverters from the second 5-input majority gate to the 3-input majority. Moreover, all the inputs are used repeatedly instead of using them single time and make a wire to connect them in the other majority gate. This layout could avoid the crossover but failed to produce a robust and efficient design. In the proposed design in [34, 37] a simple and compact design can be observer. However, both the layouts have used multi-layer cross over which not only increases the complexity of the design but also buildability overhead increases. The constraint of wire-crossing was resolved in the designs proposed in [32, 38], where the cross over based on rotated cell ( $90^0$  and  $45^0$  cell) were used which still has the same impact on fabrication. An optimized design with normal cell based and wire crossing less layout claims to be declined in area, cell complexity proposed in [36]. None of them did considered the proper layout of the underlying clocking scheme and it motivated us to design a regular clock based comparator rather follows the rule of considering number of cells in a clocking zone.

### 2.1. Design method of compartor and its QCA layout

A binary comparator, an essential combinational circuit in logic design is extensively used in central processing unit (CPU), ALU circuit and micro-controllers. It accesses two numbers and returns whether a number (say A) is greater ( $A > B$ ), lesser ( $A < B$ ) or equal to ( $A = B$ ) the other number (say B) as formulated in Table 1. In this section, a QCA technology based efficient single layer comparator design is proposed. The block diagram and the logic function for the comparator is represented in Figure 2 and (1) respectively.

$$f(A, B) = \{A > B, A = B, A < B\} \quad (1)$$

where, A and B are the inputs to the composite gate. From the truth Table 1, the outputs of the comparator can be expressed as following (2):

$$f(A > B) = A.\bar{B}$$

$$\begin{aligned}
 f(A = B) &= \overline{(A \oplus B)} \\
 f(A < B) &= \overline{A} \cdot B
 \end{aligned}
 \tag{2}$$

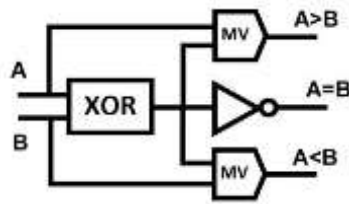


Figure 2. Block diagram of comparator

Table 1. Comparator truth table

Inputs		Outputs		
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

However, from the design perspective to reduce the inverters and the gate count in the expression used in (2), the expressions can also be rewritten using two majority voter gate and one XOR gate and one inverter only, as shown in (3) and the corresponding circuit diagram is shown in Figure 3(a). From the circuit diagram it can be noticed that, the XOR gate followed by an inverter can generate the logic for equality. To realize A>B and A<B, the output produced by XOR gate can be made ANDed with input A and B respectively. The XOR gate itself uses a single majority gate and the cell response methodology as proposed in [28], which ultimately reduces the QCA cost of the circuit. At the same time, the design complexity is reduced with the only use of majority gate and inverter only. Accordingly, the schematic diagram and the QCA layout for the proposed circuit is displayed in Figure 3.

$$\begin{aligned}
 f(A = B) &= \overline{(A \oplus B)} \\
 f(A > B) &= (A \oplus B) \cdot A \\
 f(A < B) &= (A \oplus B) \cdot B
 \end{aligned}
 \tag{3}$$

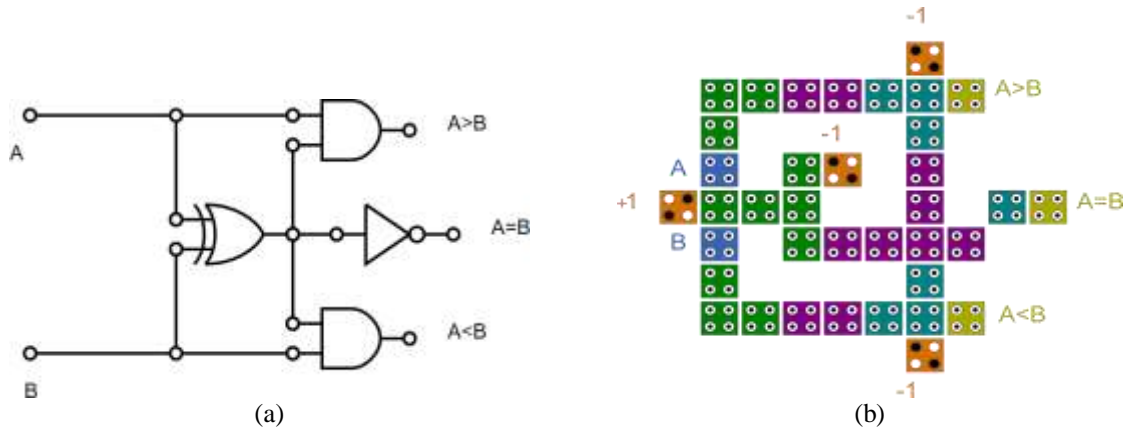


Figure 3. Proposed comparator (a) Schematic diagram (b) QCA layout

From the diagram shown in Figure 3(b), it is inferred that the expression drawn for the proposed comparator requires 2 majority gates, 1 single clock zone based XOR gate and a single inverter. The important property of cell response of QCA is utilized for the achievement of less area, high density and enhanced performance. The simulated waveform generated for the proposed comparator is depicted in Figure 4. While verifying the results with the simulated value, the exact magnitude with high polarization as per the comparator truth table were perceived with no noticeable data loss. This design comprises of 37 cells (all 90° cell) utilizing an area of 0.06 m<sup>2</sup> and utilizing only 3 clock zones. The single bit coplanar comparator was simulated and verified using QCADesigner [52] version 2.0.3 in bi-stable approximation keeping the parameters in default mode.

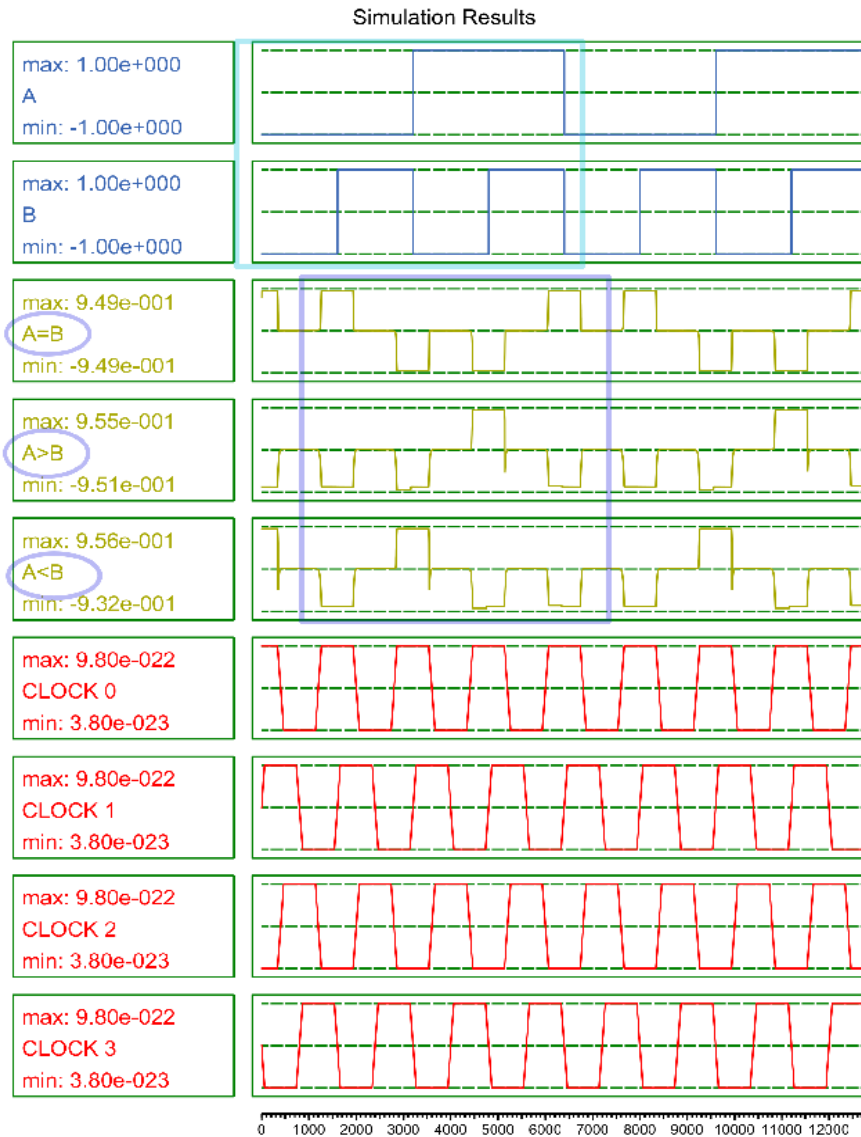


Figure 4. Simulation result of the proposed comparator

## 2.2. Regular clocking based realization

Regular clocking scheme initially proposed in [46] which after further study and analysis proposed for regularity, uniformity and bounded shaped in [48]. However, both of them did not propose any formal scheme. The first ever formal design for the formulation of clocking scheme was proposed in [49] (two-dimensional QCA clocking schemes) as shown in Figure 5(a). Whereas, number of rotated grid of cell is to be arranged for the support of feedback loop, which indicates it was neither easily scalable nor robust and efficient for sequential circuits. This critical issue was resolved in [50] (shown in Figure 5(b)) with an added complication of multi-layer wire crossing in the design. Later, a robust and scalable scheme with coplanar wire crossing was proposed in [51]. With the added benefit of three-directional information flow in any particular clock zone, it lacks in continuous underlying wire connection for clock zone 3 (Figure 5(c)). It however, increased the number of underlying metal crossing. These issues may influence to introduce a new robust, efficient and scalable clocking scheme with minimized underlying metal wire crossing.

As stated above, use of underlying clocking scheme makes a design more suitable one for fabrication and practical realization. In this regard, a proper synchronization between majority gates and the clocking along with the latency plays an important role. The arrangement of the gates should be in successive manner of clocking zones with some addition cells for appropriate synchronization from input to output [53]. For the specification of cells, routing algorithms, placement and fabrication; a regular clocking scheme play



an important role in enabling the QCA technology to progress [50]. The existing regular clocking schemes illustrates that, the contiguous zone number are used to identify the adjacent clock zones. Like, Switch phase (number 1) followed by Hold phase (number 2) followed by Release phase (number 3) and so on.

Taking all these issues along, a new clocking scheme with all the desired advantages and eliminating the pitfalls of the existing with a special requirement of reduction in underlying metal wire crossing was required. The clocking layout for the similar regular clocking scheme can be seen in Figure 6(a) along with the indication of feedback path realization in both clock wise and anti-clock wise directions. The clock wise feedback loop is directed with red lines and the anti-clockwise loop is shown with yellow lines (as pointed in Figure 6(b)).

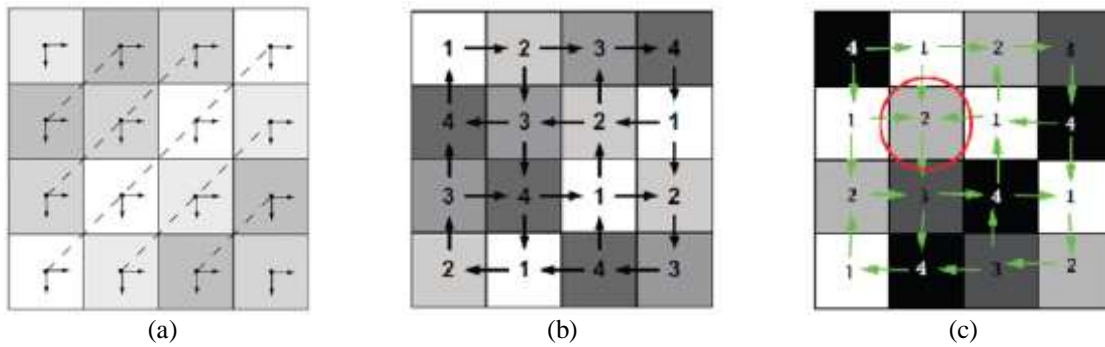


Figure 5. Regular Clocking Scheme (a) 2-D wave proposed in [49] (b) USE proposed in [50] (c) RES Clocking Scheme proposed in [51]

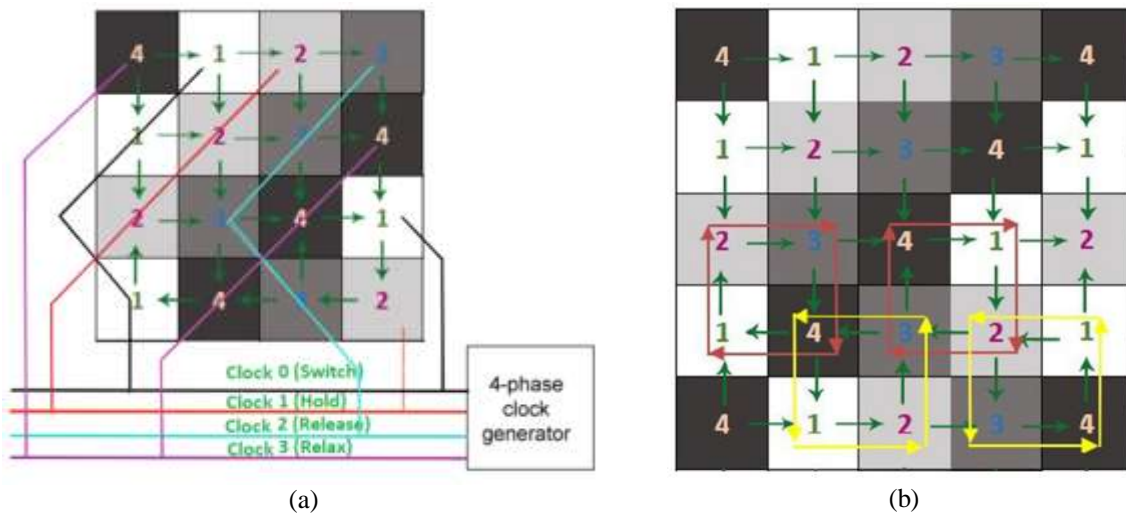


Figure 6. (a) 4X4 grid layout of new regular clocking Scheme (b) Realization of feedback path

Accordingly, with the advent of the new regular clocking scheme, the proposed comparator was expanded using the same as depicted in Figure 7. Figure 7(b) illustrates the first QCA layout for comparator design, overlay by a grid of cells with regular clock zones. It is designed with a 65 grid from the extended version of the newly introduced clocking scheme. It simply replicates the QCA design with 3 majority gate and a single inverter. The Figure 7(a) shows the corresponding grid of cell used to implement the design. For the ease of the design, the cell responsible for cell response property in the XOR gate has been kept in the clock zone 3. It consists of 82 cells in an area of 0.18 m<sup>2</sup> with a latency of 1.5 clock cycles; which indicates the superiority of the design in respect to most of the metrics and also the compactness of the design. This is an efficient, scalable and robust implementation in a single layer avoiding any wire cross using 90° cells only. In accordance with this, the output for the design using regular clocking is also shown in Figure 8, which also claims the functionality of the comparator with a delay in the clocking.

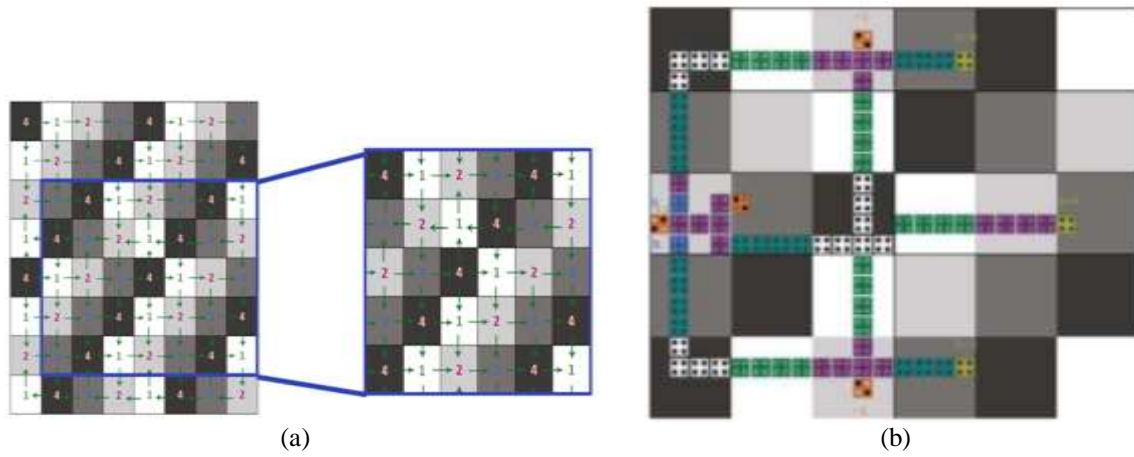


Figure 7. (a) partitioned grid from extended version of new regular clocking (b) regular clocking scheme-based comparator

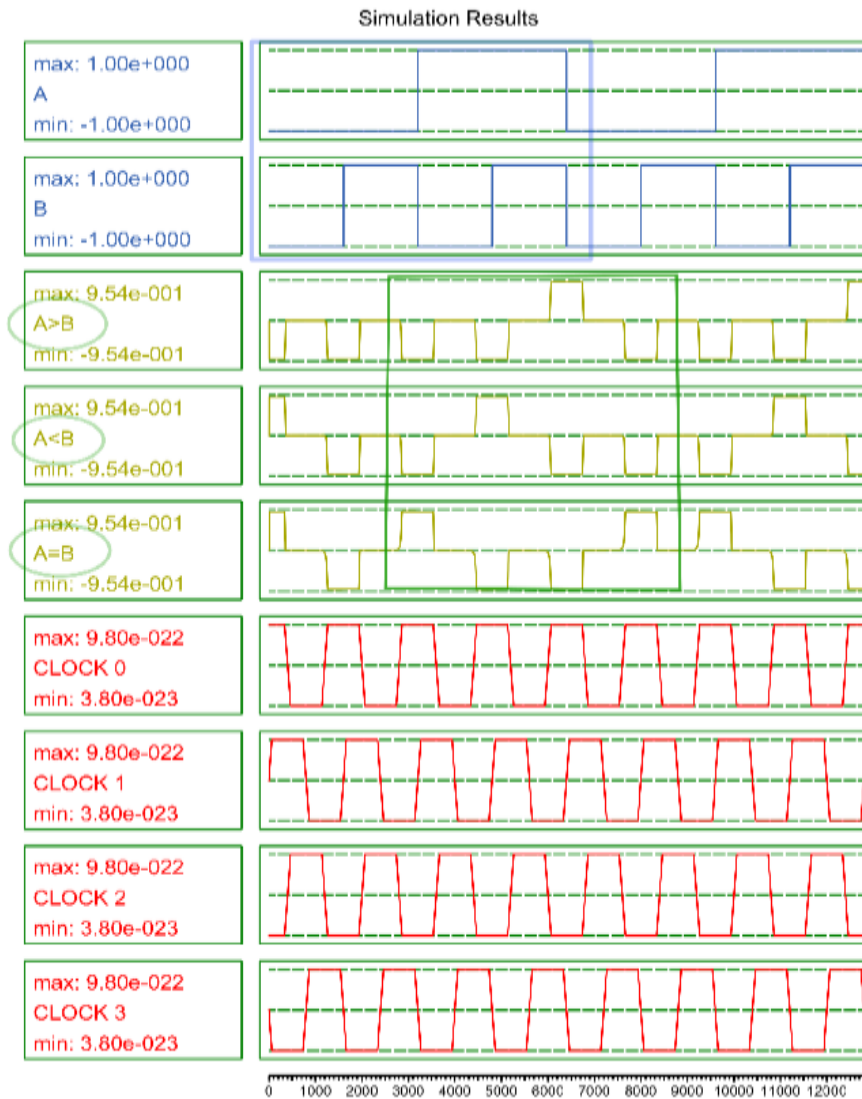


Figure 8. Simulation result of the comparator using underlying regular clocking

### 3. RESULTS AND DISCUSSION

This section discusses the exploration of the comparisons with the designs in its counterparts. The cost efficiency and power dissipation analysis were shown to prove the completeness of the design. Table 2 represents the comparative result analysis of the proposed comparator design in this paper with previously existing designs in [32-38, 39-40]. The multi-layer based design as reported in [33, 34, 37], which is not a convenient approach for fabrication. It can be noticed that, the design with optimized area in [40] is based on deposited cell alignment at input 'A'. The cell misplacement is one of the common faults that can occur at cell deposition phase and makes the circuit more prone to faulty circuit [54, 55]. The other design, utilizing minimum area can be found in [39], but compromises the gate count and scalability of the design. Considering the robustness, fault-free and reduced complex circuit (in terms of gate counts), the proposed design has a sustainable improvement in cell count and latency. However, the striking observation can be made that, no previous design has considered regular clocking scheme and thus reducing the fabrication burden. The efficiency, scalability and robustness of the circuit also enhanced with the consideration of regular clocking while design. The proposed efficient comparator designed in QCA considerably, improves in gate counts (majority, inverter) with a stable polarized output, at a great deal. Most importantly, implementation with the proposed clocking scheme not only makes the proposed comparator surplus the existing design in this metrics, but also a design with a minimum number of underlying metal wire crossing is explored.

Table 2. Comparison of comparator by conventional metrics

Proposed	Cell#	Latency	Majority#	Inverter#	Crossover#	Layer Type	Area (in m <sup>2</sup> )	Regular
In [32]	53	1	3	1	2	Coplanar	0.07	No
In [33]	319	3	17	14	6	Multi-Layer	0.343	No
In [34]	79	1	5	4	5	Multi-Layer	0.0388	No
In [35]	43	1.25	3	8	0	Coplanar	0.08	No
In [36]	117	2	8	3	0	Coplanar	0.182	No
In [37]	100	1	3	3	2	Multi-Layer	0.13	No
In [38]	99	1	3	3	2	Coplanar	0.13	No
In [39]	42	0.75	3	4	0	Coplanar	0.05	No
In [40]	38	0.5	3	3	0	Coplanar	0.03	No
In Figure 3	37	0.75	2	1	0	Coplanar	0.06	No
In Figure 7	82	1.5	2	1	0	Coplanar	0.18	Yes

#### a. Cost analysis

As the technology advances, area-delay product has the dominance in calculating the cost in CMOS [56]. It was found to be helpful in optimum design in VLSI. It was reconsidered with further studies [44] and proposed CMOS technology cost function as following (4):

$$\text{Cost} = A \times T^2 \quad (4)$$

where A denotes the area of the circuit and T represents the delay or number of clock used from input to output of the circuit. Likewise CMOS, a cost functions for QCA circuit needed to be investigated and subsequently a new function was proposed in [45] considering cell count, gate count, area, delay and number of crossover metrics as presented in (5).

$$\text{Cost}_{\text{QCA}} = (M^2 + I + C^2) \times T^2 \quad (5)$$

where, M) Majority gates count, I) inverters count, C) number of crossovers and T) QCA delay (Latency).

The clocking zones count denotes the latency and an important metric in the analysis of circuit performance. An important factor in QCA technology is the crossover, which require proper arrangement during fabrication [57]. Multi-layer crossover based design have thrice the cost of single layer design. Thus, it is a peerless metric in QCA cost functions and it also evaluates complexity and fabrication difficulty. Inverters measures complexity and majority gates count is used to measure both complexity and power dissipation. These are the established and mostly used formulations which is used in the evaluation of QCA cost. The proposed comparator design is compared in terms of QCA cost by using both of these (4) and (5), and the comprehensive results are shown in Table 3. The optimum cost can be observed in case of design in [40] with (4), but it suffers with cell misplacement fault [58]. A slight change in the position of the cells adjacent to input 'A' in the proposed design may lead to completely different or wrong output pattern. Thus, the robust and efficient design proposed in this paper, observes a significant improvement while comparing the proposed design with the other counterparts. A sustainable gain has been recorded with the well established and appropriate QCA cost equations for QCA circuits (5). Thus, the proves our claim for a cost-effective design and buildability using regular clocking scheme.



The extensive comparison of the proposed design with the matching counterparts shows that the design is optimized in terms of QCA cost and can be considered as better design and also useful more complex QCA designs. In accordance with the results as per Table 2 and Table 3, the proposed comparator achieves a significant improvement in area, cell count and QCA cost. Moreover, the comparator design using the regular clocking scheme also render equivalent efficiency as compared to the existing designs without regular clocking which exhibits the efficiency of the design.

Table 3. Cost of comparator

Comparator	Area x Delay <sup>2</sup>	(M <sup>2</sup> +I+C <sup>2</sup> ) x T <sup>2</sup>	Regular Clocking
In [32]	0.72	14	No
In [33]	3.01	3051	No
In [34]	0.04	54	No
In [35]	0.13	26.6	No
In [36]	0.72	268	No
In [37]	0.13	16	No
In [38]	0.13	16	No
In [39]	0.03	7.3	No
In [40]	0.01	3	No
In Figure 3	0.03	2.8	No
In Figure 7	0.41	11.25	Yes

### b. Power analysis

In this section the study related to energy dissipation of the proposed comparator is discussed. The energy dissipation is approximated using the QCAPro [43] with different kink energy values. Kink energy is the distinction between the conditions of the cell have inverse polarization and the condition of same polarization [42]. Energy dissipation of QCA layout is calculated utilizing Hamiltonian matrix for two state system presented by (6).

$$H_i = \Sigma \begin{bmatrix} \frac{-1}{2} P_j E_{i,j}^k & -\gamma \\ -\gamma & \frac{-1}{2} P_j E_{i,j}^k \end{bmatrix} \quad (6)$$

Where  $E_k$  represents kink energy between the cell  $i$  and  $j$ . It also presents the energy cost of cell ( $i$  &  $j$ ) with opposite polarization. The tunneling energy ( $i$ ) of the electron depends on the clock. The summation of each cell in the area of the radius of cell  $i$  as shown in (7) remain fixed during simulation.

$$E_{ij} = \frac{1}{4\epsilon_0\epsilon_1} \sum_{n=1}^p \sum_{m=1}^q \frac{q_{i,n}q_{j,m}}{|r_{i,n}r_{j,m}|} \quad (7)$$

QCAPro supports three different tunneling energy levels ( $0.5 E_k$ ,  $1 E_k$ , and  $1.5 E_k$ ) and the proposed design have been analyzed under all the levels. The values are evaluated using QCA layout, switching vector and test vector as inputs to QCAPro considering the temperature of 2K. The thermal layout map and the polarization map for the proposed comparator with a tunneling energy of  $1.5 E_k$  are depicted in Figure 9. It can be observed that, the energy dissipation is higher for the cell with darker spot. Therefore, darker the cell more likely to generate higher value of polarization. Table 4 shows the analysis of energy dissipation for the cost efficient comparator in all distinct levels ( $0.5$ ,  $1$ , and  $1.5 E_k$ ) at 2 K temperature. The results shed light on the fact that, the proposed design is not only cost effective design with a regular clocking, but also a power aware circuit.



Figure 9. Energy dissipation map for proposed (a) comparator (without clocking) (b) comparator (with clocking) at  $1.5 E_k$

Table 4. Power dissipation result

Proposed Design	Average of leakage energy dissipation (meV)			Average of switching energy dissipation (meV)			Total energy consumption (meV)		
	0.5Ek	1Ek	1.5Ek	0.5Ek	1Ek	1.5Ek	0.5Ek	1Ek	1.5Ek
Without Clocking	11.31	33.85	60.11	54.61	47.09	40.04	65.92	80.94	100.15
With Clocking	23.91	75.38	136.29	124.69	106.58	89.43	148.6	181.96	225.72

#### 4. CONCLUSION

A cost-effective, coplanar QCA comparator design is proposed without/with regular underlying clocking circuit. The augmentation challenge of the underlying clocking circuit with QCA cell layout is addressed successfully and a proper design is established. Both the cell-layout of the comparator (without & with clocking circuit) are analysed and a significant improvement in area in coplanar approach, latency and QCA cost of the circuit with a consideration of robust, low complex and fabricable issues. It is worthy to mention that the proposed comparator outperforms the existing circuits enabling a regular clocking circuit. The simulation results confirm the accuracy of the proposed layout. Again, the power analysis is carried out by QCAPro tool which shows the superiority than the existing designs. Most importantly the use of underlying regular clocking scheme in the extended design of the proposed comparator incurs negligible power dissipation which drives one step forward towards the realization of power-aware circuit. In the near future, the challenges of the power aware circuit in QCA under the influence of regular clocking scheme will be investigated.

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