

Reduction of common mode voltage for cascaded multilevel inverters using phase shift keying technique

Vinh-Quan Nguyen, Quang-Tho Tran

Faculty of Electrical and Electronics Engineering, HCM City University of Technology and Education, Vietnam

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ABSTRACT

Demand of cascaded multilevel inverters in industries of electric drives and renewable energy is increasing due to their large-scale capacity and high voltage. The modulation technique of inverters significantly affects the power quality of the inverter output voltage. This paper proposes a new method of carrier wave modulation using the phase shift keying technique for cascaded multilevel inverters. The phase of a constant frequency carrier wave is changed at an accurate time by an input sinusoidal control signal. This modulation technique is simply implemented and only needs a small memory. It also helps reduce the common mode voltage of inverters in order to suppress the output voltage harmonics. Moreover, the ability to reduce switching count also helps the inverters decrease switching loss. The simulated and experienced results on a cascaded 9-level 3-phase inverter and an F28379D DSP kit have validated the performance of the proposed technique compared with that of the APOD and POD methods.

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Corresponding Author:

Quang-Tho Tran

Faculty of Electrical and Electronics Engineering

HCM City University of Technology and Education, Vietnam

Email: thotq@hcmute.edu.vn

1. INTRODUCTION

Demand of cascaded multilevel inverters is increasing [1-8] in industries of electric drives and renewable energy [4, 9, 10] due to their benefits such as large-scale capacity, the ability to provide a sinusoidal shaped output voltage [11], and suppress dv/dt . The modulation technique significantly affects the power quality of the inverter output voltage. There have been many modulation solutions published, in most these solutions, the control signals are compared directly with the carrier waves that have not been modulated [12-16]. Due to the independence between the carrier wave and the control signal, this makes the carrier wave not contain information of any quantities. Thus, the reconstructing of the control signal in output voltage is very difficult to gain the results as expected. Therefore, the appearance of common mode (CM) voltage in the inverters cannot be avoided. There are many solutions [17-24] to improve the output power quality of inverters by using the reduced-common-mode voltage strategies. However, the increase of carrier wave frequency makes the memory size and switching count increase. This also causes the voltage harmonics and the switching loss to increase. Moreover, the limits of hardware in the fact make these solutions be difficult to implement due to higher expenditures.

The phase shift keying technique (PSK) has been used extensively in telecommunication [25-28], but it has never been used in inverters. PSK is a digital process of modulation which conveys information data of a control signal by modulating the phase of a constant frequency carrier wave. This paper proposes a method for carrier wave modulation of cascaded multilevel inverters using the phase shift keying technique. The PSK of carrier waves in every fundamental period helps the switching of the switches become more

optimal in every voltage level. As a result, the advantages of the proposed method help reduce the common mode voltage and improve the power quality of inverter output voltage. In addition, the results of the proposed method are also compared with those of the alternative phase opposition disposition (APOD) and phase opposition disposition (POD) techniques. The performance has also been validated by relying on the results of simulation and experiment on a cascaded 9-level inverter system and an F28379D DSP kit for balanced and unbalanced DC sources. A cascaded 9-level inverter model is showed in Section 2. The phase modulation carrier wave of the proposed method is presented in Section 3. Section 4 shows the simulation and experiment results and discussions for the PSK, APOD and POD methods to validate the performance of the proposed method. The benefits of modulated carrier waves are also concluded in Section 5.

2. CASCADED 9-LEVEL INVERTER SYSTEM

The one-phase structure of a cascaded 9-level H-bridge 3-phase inverter is presented in Figure 1. Where S_{jx} is the state ON/OFF for the upper switches respectively as (1), with the phase $x=a, b, c$. The lower switches are symbolized as S'_{jx} . Each phase terminal of inverter is connected with an inductor L as 50mH and a load resistor R as 45Ω. The voltage of each DC source is 30V.

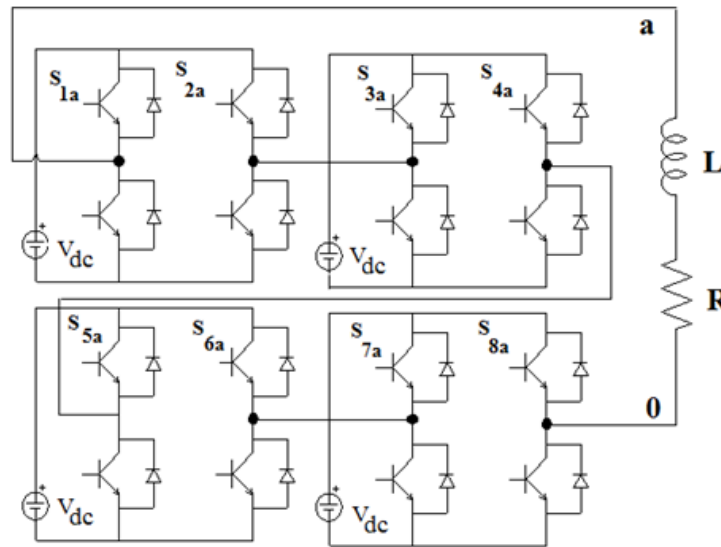


Figure 1. Phase A of a cascaded 9-level H-bridge 3-phase inverter

$$\text{Where: } S_{ja} + S'_{ja} = 1; \quad \text{with } j = 1 \div 8 \tag{1}$$

Table 1 describes the switching states of switches for phase A. Where $n=9$ is the level number of the inverter and the dc voltage sources are the same, 9 levels of output voltage are $-4V_{dc}, -3V_{dc}, -2V_{dc}, -1V_{dc}, 0, +1V_{dc}, +2V_{dc}, +3V_{dc},$ and $+4V_{dc}$ respectively. In the inverter control diagram showed in Figure 2, $g(t)$ is the control signal with the magnitude from -1 to $+1$, $G(t)$ is the signal normalized appropriate to the number of levels for inverter and given in (2).

Table 1. The switching state of switches for phase A

n	S_{1a}	S_{2a}	S_{3a}	S_{4a}	S_{5a}	S_{6a}	S_{7a}	S_{8a}	Output voltage
0	0	1	0	1	0	1	0	1	$-4V_{dc}$
1	0	1	0	1	0	1	0	0	$-3V_{dc}$
2	0	1	0	1	0	0	0	0	$-2V_{dc}$
3	0	1	0	0	0	0	0	0	$-1V_{dc}$
4	0	0	0	0	0	0	0	0	$0V_{dc}$
5	1	0	0	0	0	0	0	0	$+1V_{dc}$
6	1	0	1	0	0	0	0	0	$+2V_{dc}$
7	1	0	1	0	1	0	0	0	$+3V_{dc}$
8	1	0	1	0	1	0	1	0	$+4V_{dc}$

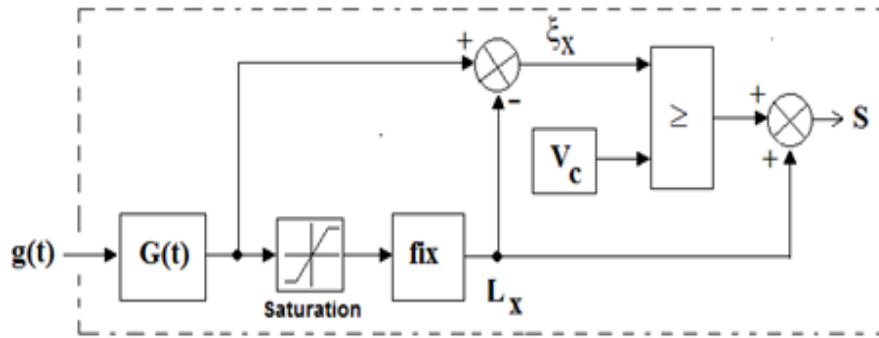


Figure 2. Control diagram of the inverter

$$G(t) = (g(t) + 1) \frac{n-1}{2} \tag{2}$$

In the control model for the cascaded inverter, two components of the voltage $G(t)$ are ξ_x and L_x ($x=a, b, c$). Where $0 \leq L_x \leq n-2$ is the integer of the signal $G(t)$ and given by (3).

$$L_x \begin{cases} n - 2, & \text{if } G(t) \geq n - 2 \\ \text{fix}(G(t)), & \text{otherwise} \end{cases} \tag{3}$$

And $0 \leq \xi_x \leq 1$ is the remainder after division and given by (4).

$$\xi_x = G(t) - L_x \tag{4}$$

3. THE PROPOSED CARRIER WAVE PHASE MODULATION

The carrier wave is described as (5).

$$e(t) = A_c \cos(\omega_c t + \theta) \tag{5}$$

The carrier wave before normalization has a form as (6) in Figure 3. Where ω_c is as $2\pi f_c$ and θ is the phase angle.

$$c(t) = \frac{2}{\pi} \sin^{-1}(e(t)) = \frac{2}{\pi} \sin^{-1}(A_c \cos(\omega_c t + \theta)) \tag{6}$$

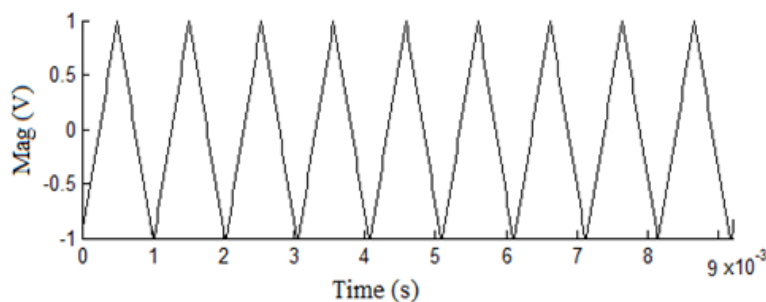


Figure 3. Carrier wave $c(t)$ before normalization with $A_c=1$ and $f_c=1\text{kHz}$

The carrier wave has been normalized by (7) and showed in Figure 4. Where $\max(c(t))$ and $\min(c(t))$ are the maximum and minimum magnitudes of $c(t)$ respectively. The spectrum of unmodulated carrier wave in Figure 5 shows the magnitude as 0.4 at the frequency of 1kHz and its THD as 10.51%.

$$V_c(t) = \frac{\max(c(t)) + c(t)}{\max(c(t)) + \min(c(t))} \tag{7}$$

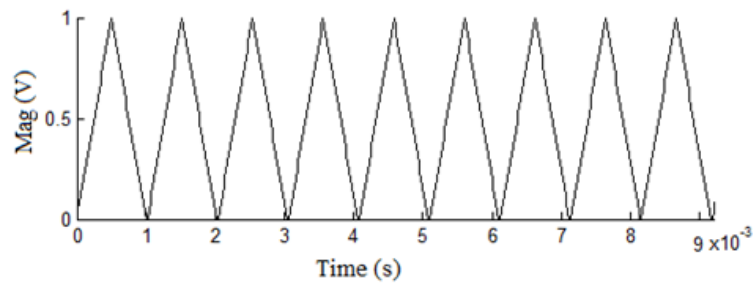


Figure 4. Normalized carrier waves

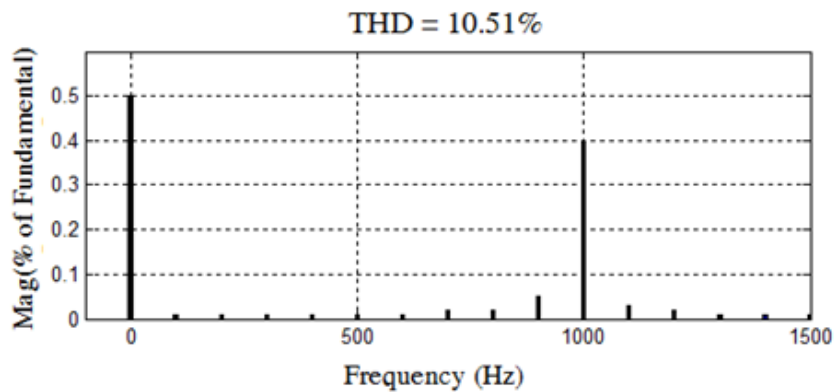


Figure 5. Carrier spectrum before modulation

This showed that the carrier wave before modulation is completely independent from the control signal. Thus, it is very difficult to reconstruct the control signal basing on such carrier waves. This leads to producing the common mode voltage (CMV) and output voltage harmonics.

3.1. The proposed phase shift keying technique

A sinusoidal control signal as (8) is used to modulate the phase of carrier wave.

$$g(t) = E_m \sin(\omega_m t) \tag{8}$$

The PSK modulated waveform can be in phase or opposite phase with the control signal $g(t)$. This waveform is also described as (9)

$$c_{PSK}(t) = A \cdot d(t) \cdot c(t) \tag{9}$$

Where $A = \pm 1$ is the magnitude of the high frequency carrier wave, $c(t)$, and $d(t) = \pm 1$ depends on the control signal.

$$d(t) = \begin{cases} +1 & \text{for } g(t) \geq 0 \\ -1 & \text{for } g(t) < 0 \end{cases} \tag{10}$$

Figure 6 is the waveform of $d(t)$ with the magnitude of ± 1 . It also is a function of the control signal $g(t)$ and the PSK modulated carrier wave. The normalized carrier wave can be obtained from (7) as follows:

$$V_{PSK}(t) = \frac{\max + c_{PSK}(t)}{\max + \min} \tag{11}$$

The PSK modulated carrier wave $V_{PSK}(t)$ with the frequency of 1KHz is shown in Figure 7. The spectrum of this carrier wave is also shown in Figure 8 with the magnitude of 0.42 at the frequency of 1kHz and THD as 12.17%.

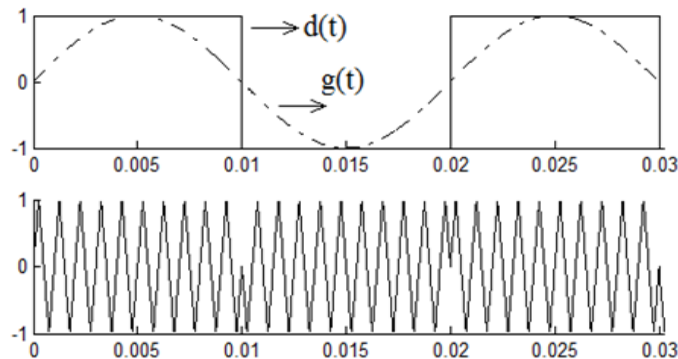


Figure 6. PSK modulated carrier waves

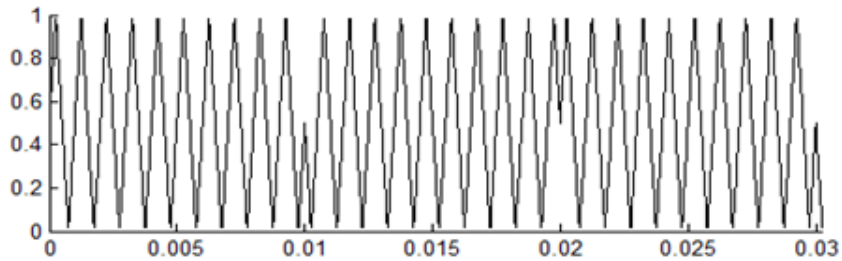


Figure 7. Normalized PSK carrier waves of one phase

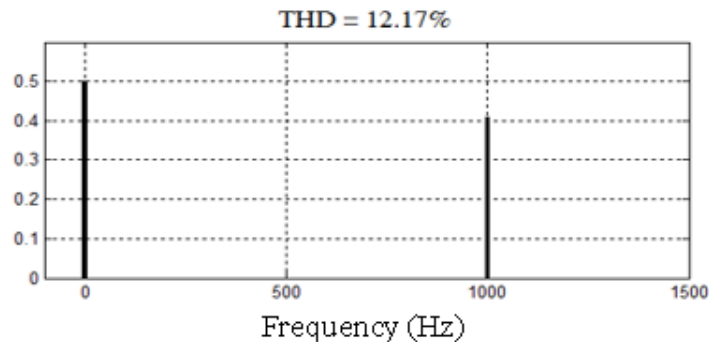


Figure 8. Spectrum of PSK carrier waves

The common mode voltage of the unmodulated carrier waves in Figure 9(a) is $\pm 2V_{dc}/3$ for $E_m=1$, twice higher than that of the PSK method in Figure 9(b) and satisfied (12).

$$V_{CM} = \frac{V_{ao} + V_{bo} + V_{co}}{3} \tag{12}$$

Basing on Figure 9 and (12), at the specific moment t , the common mode voltage for the unmodulated carrier waves in Figure 9(a) is +20V (as $2*V_{dc}/3$) while that of the modulated ones using PSK in Figure 9(b) is +10V (as $1*V_{dc}/3$). The phase shift of carrier waves in every fundamental period helps the switching state change more optimal and reduce the common mode voltage.

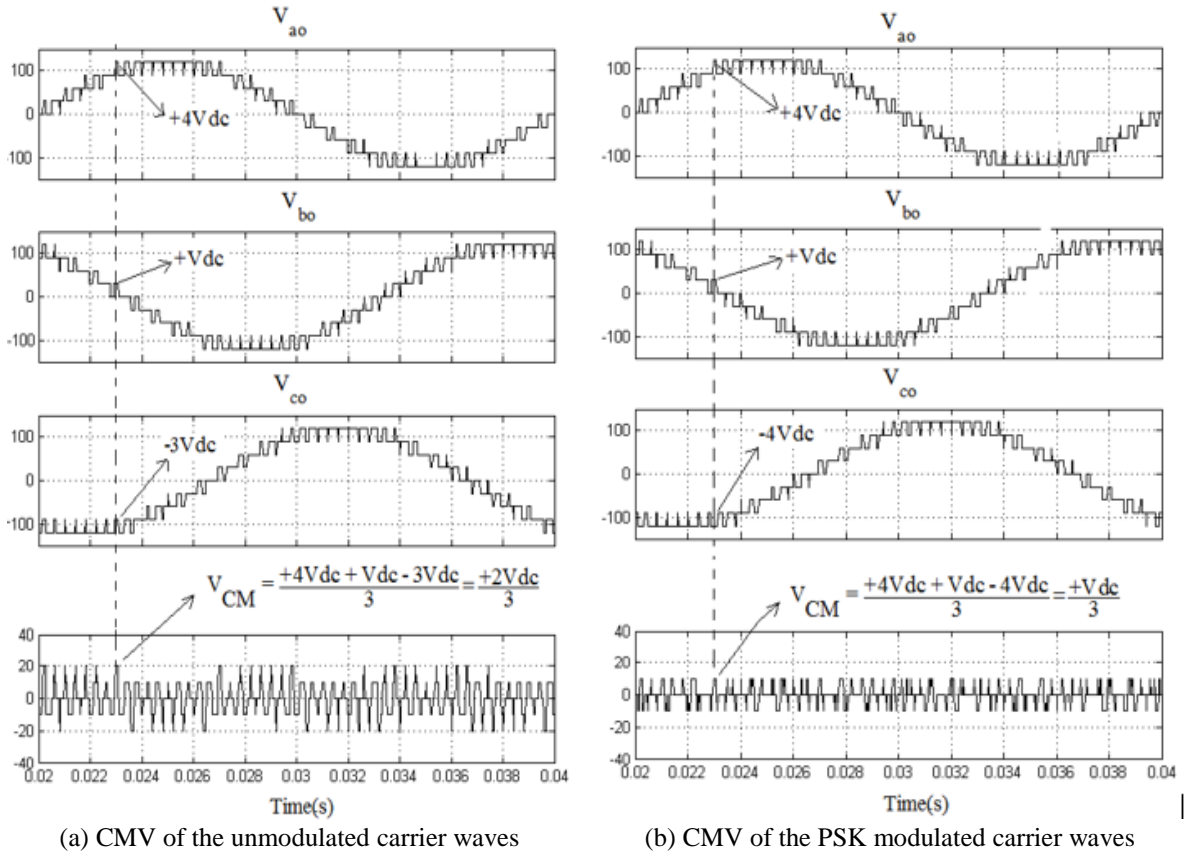


Figure 9. Phase voltages and common mode voltages

3.2. Strategy for reducing the number of switching commutations

In order to enhance the performance of the PSK method much more, an offset function ξ_o is also proposed to add ξ_x in this paper as (13). Where $n=9$ is the level of inverter and F_L is as (14). When using the proposed strategy in Figure 10, the number of switching commutations in one fundamental period is also decreased and showed in Section 4.

$$\xi_o = \begin{cases} 1 - \max(\xi_x), & \text{if } F_L = \frac{3(n-1)}{2} - 2 \\ -\min(\xi_x), & \text{if } F_L = \frac{3(n-1)}{2} - 1 \\ 0, & \text{otherwise} \end{cases} \quad (13)$$

$$F_L = \sum L_x, \quad x=a, b, c \quad (14)$$

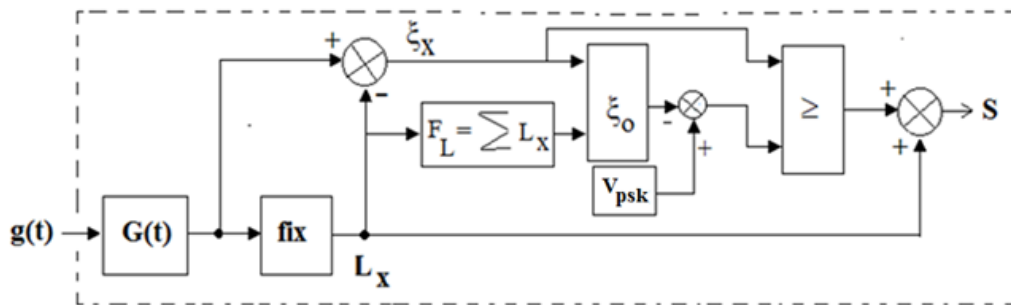


Figure 10. Proposed strategy for reducing the number of switching commutations

4. SIMULATION AND EXPERIMENT RESULTS

The parameters for simulation and experiment system are showed in Table 2. Three magnitude values of E_m as 1, 0.5, and 0.2 are used to test in this paper for validating the wide range of modulation index.

Table 2. System parameters

Description	Value
Inductor L	50 mH
Load resistor R	45 Ω
Sample time Ts	20 μ s
Carrier frequency	2.5 kHz
Deadtime	2 μ s
V_{dc}	30V

4.1. Simulation results

The simulation diagram using PSK technique is showed in Figure 11. Where the inductor L is 50mH and the load resistor is 45 Ω . The simulation results of the PSK, APOD, and POD methods are also shown in Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, and Figure 17 for the different magnitude values of E_m .

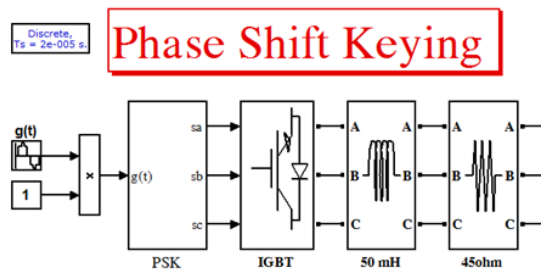
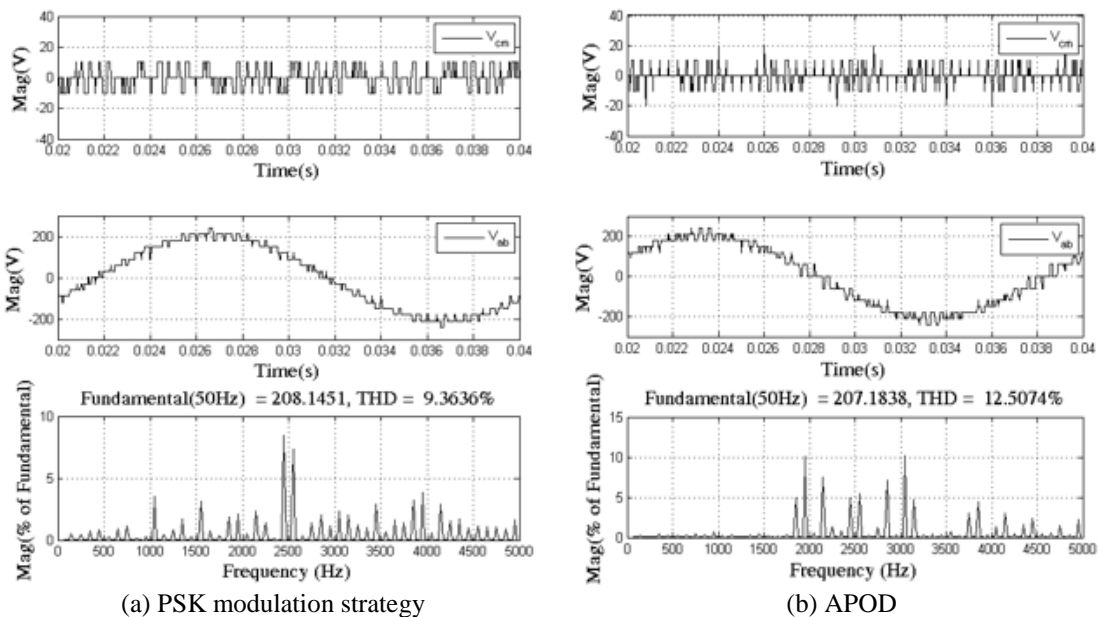
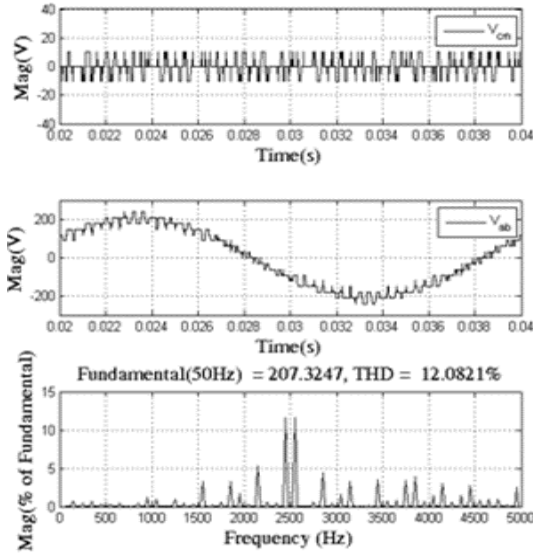


Figure 11. Simulation diagram of PSK modulation

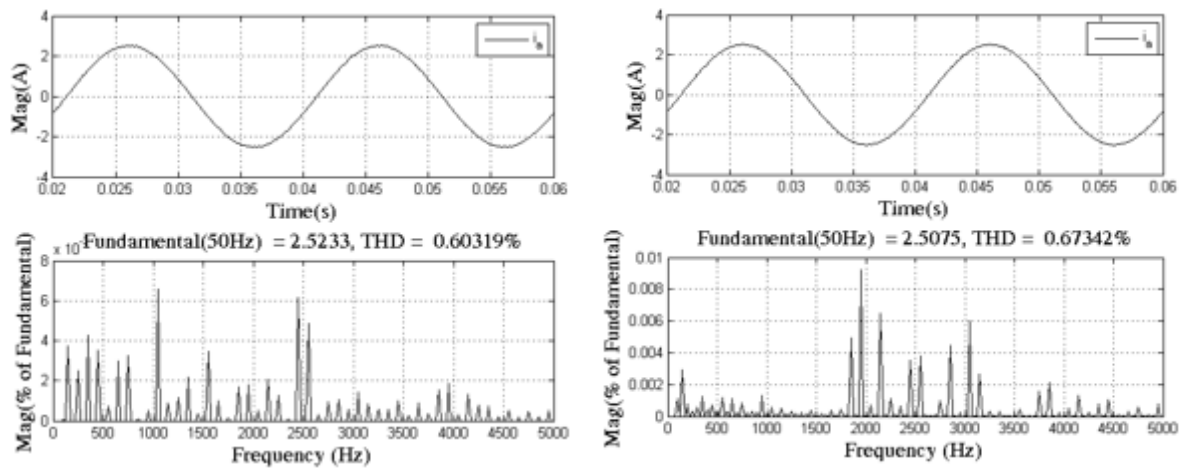
In case $E_m=1$, the CM voltages of the PSK and POD are as $\pm V_{dc}/3$ in Figures 12(a) and 12(c) while that of the APOD in Figure 12(b) is as $\pm 2V_{dc}/3$. In addition, the line voltage THD value of the PSK, as 9.36%, is lower than those of the APOD and POD methods as 12.5% and 12% respectively. This helps the phase current THD value of the PSK method in Figure 13(a), as 0.6%, smaller than those the APOD and POD in Figures 13(b) and 13(c), as 0.67% and 0.7% respectively.





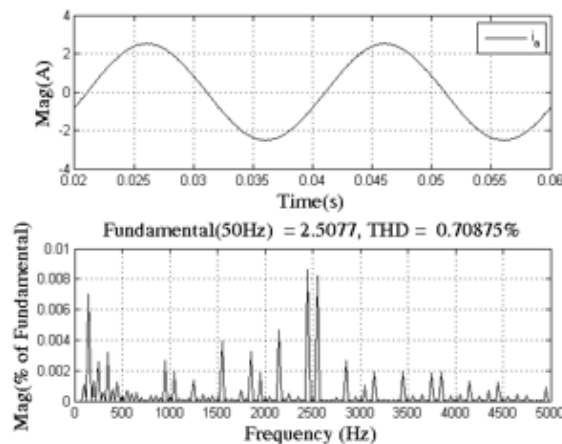
(c) POD

Figure 12. Top Trace: CMV waveform, Middle Trace: Line voltage V_{ab} , Bottom Trace: THD of line voltage V_{ab} for $E_m=1.0$



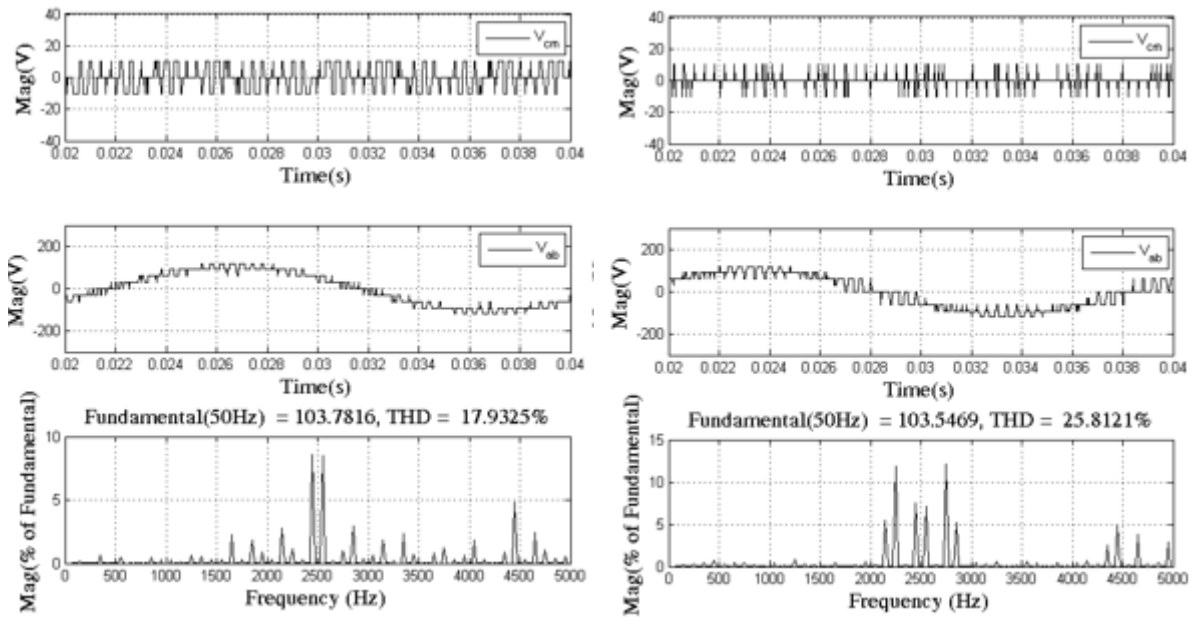
(a) PSK modulation strategy

(b) APOD



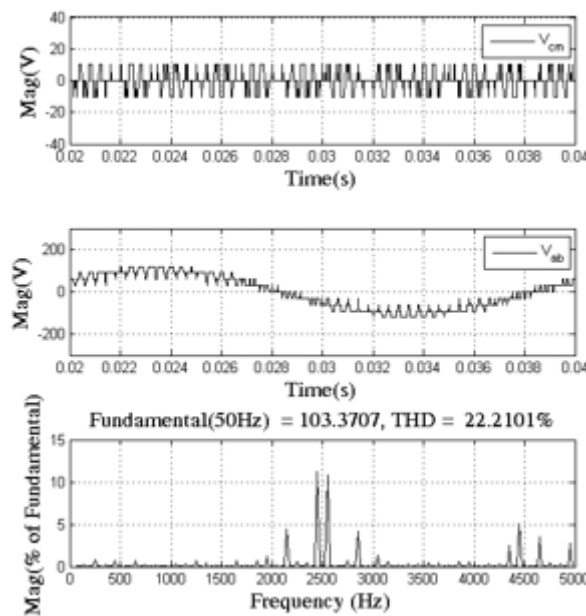
(c) POD

Figure 13. Top Trace: Phase Current i_a , Bottom Trace: THD of phase current i_a for $E_m=1.0$



(a) PSK modulation strategy

(b) APOD



(c) POD

Figure 14. Top Trace: CMV waveform, Middle Trace: Line voltage V_{ab} , Bottom Trace: THD of line voltage V_{ab} for $E_m=0.5$

Similarly, in case $E_m=0.5$, the line voltage THD value of the PSK in Figure 14(a), as 17.9%, is the smallest compared with those of the APOD and POD in Figures 14(b) and 14(c) as 25.8% and 22.2% correspondingly. As a result, the PSK phase current THD, as 0.9% in Figure 15(a), is the lowest compared with those of the APOD and POD as 1.34% and 1.2% in Figures 15(b) and 15(c) respectively.

For $E_m=0.2$, the results in Figure 16 have also showed the voltage THD value of the PSK, as 48.1%, is lower than those of the APOD and POD as 69.1% and 69.7% respectively. The results in Figure 17 also showed the current THD of the PSK is as 2.4%, lower than those of the others as 3.8% and 3.7% respectively. The voltage and current THD values of the three methods according to the magnitude of E_m are also shown in Figure 18. Especially, the line voltage weighted THD factor (WTHD) of the PSK method in the bottom trace of Figure 18 has the same shape as the current THD in the middle trace of Figure 18. This means that the PSK method offers independence from the load parameters R-L [29].

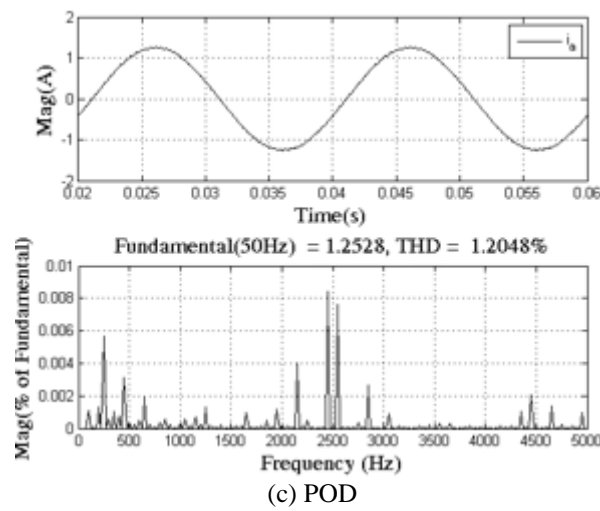
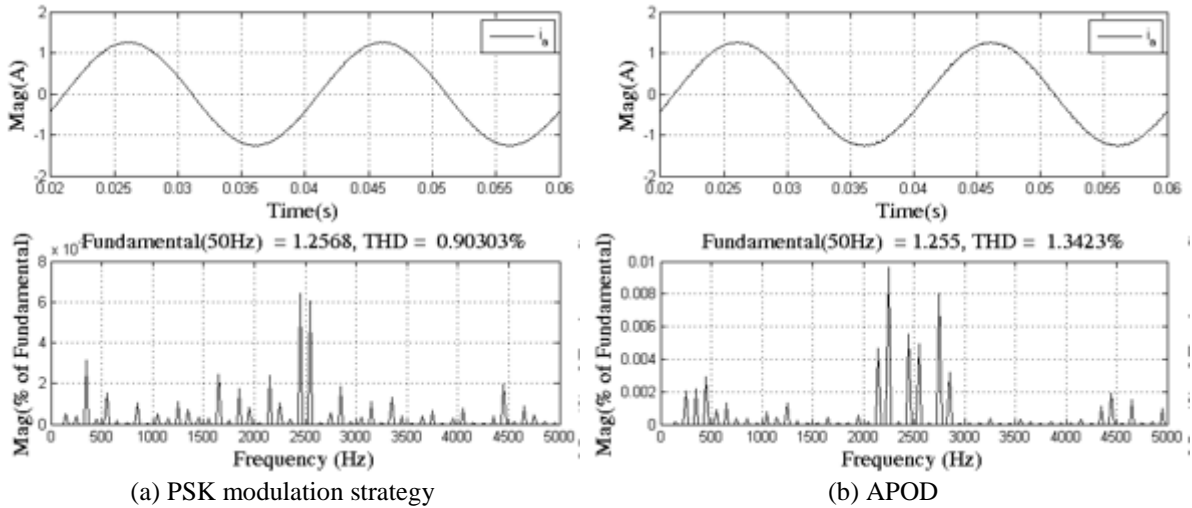
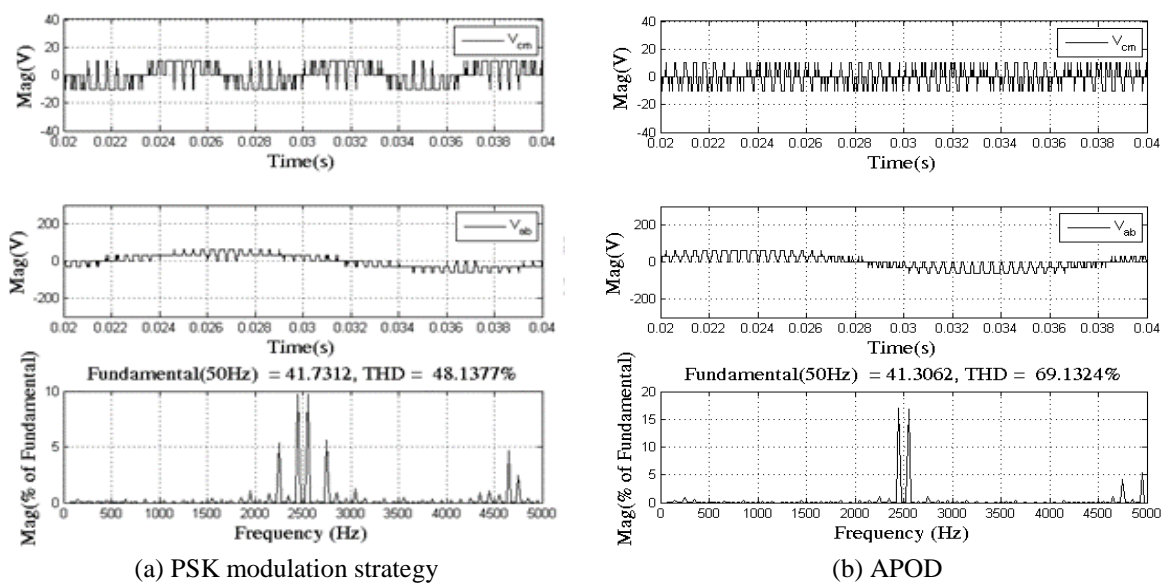


Figure 15. Top Trace: Phase Current i_a , Bottom Trace: THD of phase current i_a for $E_m=0.5$



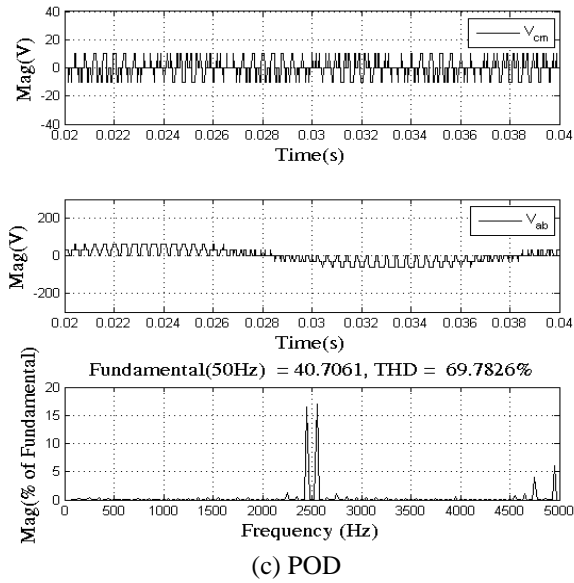


Figure 16. Top Trace: CMV waveform, Middle Trace: Line voltage V_{ab} , Bottom Trace: THD of line voltage V_{ab} for $E_m=0.2$

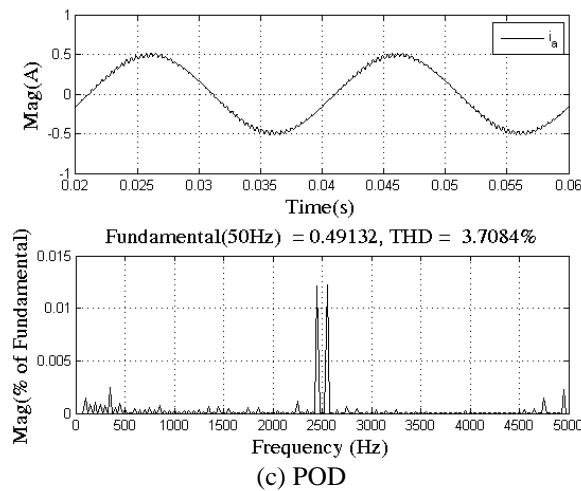
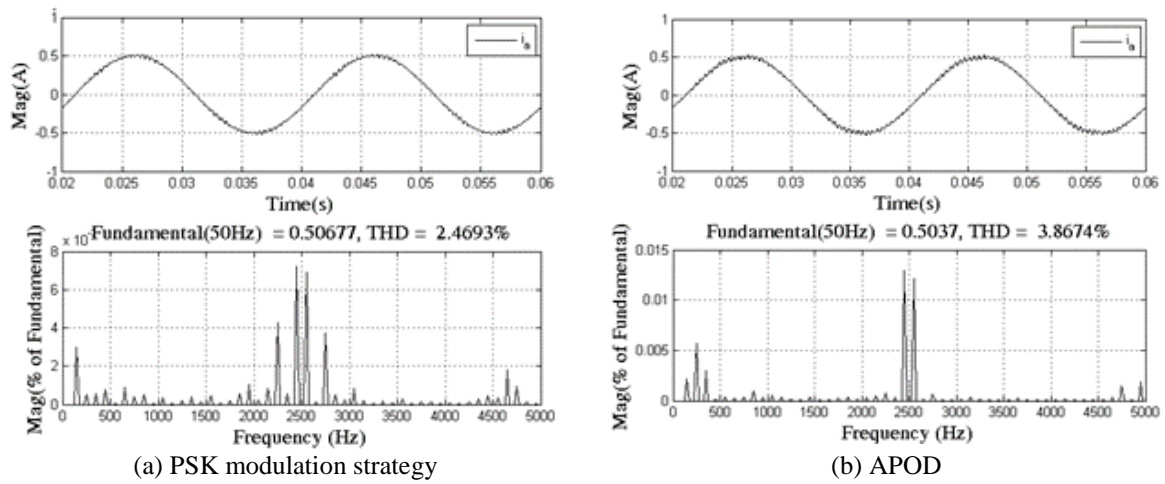
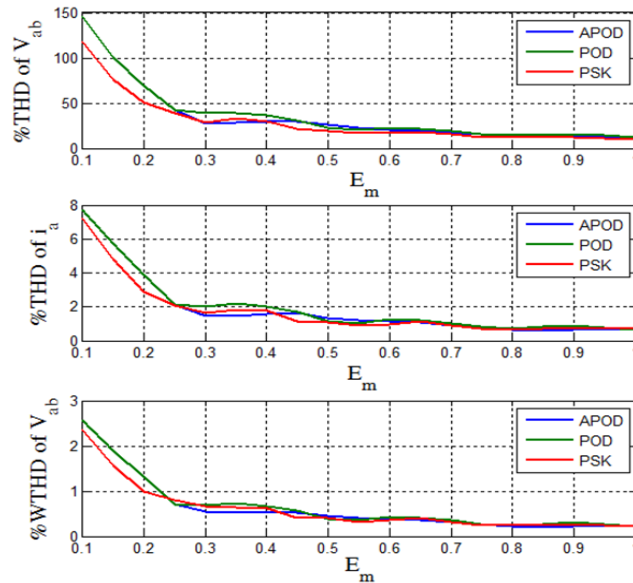
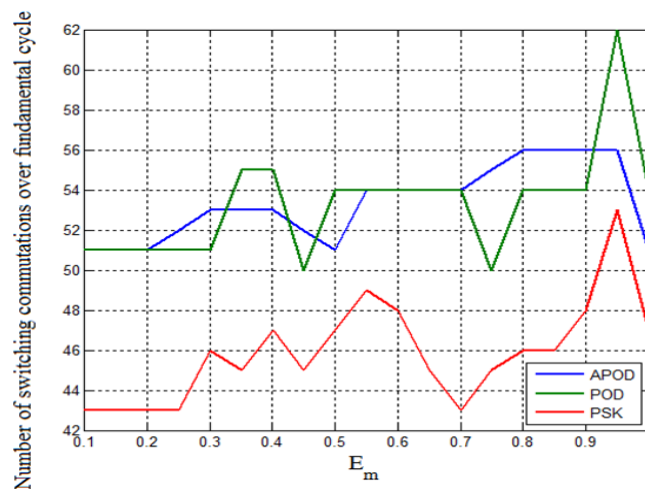


Figure 17. Top Trace: Phase Current i_a , Bottom Trace: THD of phase current i_a for $E_m=0.2$

Figure 18. THD values versus E_m

Moreover, in every fundamental period, the number of IGBT switching commutations in Figure 19 for each phase of the PSK modulation method is low significantly compared with those of the APOD and POD methods when using the proposed strategy in Figure 10. This will contribute to decreasing the switching loss of inverters.

Figure 19. The number of switching commutations versus E_m

4.2. Experiment results

The model used for experiment in this paper has used an F28379D DSP kit and a cascaded 9-level inverter system. The experiment results of the PSK method are shown in Figure 20, Figure 21, Figure 22. The THD comparison of the PSK, APOD, and POD methods is shown in Figure 23. The common mode voltage for $E_m=1$ in the top trace of Figure 20(a) is still $\pm 10V$. However, the center of the CMV is not zero any more. Because the voltages of the DC sources in the fact are not the same as 30V. This also proves that the PSK method is true for the unbalanced DC sources. The line voltage THD is 12.6% and the phase current THD is 1.9%. These experiment values are slightly higher than those of the simulation results in Figure 12 and Figure 13. However, the experiment values of the APOD and POD are also slightly higher than those of the simulation results respectively due to the hardware parameters slightly different from the simulation ones.

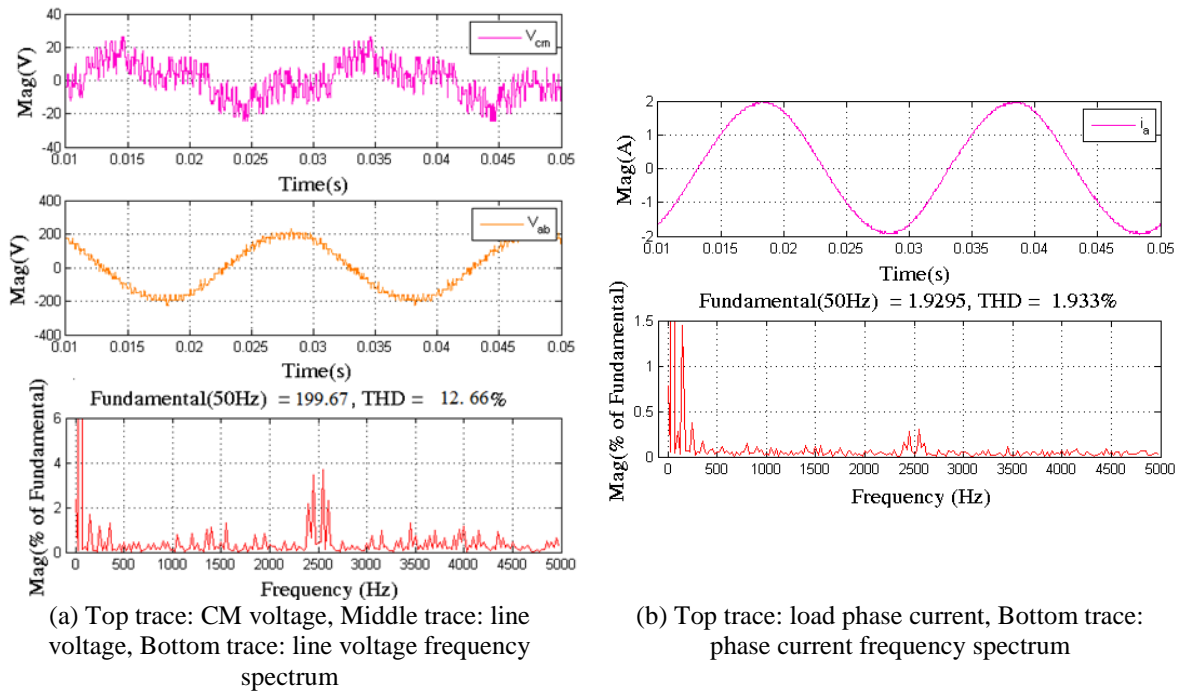


Figure 20. The line voltage and phase current frequency spectra for $E_m=1$

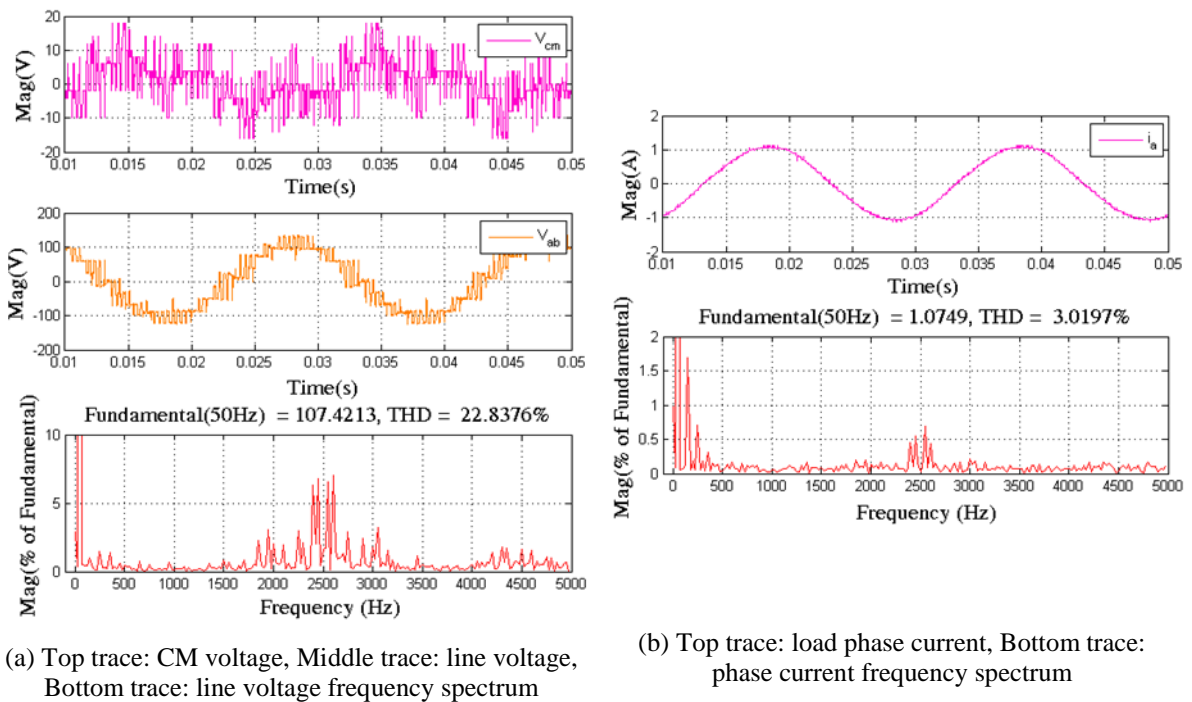


Figure 21. The line voltage and phase current frequency spectra for $E_m=0.5$

Similarly, for $E_m=0.5$, the line voltage THD is 22.8% in Figure 21(a) and the phase current THD is 3% in Figure 21(b). When $E_m=0.2$, the experiment results showed the line voltage and phase current THD values are 58.7% and 6.7% in Figure 22 respectively.

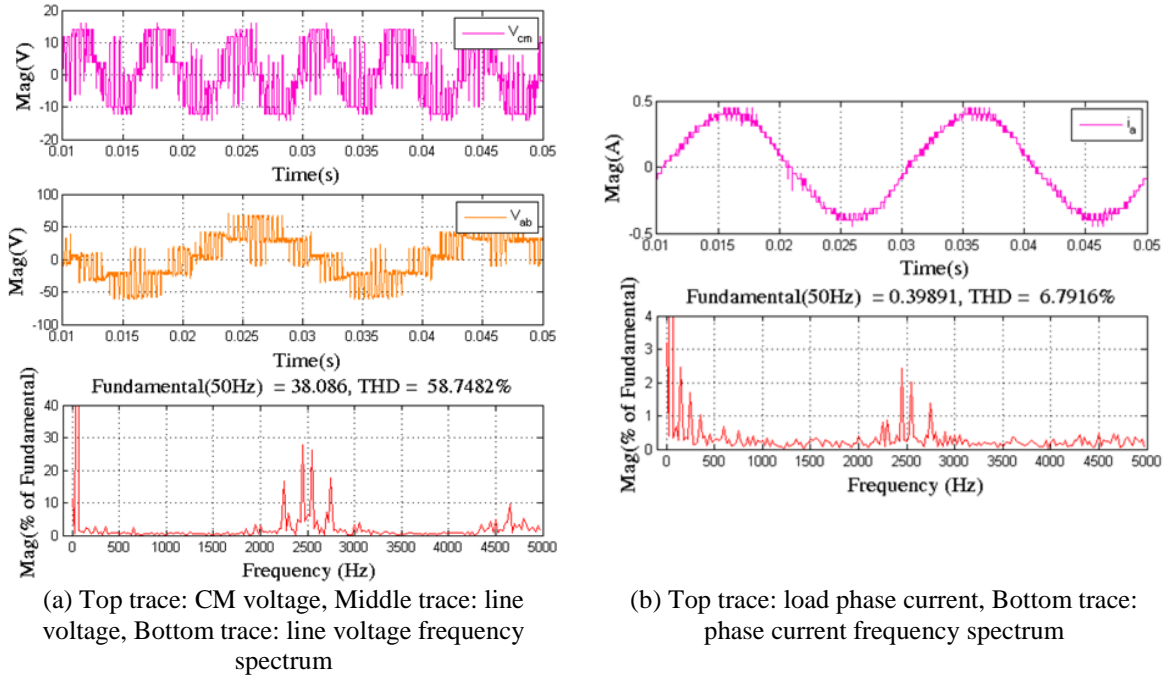


Figure 22. The line voltage and phase current frequency spectra for $E_m=0.2$

In addition, the experiment THD results in Figure 23 have also validated the performance of the PSK method equivalent to the APOD method.

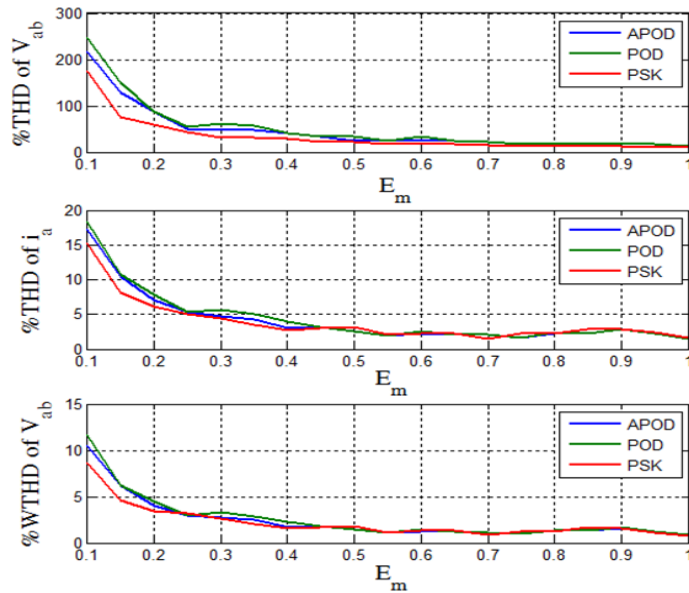


Figure 23. THD values versus E_m for experiment

5. CONCLUSION

This paper presented a method for decreasing the common mode voltage of cascaded multilevel inverters using the phase shift keying technique to modulate the phase of carrier waves. This technique also helps the cascaded multilevel inverters reduce the number of switching commutations of IGBTs when using the proposed strategy. Then, it reduces switching loss of inverters. In addition, the output voltage harmonics

are also significantly suppressed. The weighted total harmonic distortion factor (WTHD) is also considered to prove the independence from the load parameters of the proposed method. The simulation and experiment results on the cascaded 9-level 3-phase inverter system have confirmed the performance of the proposed method compared with those of the APOD and POD using unmodulated carrier waves.

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BIOGRAPHIES OF AUTHORS



Vinh-Quan Nguyen was born in Vietnam, in 1963. He received his M. E. degree in Automation from HCM city University of Technology, VNU-HCMC, Vietnam, in 2011. He had also completed his Ph. D. degree in Power systems from HCM city University of Technology, VNU-HCMC, Vietnam, in 2020. He is currently working as a lecture in Faculty of Electrical and Electronics Engineering, HCM city University of Technology and Education. His research interests are circuit design, power electronics control, and embedded systems.



Quang-Tho Tran received his M. E. degree in Electrical Engineering from HCM city University of Technology, VNU-HCMC, Vietnam, in 2003; and his Ph. D. degree in Electrical Engineering from HCM-UTE, Vietnam. He is currently working as a lecture in Faculty of Electrical and Electronics Engineering, HCM city University of Technology and Education. His research interests include electric drives, DC-AC inverters, DC-DC converters, and renewable energy conversion.