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Design of very low-voltages and high-performance CMOS gate-driven operational amplifier

Hayder Khaleel AL-Qaysi[1], Musaab Mohammed Jasim[2], Siraj Manhal Hameed[3]
[1]Department of Electronic Engineering, College of Engineering, University of Diyala, Iraq
[2,3]Department of Computer Engineering, College of Engineering, University of Diyala, Iraq

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ABSTRACT

This paper presents the description and analysis of the design and HSPICE-based simulation results of very low-voltages (LVs) power supplies and high-performance specifications CMOS gate-driven (GD) operational amplifier (Op-Amp) circuit. The very LVs CMOS GD Op-Amp circuit designed using 90nm CMOS technology parameters and the folded cascode (FC) technique employed in the differential input stage. The HSPICE simulation results demonstrate that the overall gain is 73.1dB, the unity gain bandwidth is 14.9MHz, the phase margin is 61°, the total power dissipation is 0.91mW, the output voltage swing is from -0.95V to 1V, the common-mode rejection ratio is 84.2dB, the equivalent input-referred noise voltage is $50.94\text{nV}/\sqrt{\text{Hz}}$ at 1MHz, the positive slew rate is $11.37\text{V}/\mu\text{s}$, the negative slew rate is $11.39\text{V}/\mu\text{s}$, the settling time is 137ns, the positive power-supply rejection ratio is 74.2dB, and the negative power-supply rejection ratio is 80.1dB. The comparisons of simulation results at $\pm$1V and $\pm$0.814V power supplies' voltages of the very LVs CMOS GD Op-Amp circuit demonstrate that the circuit functions with perfect performance specifications, and it is suitable for many considerable applications intended for very LVs CMOS Op-Amp circuits.

Corresponding Author:

Hayder Khaleel AL-Qaysi,
Department of Electronic Engineering,
College of Engineering,
University of Diyala,
Baqubah, Diyala, Iraq.
Email: hay.kha.82@gmail.com

1. INTRODUCTION

In recent years, the growing global electronics markets' needs for portable, wearable, wireless, battery-driven, and reliable electronics in submicron and nanometer VLSI analog and mixed-signal systems have generated the desire and opened new horizons in the field of scientific researches to design very low-voltages (LVs) power supplies and efficient low power (LP) complementary metal-oxide field-effect transistors (CMOSFETs) based analog sub-circuits [1-3]. In those systems, the threshold voltages ($V_{th,n,p}$) of the MOSFETs are not reducing compared to the rate at which the power supplies voltages reduction [4] and the ratio of lengths-to-widths of the down-scaled MOSFETs channels [5]. In very LVs power supplies and LP MOSFETs circuits, the minimum power supplies voltages must be equal to or greater than the $V_{th,n,p}$ values, and this imposes an additional strict restriction on the possibility of reducing the power supplies voltages [6].

However, Digital MOSFETs circuits benefit from the use of low-$V_{th,n,p}$ values MOSFETs and very LVs power supplies to improve their performance specifications. Whereas, the use of low-$V_{th,n,p}$ values MOSFETs and very LVs power supplies lead to the deterioration in the performance specifications of the analog MOSFETs circuits due to the effects of gate leakage currents, short-channel lengths, and permissible noise voltages margins [4-9]. Consequently, these effects increase the complexity of designing the analog

MOSFETs circuits, and the only solution to keep pace with the performance of the digital MOSFETs circuits is to choose suitable and simple analog MOSFETs circuits topologies with very LVs power supplies.

CMOS operational amplifier (Op-Amp) circuits with different topologies are the main building blocks that perform useful and multiple functions in the analog and mixed-signal integrated circuits (ICs) [10-13]. Consequently, the selection of suitable and simple design for very LVs power supplies and high-performance specifications CMOS Op-Amp circuits is very crucial because their performance specifications directly affect the overall performance specifications of the analog and mixed-signal ICs. The minimum and maximum input common-mode ($V_{in(min)}$,$V_{in(max)}$, respectively) and differential-mode range voltages in the classical CMOS gate-driven (GD) Op-Amp circuits topologies are relatively small and greatly influenced by the power supplies' voltages [14]. To overcome these shortcomings, several promising very LVs power supplies' design techniques have introduced to increase the $V_{in(min)}$ and $V_{in(max)}$ values of the very LVs power supplies and high-performance specifications CMOS Op-Amp circuits topologies. Among these design techniques, the most widely used are: parallel-connected nMOSFETs and pMOSFETs differential input pairs [15, 16], DC level-shifters MOSFETs [16-20], self-cascoded MOSFETs [17, 19], sub-$V_{th,n,p}$ region operation MOSFETs [17, 19], dynamic $V_{th,n,p}$ MOSFETs [19], floating-gate (FG) MOSFETs [17-21], quasi floating-gate (QFG) MOSFETs [18, 20, 22, 23], and bulk-driven (BD) MOSFETs [4, 17-19]. There are advantages and disadvantages to each of these very LVs power supplies' design techniques reported in [4, 15-19]. Conclusively, all of these design techniques aim to reduce the $V_{th,n,p}$ values or cancel their impacts on the performance specifications of the CMOS Op-Amp circuits topologies. Consequently, allow the CMOS Op-Amp circuits topologies to operate in the very LVs power supplies range with high-performance specifications.

In this paper, the main objective is to design simple, very LVs, and folded cascode (FC) technique-based differential input stage CMOS GD Op-Amp circuit topology capable of operating at the minimum power supplies voltages that equal the sum of three drain-source saturation voltages with high-performance specifications. Our contribution to solving this problem is by simulating and analyzing the impact of the various performance specifications of the very LVs CMOS GD Op-Amp circuit at different power supplies voltages using the HSPICE simulation program. Consequently, the results are generalized with proposals to build CMOS Op-Amp circuits that have higher performance specifications in the future. The rest of this paper is arranged as follows: The description and design performance specifications of the very LVs CMOS GD Op-Amp circuit topology are presented in Section 2. HSPICE simulation results that illustrate the obtained design performance specifications are described and analyzed in Section 3. Finally, the concluding remarks of this work and future work are drawn in Section 4.

2. VERY LVs CMOS GD OP-AMP DESCRIPTION

The selected very LVs CMOS GD Op-Amp circuit topology in this paper is shown in Figure 1 [24]. This circuit bases on the folded cascode (FC) technique in the differential input stage. The differential input stage is composed of the simple differential GD nMOSFETs pair M1 and M2 with transistors M3 and M4, which acting as balanced-active current source pMOSFETs loads. Consequently, the use of this structure in the differential input stage has a great advantage as it provides the broadest values for the input common-mode range voltages ($V_{in(min)}$ and $V_{in(max)}$, respectively) without the need to increase the complexity of the circuit by using the parallel-connected nMOSFETs and pMOSFETs differential input stages structure. The differential input stage is more susceptible than the other very LVs CMOS GD Op-Amp circuit stages to the impact of the very LV power supply, which its minimum value is determined by using (1):

$$V_{DD(min)} = V_{SD3(sat)} + V_{DS1(sat)} + V_{DS5(sat)} \quad (1)$$

where $V_{SD3(sat)}$ is the source-drain saturation voltage of transistor M3, $V_{DS1(sat)}$ and $V_{DS5(sat)}$ are the drain-source saturation voltages of transistor M1 and nMOSFET transistor M5, respectively.

If the value of positive power supply voltage (V_{DD}) is greater than $V_{DD(min)}$, then the value of $V_{in(min)}$ and $V_{in(max)}$ are determined by using (2) and (3), respectively:

$$V_{in(min)} = V_{SS} + V_{DS5(sat)} + V_{GS1} \quad (2)$$

where V_{SS} is the negative power supply voltage and V_{GS1} is the gate-source voltage of transistor M1.

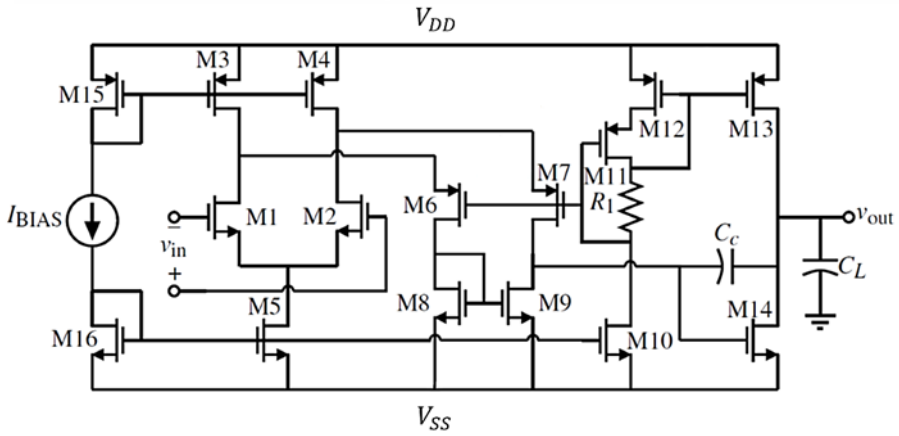


Figure 1. Topology of very LVs CMOS GD Op-Amp circuit

$$V_{in(max)} = V_{DD} - V_{SD3(sat)} + V_{th,n} \quad (3)$$

The sources of pMOSFET transistors M6 and M7 are connected to the output of differential GD nMOSFETs pair input stage. The gate-source voltages of transistors M6 and M7 (V_{GS6} and V_{GS7}, respectively) are provided by the proper selection of the resistance value R_1. Thus, the source-drain saturation voltages of the active current source pMOSFETs loads M3 and M4 are $V_{SD3,4(sat)} = V_{ON}$. This provides the maximum value for the $V_{in(max)}$ and also allows the variation in the power supply voltage without limiting the $V_{in(max)}$ value. The transistors M6 and M7 perform the process of folding the differential currents signals output from the differential GD nMOSFETs pair input stage, and then the nMOSFET transistors M8 and M9, which form the current-mirror circuit, convert these differential currents signals into single-ended current signals. The gain (A_{v1}) of the differential GD nMOSFETs pair input stage is determined by using (4):

$$A_{v1} = \frac{g_{m1}}{g_{ds7}+g_{ds9}} \quad (4)$$

where g_{m1} is the transconductance value of transistor M1, g_{ds7} and g_{ds9} are the channel conductance values of transistors M7 and M9, respectively.

The DC bias current source (I_{BIAS}), the nMOSFET transistors M16, and the transistor M5 utilized to provide a proper Dc biasing for the very LVs CMOS GD Op-Amp circuit. To guarantee that the transistor M16 and the pMOSFET transistor M15 operating in the saturation regions, they are connected as diodes. Finally, the pMOSFET transistor M13 and the nMOSFET transistor M14 are used as a simple common-source or class A output gain stage with Miller compensation capacitor (C_C) technique to increase the overall gain (A_v) and stability of the very LVs CMOS GD Op-Amp circuit. The gain (A_{v2}) of the output stage is determined by using (5):

$$A_{v2} = \frac{g_{m14}}{g_{ds13}+g_{ds14}} \quad (5)$$

where g_{m14} is the transconductance value of transistor M14, g_{ds13} and g_{ds14} are the channel conductance values of transistors M13 and M14, respectively.

Thus, the overall gain (A_v) of the very LVs CMOS GD Op-Amp circuit is determined by using (6):

$$A_v = \frac{g_{m1}.g_{m14}}{(g_{ds7}+g_{ds9}).(g_{ds7}+g_{ds9})} \quad (6)$$

Also, the total dissipated power (P_{diss}) by the very LVs CMOS GD Op-Amp circuit is determined by using (7):

$$P_{diss} = (I_{BIAS} + I_{D5} + I_{D14}).(V_{DD} + |V_{SS}|) \quad (7)$$

The key features of this very LVs CMOS GD Op-Amp circuit compared to the classical CMOS GD two-stage Op-Amp circuit include:

a) It uses lower power supplies' voltages.
b) It uses balanced-active current source loads.

The desired design performance specifications of the very LVs CMOS GD Op-Amp circuit, shown in Figure 1, are listed in Table 1. The values of all MOSFETs aspect ratios (W_i/L_i, where i =1 to 16) used in this circuit are listed in Table 2, and they calculated by the utilization of design step equations developed in the reference paper [24]. Then the obtained aspect ratios' values iteratively adjusted according to the desired design performance specifications by using the HSPICE simulator program. The values of the compensation capacitor C_C =2pF, the load capacitor C_L =10pF, the resistor R_1 =12.3KΩ, and I_{BIAS} = 20μA.

Table 1. Design performance specifications of the very LVs CMOS GD Op-Amp circuit

Performance Specifications	Desired Values
V_{DD} (V)	1
V_{SS} (V)	-1
Overall Gain (A_v) (dB)	>60
Unity Gain Bandwidth (GBW) (MHz)	≥10
Phase Margin (PM) (°)	≥60
Power Dissipation (P_{diss}) (mW)	≤1
DC Input-offset Voltage (V_{OS}) (V)	<0.3
Output Voltage Swing (V)	-1 to 1
CMRR (dB)	≥60
Slew Rate (+ve) (V/μs)	≥10
Slew Rate (−ve) (V/μs)	≥-10
Settling Time (T_S) (ns)	≤150
$V_{in(min)}$ (V)	≥-1
$V_{in(max)}$ (V)	≤1
$PSRR^+$ (dB)	≥60
$PSRR^-$ (dB)	≥60
Load Capacitance (C_L) (pF)	≥10
Resistance (R_1) (KΩ)	≥12.3

Table 2. Aspect ratios (W_i/L_i) of all MOSFETs

MOSFETs	Type	W_i/L_i (μm/μm)
M1, M2	nMOSFET	3.75/0.5
M3, M4	pMOSFET	10.05/0.5
M5	nMOSFET	30/0.5
M6, M7, M11, M12, M15	pMOSFET	6.67/0.5
M8, M9	nMOSFET	0.5/0.5
M10, M16	nMOSFET	23/0.5
M13	pMOSFET	99.03/0.5
M14	nMOSFET	12.5/0.5

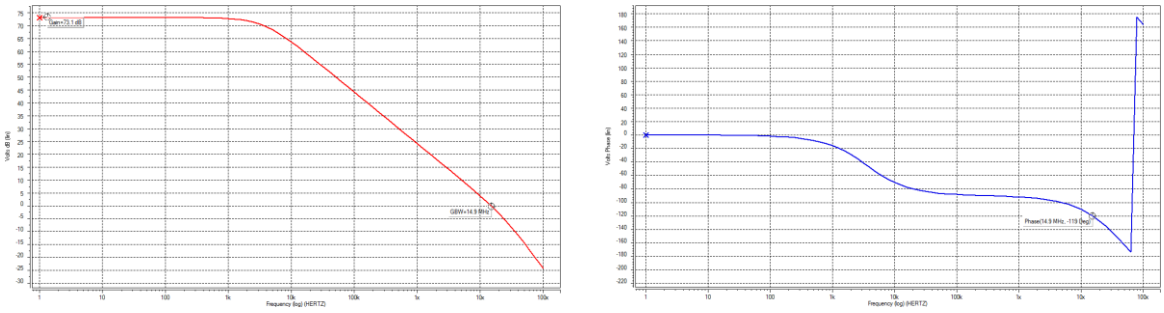
3. SIMULATION RESULTS

The very LVs CMOS GD Op-Amp circuit topology, shown in Figure 1, is designed and simulated by the HSPICE simulator environment using the BSIM4 model (Level 54) in 90nm CMOS technology process parameters. The simulation results of performance specifications plotted using Synopsys Cscope tools to validate the circuit design in the open-loop and unity-gain configurations. Besides, the relationships between varying the power supplies' voltages from ±1V to ±0.814V and the different performance specifications of the very LVs CMOS GD Op-Amp circuit investigated.

The design performance specifications of the very LVs CMOS GD Op-Amp circuit and the aspect ratios values of the utilized MOSFETs are listed in Tables 1 and 2, respectively, and $V_{th,n}$ =0.279V, $V_{th,p}$ = −0.285V, I_{BIAS} =20μA. The selected channel length value of each MOSFET transistor used in the circuit is $L_{i=1\text{ to }16}$ =0.5μm to minimize the effect of channel length modulation parameters λ_n and λ_p. The HSPICE simulation results for the very LVs CMOS GD Op-Amp circuit in the open-loop configuration determine the values of the following performance specifications: overall gain (A_v), unity gain bandwidth or gain bandwidth (GBW), phase margin (PM), total power dissipation (P_{diss}), input resistance (R_{in}), output resistance (R_{out}), DC input-offset voltage (V_{OS}), output voltage swing range, common-mode rejection ratio (CMRR), and equivalent input-referred noise (IRN) voltage.

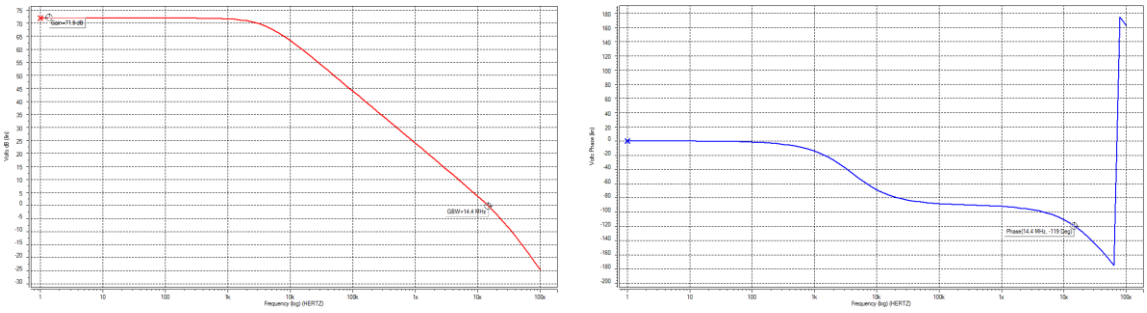
Figure 2 depicts the frequency response simulation results of the circuit at $V_{DD} = |V_{SS}|$ =1V. The results show that the achieved overall gain value (A_v) is 73.1dB, and the unity gain bandwidth value (GBW) is 14.9MHz while the phase margin value (PM) is 61°. Figure 3 depicts the frequency response simulation results of the circuit at $V_{DD} = |V_{SS}|$ =0.814V. The results show that the achieved overall gain

value (A_v) is 71.9dB, and the unity gain bandwidth value (GBW) is 14.4MHz while the phase margin value (PM) has not changed, and this means that the circuit has high stability.



(a) (b)

Figure 2. Frequency response of the circuit at $V_{DD} = |V_{SS}|$ =1V (a) overall gain (A_v). (b) phase margin (PM)



(a) (b)

Figure 3. Frequency response of the circuit at $V_{DD} = |V_{SS}|$ =0.814V (a) overall gain (A_v), (b) phase margin (PM)

The total power dissipation value (P_{diss}) of the circuit at $V_{DD} = |V_{SS}|$ =1V is 0.91mW while at $V_{DD} = |V_{SS}|$ =0.814V is found to be 0.73mW. The input and output resistance values (R_{in}) and (R_{out}) of the circuit at $V_{DD} = |V_{SS}|$ =1V are 387MΩ and 14.8KΩ, respectively, while at $V_{DD} = |V_{SS}|$ =0.814V are found to be 411MΩ and 13.9KΩ, respectively. Figure 4 depicts the simulation results of the DC input-offset voltage (V_{OS}) and the output voltage swing of the circuit at $V_{DD} = |V_{SS}|$ =1V. The results show that the achieved DC input-offset voltage value (V_{OS}) is 293mV, while the output voltage swing range is from -0.95V to 1V. Figure 5 depicts the simulation results of the DC input-offset voltage (V_{OS}) and the output voltage swing of the circuit at $V_{DD} = |V_{SS}|$ =0.814V. The results show that the achieved DC input-offset voltage value (V_{OS}) is 0.778mV, while the output voltage swing range is from -0.763V to 0.814V.

Figure 6 depicts the simulation result of the common-mode voltage gain ($A_{v,cm}$) of the circuit at $V_{DD} = |V_{SS}|$ =1V. The result shows that the achieved common-mode voltage gain value ($A_{v,cm}$) is −11.1dB. Consequently, the common-mode rejection ratio value (CMRR) of the circuit is 84.2dB. This high CMRR value means that the circuit rejects perfectly the common-mode noise signals at its output. Figure 7 depicts the simulation result of the common-mode voltage gain ($A_{v,cm}$) of the circuit at $V_{DD} = |V_{SS}|$ =0.814V. The result shows that the achieved common-mode voltage gain value ($A_{v,cm}$) is −11.9dB. Consequently, the common-mode rejection ratio value (CMRR) of the circuit is 83.8dB.

Figure 8 depicts the equivalent input-referred noise (IRN) voltage simulation result of the circuit at $V_{DD} = |V_{SS}|$ =1V. The result shows that the achieved equivalent input-referred noise voltage range values are from 55.97nV/$\sqrt{\text{Hz}}$ to 44.06nV/$\sqrt{\text{Hz}}$ over the entire unity gain bandwidth (GBW) values. Figure 9 depicts the equivalent input-referred noise (IRN) voltage simulation result of the circuit at $V_{DD} = |V_{SS}|$ =0.814V. The result shows that the achieved equivalent input-referred noise voltage range values are from 48.13nV/$\sqrt{\text{Hz}}$ to 44.75nV/$\sqrt{\text{Hz}}$ over the entire unity gain bandwidth (GBW) values. Consequently, the circuit has an excellent equivalent input-referred noise voltage performance specifications.

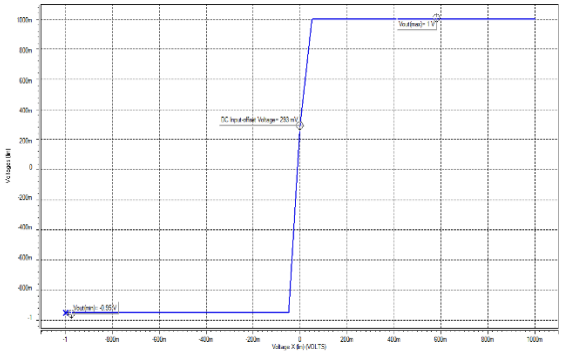


Figure 4. DC input-offset voltage (V_{OS}) and output voltage swing of the circuit at $V_{DD} = |V_{SS}| = 1V$

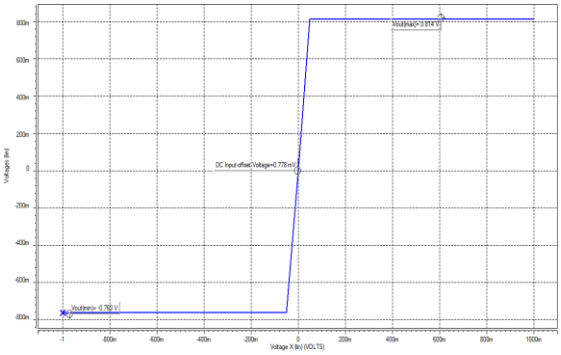


Figure 5. DC input-offset voltage (V_{OS}) and output voltage swing of the circuit at $V_{DD} = |V_{SS}| = 0.814V$

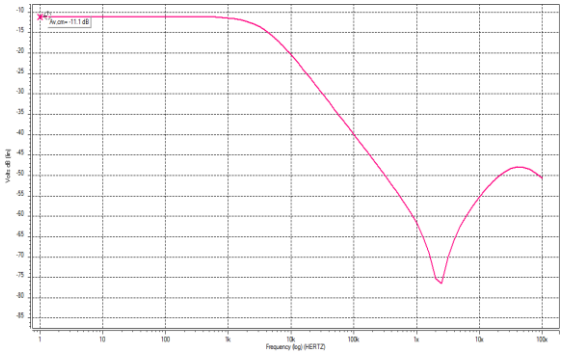


Figure 6. Common-mode voltage gain ($A_{v,cm}$) of the circuit at $V_{DD} = |V_{SS}| = 1V$

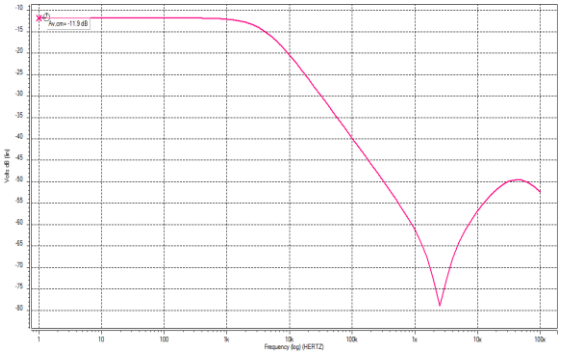


Figure 7. Common-mode voltage gain ($A_{v,cm}$) of the circuit at $V_{DD} = |V_{SS}| = 0.814V$

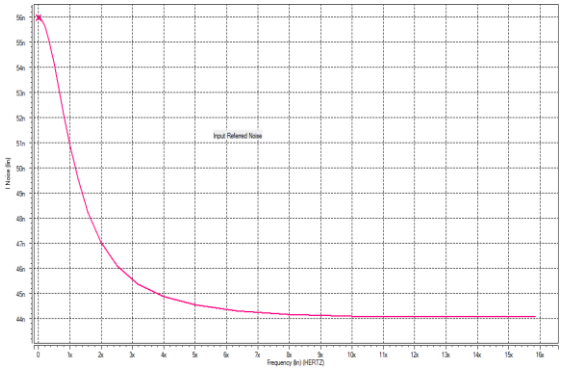


Figure 8. Equivalent input-referred noise voltage of the circuit at $V_{DD} = |V_{SS}| = 1V$

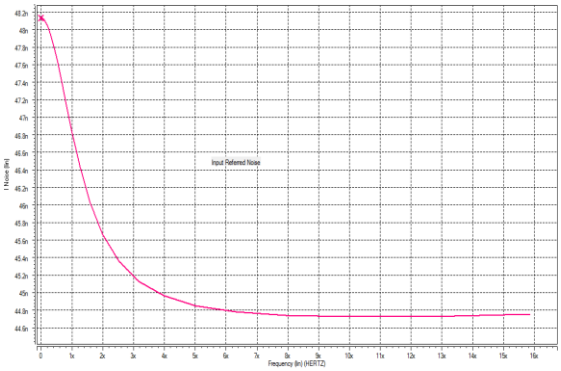


Figure 9. Equivalent input-referred noise voltage of the circuit at $V_{DD} = |V_{SS}| = 0.814V$

The HSPICE simulation results for the very LVs CMOS GD Op-Amp circuit in the unity-gain configuration determine the values of the following performance specifications: slew rates ($SR^{\pm}$), settling time (T_S), input common-mode range (ICMR) voltage, and power-supply rejection ratios ($PSRR^{\pm}$). Figure 10 depicts the slew rates ($SR^{\pm}$) and settling time (T_S) simulation results of the circuit at $V_{DD} = |V_{SS}| = 1V$. The results show that the achieved positive slew rate value (SR^{+}) is 11.37V/µs, and the negative slew rate value (SR^{-}) is 11.39V/µs, while the settling time value (T_S) is 137ns. Figure 11 depicts the slew rates ($SR^{\pm}$) and settling time (T_S) simulation results of the circuit at $V_{DD} = |V_{SS}| = 0.814V$. The results show that the achieved positive slew rate value (SR^{+}) is 11.45V/µs, and the negative slew rate value (SR^{-}) is 10.86V/µs, while the settling time value (T_S) is 86.2ns. Consequently, the circuit has high stability and fast settling time.

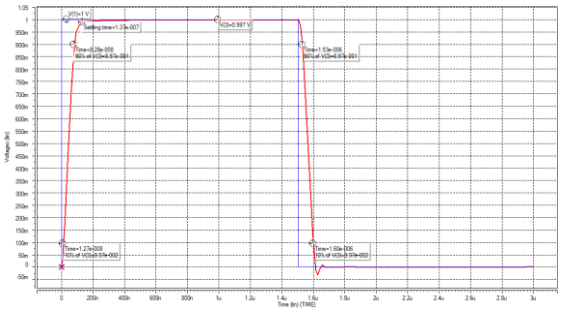


Figure 10. Slew rate (SR) and settling time (T_S) of the circuit at $V_{DD} = |V_{SS}|$ =1V

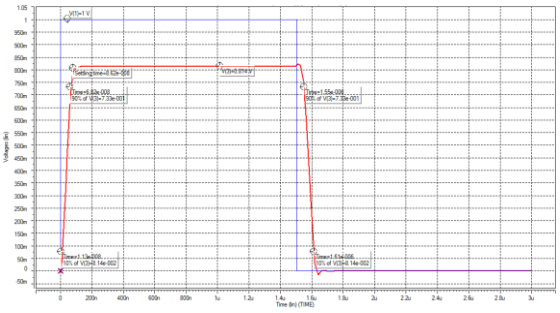


Figure 11. Slew rate (SR) and settling time (T_S) of the circuit at $V_{DD} = |V_{SS}|$ =0.814V

Figure 12 depicts the input common-mode range (ICMR) voltage simulation result of the circuit at $V_{DD} = |V_{SS}|$ =1V. The result shows that the achieved input common-mode range (ICMR) voltage value is from $V_{in(min)} = -0.484$V to $V_{in(max)}$ =1V. Figure 13 depicts the input common-mode range (ICMR) voltage simulation result of the circuit at $V_{DD} = |V_{SS}|$ =0.814V. The results show that the achieved input common-mode range (ICMR) voltage value is from $V_{in(min)} = -0.309$V to $V_{in(max)}$ =0.814V.

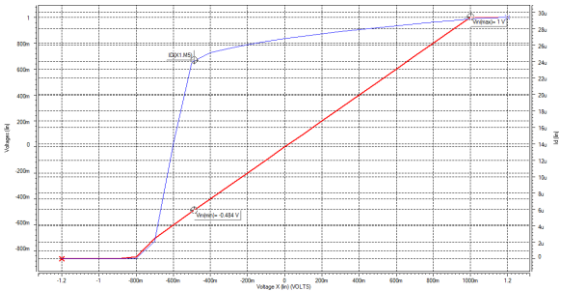


Figure 12. Input common-mode range (ICMR) voltage of the circuit at $V_{DD} = |V_{SS}|$ =1V

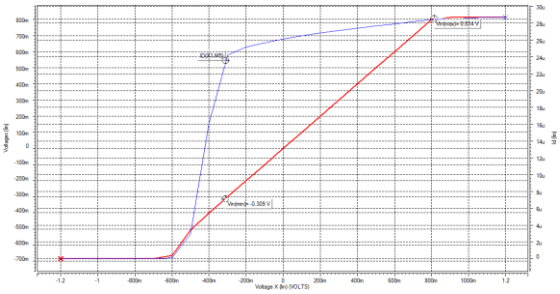
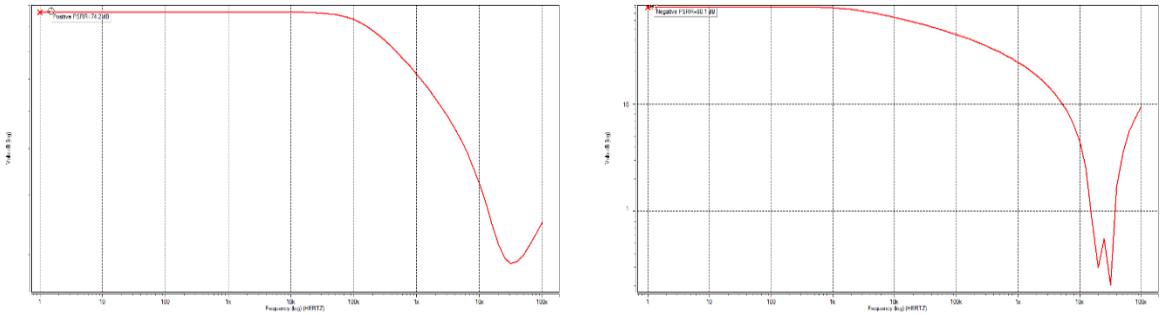


Figure 13. Input common-mode range (ICMR) voltage of the circuit at $V_{DD} = |V_{SS}|$ =0.814V

Figure 14 depicts the power-supply rejection ratios ($PSRR^{\pm}$) simulation results of the circuit at $V_{DD} = |V_{SS}|$ =1V. The results show that the achieved positive power-supply rejection ratio value ($PSRR^{+}$) is 74.2dB, and the negative power-supply rejection ratio value ($PSRR^{-}$) is 80.1dB. Figure 15 depicts the power-supply rejection ratios ($PSRR^{\pm}$) simulation results of the circuit at $V_{DD} = |V_{SS}|$ =0.814V. The results show that the achieved positive power-supply rejection ratio value ($PSRR^{+}$) is 72.3dB, and the negative power-supply rejection ratio value ($PSRR^{-}$) is 76.6dB. Consequently, the circuit has high rejections to the ripples from the power supplies voltages.

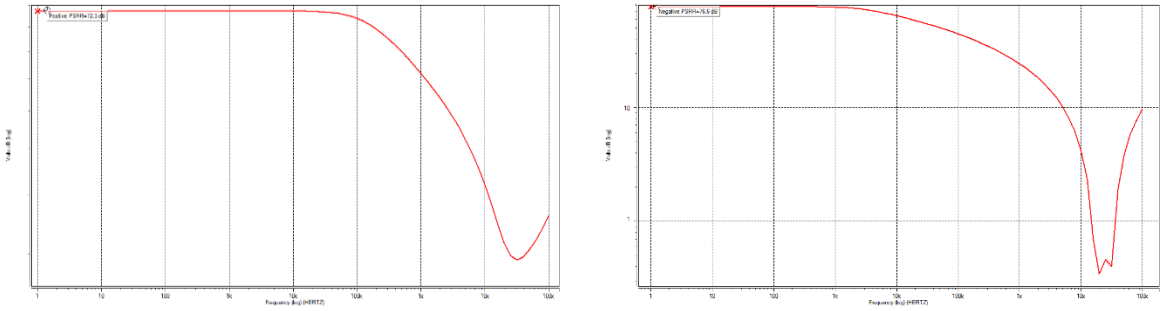
The performance specifications of the very LVs CMOS GD Op-Amp circuit at $V_{DD} = |V_{SS}|$ =1V and $V_{DD} = |V_{SS}|$ =0.814V are summarized in Table 3. It is evident from the listed simulation results in Table 3 that the values of total power dissipation (P_{diss}), DC input-offset voltage (V_{OS}), equivalent input-referred noise voltage, positive slew rate (SR^{+}), and settling time (T_S) are directly proportional to the power supplies' voltages values. Also, the values of overall gain (A_v), output voltage swing range, common-mode rejection ratio (CMRR), negative slew rate value (SR^{-}), input common-mode range voltage (ICMR), and power-supply rejection ratios ($PSRR^{\pm}$) are inversely proportional to the power supplies' voltages values. Furthermore, the value of phase margin (PM) has not changed with the variation in the power supplies' voltages values. Consequently, the P_{diss} value is improved by 19.8%, the V_{OS} value is improved by 99.7%, the average value of the equivalent IRN voltage range is improved by 71.6%, the SR^{+} value is improved by 0.7%, and the T_S value is improved by 37.1%. Also, the A_v value is decreased by 1.6%, the average value of the output voltage swing range is decreased by 19.1%, the CMRR value is decreased by 0.47%, the SR^{-} value is decreased by 4.6%, the average value of ICMR voltage is decreased by 24.3%, the $PSRR^{+}$ value is decreased by 2.5%, and the $PSRR^{-}$ value is decreased by 4.3%. Based on the preliminary results, it is evident that the very LVs CMOS GD Op-Amp circuit possesses high-performance specifications, and it has achieved the desired design performance specifications listed in Table 1 at the power supplies' voltages values $\pm$1V and $\pm$0.814V.

Furthermore, the comparisons of the performance specifications of the very LVs CMOS GD Op-Amp circuit with the other Op-Amp circuits presented in the prior papers [11, 23, 25] are summarized in Table 4. It is evident from Table 4 that the very LVs CMOS GD Op-Amp circuit presented in this paper has better performance specifications values in terms of the overall gain (A_v), unity gain bandwidth (GBW), output voltage swing which is approximately rail-to-rail swing, equivalent input-referred noise (IRN) voltage, settling time (T_S), input common-mode range (ICMR) voltage, and power-supply rejection ratios ($PSRR^{\pm}$), whereas its main drawback is it has a higher total power dissipation (P_{diss}) value.



(a) (b)

Figure 14. Power-supply rejection ratios ($PSRR^{\pm}$) of the circuit at $V_{DD} = |V_{SS}|$ =1V, (a) magnitude of $PSRR^{+}$, (b) magnitude of $PSRR^{-}$



(a) (b)

Figure 15 Power-supply rejection ratios ($PSRR^{\pm}$) of the circuit at $V_{DD} = |V_{SS}|$ =0.814V, (a) magnitude of $PSRR^{+}$, (b) magnitude of $PSRR^{-}$

Table 3. Perfomance specifications summary of the very LVs CMOS GD Op-Amp circuit at $V_{DD} = |V_{SS}|$ =1V and at $V_{DD} = |V_{SS}|$ =0.814V

Performance Specifications	Values at $V_{DD} = \|V_{SS}\|$ =1V	Values at $V_{DD} = \|V_{SS}\|$ =0.814V
Overall Gain (A_v) (dB)	73.1	71.9
Unity Gain Bandwidth (GBW) (MHz)	14.9	14.4
Phase Margin (PM) (°)	61	61
Power Dissipation (P_{diss}) (mW)	0.91	0.73
Input Resistance (R_{in}) (MΩ)	387	411
Output Resistance (R_{out}) (KΩ)	14.8	13.9
DC Input-offset Voltage (V_{OS}) (mV)	293	0.778
Output Voltage Swing (V)	-0.95 to 1	-0.763 to 0.814
CMRR (dB)	84.2	83.8
Eq. IRN voltage (nV/$\sqrt{\text{Hz}}$)	55.97 to 44.06	48.13 to 44.75
Slew Rate (+ve) (V/µs)	11.37	11.45
Slew Rate (-ve) (V/µs)	11.39	10.86
Settling Time (T_S) (ns)	137	86.2
$V_{in(min)}$ (V)	-0.484	-0.309
$V_{in(max)}$ (V)	1	0.814
$PSRR^{+}$ (dB)	74.2	72.3
$PSRR^{-}$ (dB)	80.1	76.6
Load Capacitance (C_L) (pF)	10	10
Resistance (R_1) (KΩ)	12.3	12.3

Table 4. Performance specifications comparisons of the Op-Amp circuits

Performance Specifications	This paper	[11]	[23]	[25]
CMOS Technology (nm)	90	180	500	350
Power Supply Voltage (V)	± 1	1.8	± 1	± 2
Overall Gain (A_v) (dB)	73.1	72.04	61.5	72
Unity Gain Bandwidth (GBW) (MHz)	14.9	13.33	2.31	12.64
Phase Margin (PM) (°)	61	62.46	89	65.8
Power Dissipation (P_{diss}) (mW)	0.91	0.13	0.24	-
Output Voltage Swing (V)	-0.95 to 1	-	-	0.1106 to 1.996
CMRR (dB)	84.2	-	90	-
Eq. IRN voltage ($nV/\sqrt{Hz}$)	50.94@1MHz	-	93@1MHz	-
Slew Rate (+ve) ($V/\mu s$)	11.37	11.63	3.4	20
Slew Rate ($-$ve) ($V/\mu s$)	11.39	-	-	-
Settling Time (T_s) (ns)	137	-	-	-
$V_{in(min)}$ (V)	-0.484	-	-	0.509
$V_{in(max)}$ (V)	1	-	-	1.511
$PSRR^+$ (dB)	74.2	72.09	51	-
$PSRR^-$ (dB)	80.1	-	50	-
Load Capacitance (C_L) (pF)	10	2	25	11.5

4. CONCLUSION AND FUTURE WORK

In this paper, a simple and very LVs CMOS GD Op-Amp circuit has been designed by using 90nm CMOS technology process parameters. The folded cascode (FC) technique is used in the differential input stage to meet the requirement of operation under the conditions of very LVs power supplies. The achieved HSPICE-based simulation results at ± 1V and ± 0.814V power supplies' voltages demonstrate the validity of the designed very LVs CMOS GD Op-Amp circuit operation with high-performance specifications. Consequently, the very LVs CMOS GD Op-Amp circuit is very suitable for growing global electronics markets' needs for very LVs submicron and nanometer VLSI analog and mixed-signal systems.

In the future, the work should focus on minimizing further the positive and negative power supply voltages values (V_{DD}, V_{SS}, respectively) by reducing the threshold voltages values ($V_{th,n,p}$) through the use of differential BD nMOSFET transistors pair M1 and M2 and the use of balanced BD pMOSFET active current source loads transistors M3 and M4 in the differential input stage. Thus, allowing the designed very LVs CMOS GD Op-Amp circuit in this paper to operate in the range of ultra low voltage (ULV) power supplies. Furthermore, using a suitable DC level-shifters MOSFETs technique can maximize further the values of ICMR voltages without the need to increase the complexity of the designed very LVs CMOS GD Op-Amp circuit. Finally, the total power dissipation (P_{diss}) value of the designed very LVs CMOS GD Op-Amp circuit can be minimized further through the use of MOSFET transistor to achieve proper gate-source biasing voltages (V_{GS}) of pMOSFET transistors M6 and M7 instead of using the resistor R_1.

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BIOGRAPHIES OF AUTHOR

Hayder Khaleel AL-Qaysi received a bachelor's degree in electronic engineering from College of Engineering, University of Diyala, Iraq in 2004 and received a master's degree in electronic and communication engineering from Yildiz Technical University, Turkey, in 2017. Area of research interests in the electronic circuits design, signal processing, semiconductor technology, and VLSI analog and mixed-signal systems design. He is currently work as an assistant lecturer at College of Engineering, University of Diyala, Iraq. He has 2 published papers.

Musaab Mohammed Jasim received a bachelor's degree in computer engineering from College of Engineering, University of Diyala, Iraq, in 2007 and received a master's degree in computer engineering from Yildiz Technical University, Turkey in 2017. Area of research interests in the computer networks, signal processing, and image processing. He is currently work as an assistant lecturer at College of Engineering, University of Diyala, Iraq. He has 1 published paper.

Siraj Manhal Hameed was born in Diyala, Iraq, in 1981, received his B.Sc from University of Diyala Iraq in 2004, MSc from University of Technology Baghdad Iraq in 2014. He is currently assistant lecturer at the Department of computer Engineering, College of Engineering, University of Diyala Iraq. His current research interests are power system modeling, renewable energy, Electrical drives. He is teaching several basic subjects of the computer engineering, University of Diyala, Iraq. He has 3 published papers.