

## Fabrication of Plane Transient Diode

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### Abstract

The fabrication of horizontal structure and vertical structure is proposed based on the parameters of the transient diode, theory is combined with practice in the progress of design, the picture of structural parameters is charted in this paper, establishes the foundation for making the transient diode with reliability. Transient diode horizontal structure design<sup>1</sup> is an important element in the design. The mission is based on the request of parameters, selecting the planar geometry of the die and its dimensions. For planar diode, the geometry of die plane is determined by lithography. The design of the transverse structure is the design of the lithographic version of the graphical structure. The area of the base region of the buried layer is known based on the design rules. Buried layer area can roughly calculated, it should be greater than the area of the diffusion of base region and less than the area of the chip. Its width to cross above the width of the base region and the opening of the lead hole, i.e.

**Keywords:** transient diode, horizontal structure, vertical structure

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### 1. Introduction

To design specifications PPP = 20W; to POP 150mw; VRWM = 5V; VF = 0.75V plane transient diode physical constants (structural paramaters) can be calculated by theoretical analysis as follows: Breakdown voltage  $V_{BR} = 6.25V$ ; maximum clamping the voltage  $V_{CMAX} = 8.125V$ ; peak current:  $I_{PP} \approx 2.462(A)$ ; resistivity of the epitaxial layer; width of the space charge region:  $x_m = 2.012 \times 10^{-5} cm = 0.2012 \mu m$ ; chip area A = 0.3mm<sup>2</sup>.

### 2. Research and Method

#### 2.1. The Horizontal Structural Design

Transient diode horizontal structure design [1] is an important element in the design, the mission is based on the request of parameters, selecting the planar geometry of the die and its dimensions. For planar diode, the geometry of die plane is determined by lithography. The design of the transverse structure is the design of the lithographic version of the graphical structure. The merits of the structure in the design will directly affect the reliability and yield of the diode.

Table 1. The Size of the Reference Layout

Design size	Design smallest size (μm)
the line width of the window	10*10
Line width	10
the width of the line of separation	8
buried layer to the isolation area	30
the buried layer to the base region to the isolation region	16
Lead hole of N to isolation	30
Lead hole to the boundary of buried layer	2
Scribing strip width	60
Metal strip width and spacing	10
Pads	100*100

Transverse plane transient diodes parameters [2] are: the chip area, the area of the base region (B zone) area, the buried layer, the width of isolated holes, the lateral diffusion depth, aluminum anti engraved area, the passivation layer area [3], and the like. To be designed according to the size of the reference layout (as shown in Table 1):

## 2.2. (B zone) Area of the Base Diffused Region of the PN Junction

Through a formula based on the practical experience:

$$P_{OP} = I_F \times V_F \Rightarrow I_F = \frac{P_{OP}}{V_F} = \frac{150 \text{ mW}}{0.75 \text{ V}} = 200 \text{ mA} \quad (1)$$

1mm<sup>2</sup> area can flow through the current by 3A, the diffusion-based zone area of 200mA current, quiring the PN junction can roughly estimated by the formula [4]:

$$\frac{1}{3} = \frac{A}{0.2} \quad (2)$$

It is calculated  $A = 0.067\text{mm}^2$ , so that you get the diffusion area of the base region. It can be made bigger in the layout design. Its territory is shown in Figure 1, the green part is the base area, the mesh dicing groove is outside the green part [5].

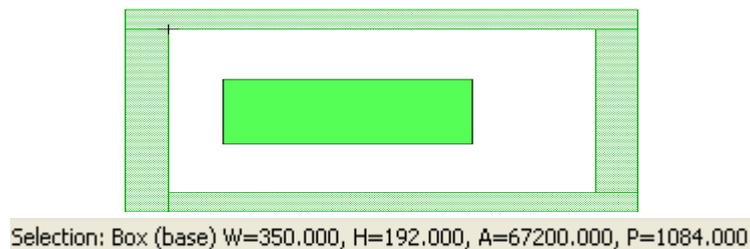


Figure 1. The Base Region

## 2.3. Buried Layer Area

The area of the base region of the buried layer [6] is known based on the design rules. Buried layer area can roughly calculated [7], it should be greater than the area of the diffusion of base region and less than the area of the chip. Its width is cross above the width of the base region and the opening of the lead hole, i.e. The area is greater than the area of the base region and the area of the hole and the buried layer. Its territory is shown in Figure 2, the blue is the area of the buried layer [8].

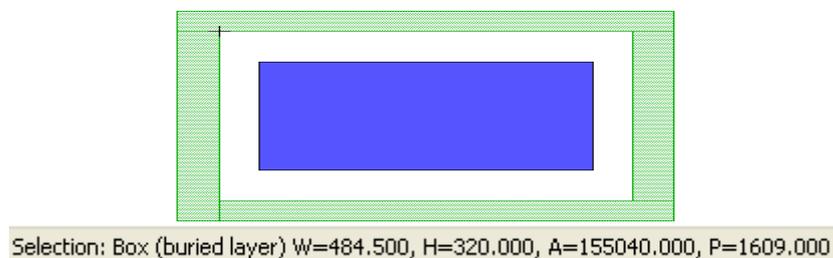


Figure 2. The Mask of Buried layer

## 2.4. The Width of the Isolated Holes

The minimum value of the width of the line of separation of design is 8 microns based on the design rules [9]; we select 10 microns, Figure 3 : red part is the isolation of the territory.

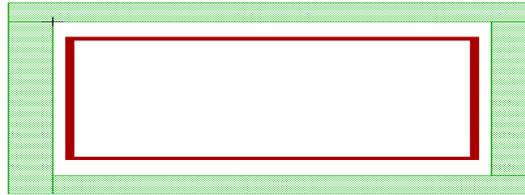


Figure 3. The Mask of Isolated Hole

### 2.5. The Area of the Lead Hole

In accordance with the requirements of the layout design rules, the width minimum we take the lead hole width minimum is 10\*10 micron [10]. In general the actual requirements can take bigger. Black in Figure 4 is the lead hole the size of the territory.

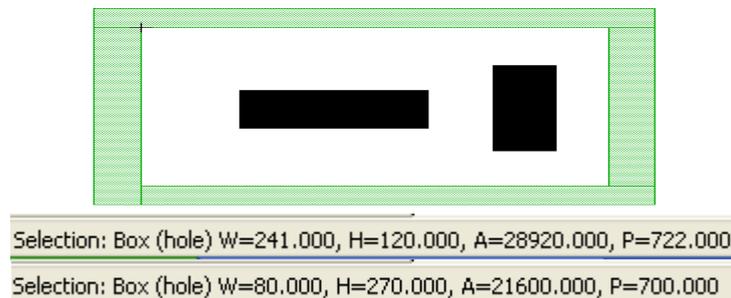


Figure 4. The Mask of Lead Hole

### 2.6. Lateral Diffusion Depth

When the diffusion of the base region happen, in addition to the longitudinal diffusion, the lateral diffusion exists [11], lateral diffusion depth is about 0.8 times than the longitudinal diffusion, the diffusion impurity concentration is substantially the same with the longitudinal direction.

### 2.7. The Area of Anti-carved Aluminum

When base region diffusion has been finished, the lead hole open, silicon above aluminum has been steamed, then the silicon surface is covered with by aluminum that we just need to retain aluminum in the place where the lead holes is around the place. So we conducted the aluminum anti engraved process. The territory of the aluminum anti carved we need has been made according to the rules, generally keeping the aluminum area greater than the area of the base area a little better. This avoids the effects of external disturbance on the contact of aluminum with the base region. Each boundary multiple than the base region of 5-6 microns. Its layout is shown in Figure 5 slash programs is the aluminum anti engraved area.

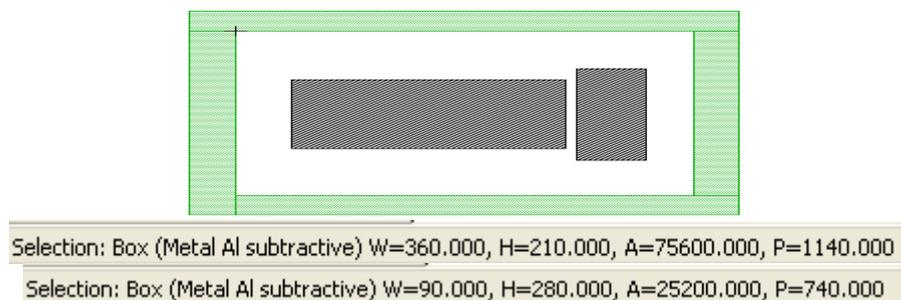


Figure 5. The Mask of Anti-engraved Aluminum

## 2.8. Passivation Layer Area

In order to avoid the influence by the surrounding atmosphere, and other external factors on the performance of the devices, a layer of protective film has been sealed in a special airtight. The process where the protective film has been formed and which overcome the surface defects has been known as surface passivation process. The masking version of the passivation is the same as the aluminum anti engraved masking version. Sometimes it is slightly larger than aluminum anti engraved area [12].

In addition, when the territory in the painting, in addition to a number of factors to be considered above, and the dicing groove width has been considered, the dicing groove minimum width is 60 microns, in accordance with the requirements of the design rules, the value has been selected in the general. The layout is shown in Figure 6, which part is passivated light blue area. In addition the factor above is to be considered, the dicing groove width has also been considered, the least width of the dicing groove width is 60mm. In general, the value is favorable.

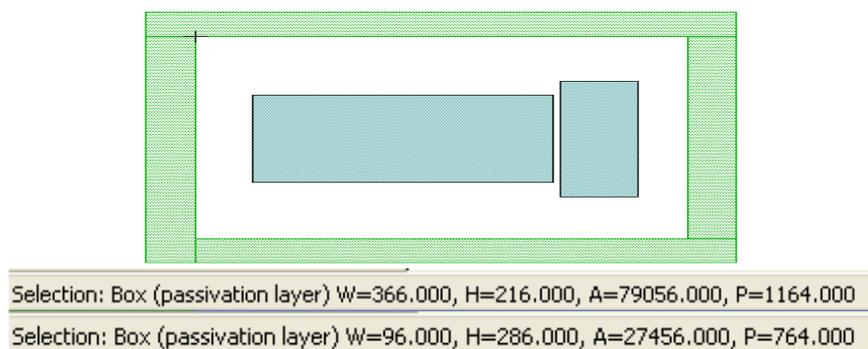


Figure 6. The Mask of Passivation

## 3. Results and Analysis

According to the indicators of the design of the plane transient diode, and combining with the main design parameters of transverse structure, we get the plane layout of the transient diode as shown in Figure 7.

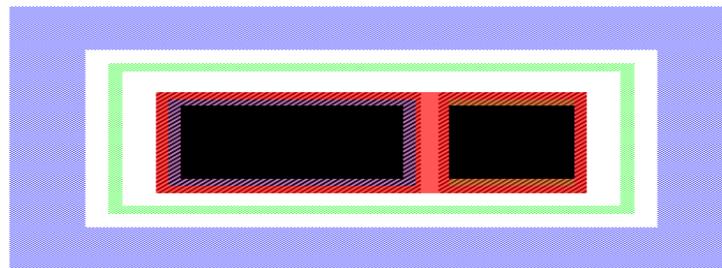


Figure 7. The Plane Layout of Transient Diode

## 4. Conclusion

By the above structure design, the qualified transient diode chip is fabricated in Gui Zhou Province Key Laboratory of micro/Nano Electronics and software by the planar process of silicon wafer cleaning, extension, oxidation, diffusion, lithography, electrode lead preparation. This work is supported partly by the key support discipline of Guizhou province No. ([2011] 275) and Zun yi city, Gui zhou, Province, application technology research and development projects (Compliance Division of Lloyd [2011]No.7).

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