The Application of the Sub-filters of the Polyphase Filter in Channel Emulator

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Abstract
This paper first gave a brief introduction of communication channel models, and then describes the characteristics of the channel emulator. According to the characteristics of the channel model, multipath is a difficult problem for hardware implementation. In order to simplify the hardware, the polyphase filter can be used for multi-path delay. Then the paper reviews the polyphase filter in the decimation and interpolation application, and simply introduces the multi-rate system. And then through the simulation experiments, the characteristics of the sub-filter of the polyphase filter were analyzed. Finally, according to the characteristics of the sub-filter, this paper presents an application in multipath delay.

Keywords: polyphase filter, channel emulator, sub-filters, multi-path delay, FPGA

1. Introduction

On the stage of the design of communication systems, planning of communications network and developing new transceiver device, analysis and simulation need to be performed on the communication channel characteristics. In order to get true and reliable channel characteristics, the researcher needs a large number of measurements and experiments, and this test method consumes huge funds, requires complex test systems, and wastes time. For example, the testing of the satellite communication channel, only a small number of organizations such like NASA could afford. In the early of the equipment development, due to the technical immaturity and the equipment instability, it is not feasible for satellite carrying equipment to analyze the channel. Under laboratory conditions, research could use mathematical analysis for the channel model, and then simulate the mathematical model with software. Good mathematical model can accurately simulate the communication channel characteristics, and there are a lot of researches on the channel model.

Three types of mathematical models are used to describe the channel, the empirical model, the probability distribution model and the geometric model. The empirical model could not explain the physical progress of the propagation, but can describe the sensitivity of important parameters; well the probability distribution model make us easier to understand the communication process, and take simplifying assumptions for the actual situation; geometric model using geometric analysis method to predict the result of single or multiple scattering source, and to explain the mechanism of decline, but hard to expand the result to the real situation. For most classic models, empirical model and probability distribution model were combined to form a new model with statistical proximity.

The channel simulation model can accurately simulate channel characteristics, but because of the excessive computing and common communication interface, resulting in a separate computer is unable to complete the simulation of real-time channel, well because of the excessive computing and no universal communication interface, the computer could not analog channel in real-time. To achieve the real-time simulation of the channel characteristics, the engineer usually use the computer with the channel emulator. The channel simulator is a cost-controllable device which could analog the channel characteristics precisely and repeatedly.

Considering the diversity of channel models, in order to achieve a variety of models on the same platform, we must identify the commonalities among the different channel models.

Through analysis, the most of the channel model focus on three key, the Doppler shift, the multipath fading and white Gaussian noise. As shown in Figure 1.
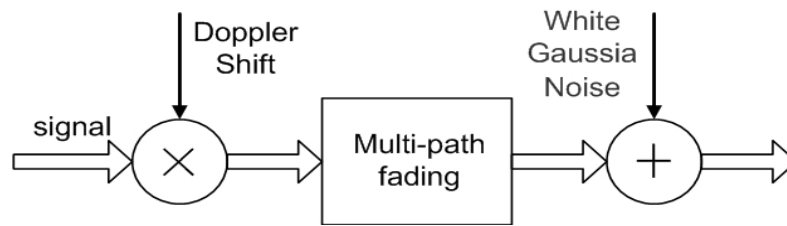

Figure 1. Common Model for Communication Channel

The multi-path fading is to describe the phenomenon that the signals reach the receiver through direct path, reflection path, and refraction path and so on. For the multi-path parameters, the multi-path delay is an important one, which describes the difference among the times of the signal reaches the receiver via different paths. Typically, in order to achieve the multi-path delay, channel emulator must have a huge cache for the signal. That requires the processor has a high-speed processing speed and a lot of storage space.

In order to simplify the design, a simple review for the structure of the polyphase filter will be given. Then we will analyze the characteristics of the sub-filters, and finally an application of the sub-filters in the multi-path delay will be given.

2. The Structure of Polyphase Filters

For multi-rate signal processing systems, two of the most important concepts are the decimation and the interpolation. However, the basic decimation and interpolation operation, requires that the processor is able to achieve a very high operation speed, This is mainly because of the low pass filter of the decimator $H_{LP}(e^{jw})$ is located in front of the decimation operator ↓ D, that is, the low pass filter is implemented before the deceleration; while for the interpolator, the low-pass filter $H_{LP}(e^{jw})$ is located after an interpolation operator ↑ I, that is, low interpolator-pass filter is carried out after the acceleration. In short, whether the decimation or the interpolation, its digital anti-aliasing filtering are carried out under the conditions of high-speed sampling rate. This will no doubt greatly improve the operational speed, and bad for the real-time process, as shown in Figure 2.
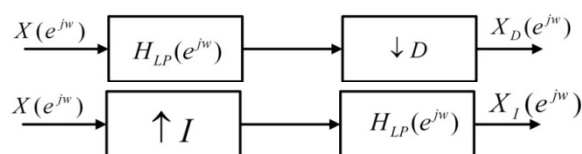

Figure 2. Decimation and Interpolation

Then introduce the basic polyphase filter structure, it is assumed that the digital filter shock response is h (n), then the Z-transform H (z) defined as:

$$H(z)^n = \sum_{n=0}^{+\infty} h(n)z^{-n}$$

(1)

Expanding the summation formula then we got:

$$H(z) = \sum_{k=0}^{D-1} z^{-K} \left[\sum_{n=-\infty}^{+\infty} h(nD+K) \cdot (z^D)^{-n} \right] \tag{2}$$

The above formula is the polyphase filter structure, and the network diagram is shown as Figure 3. Applied to the decimation and noted that the equivalent relationship, the polyphase filter structure can be obtained as shown in Figure 4.
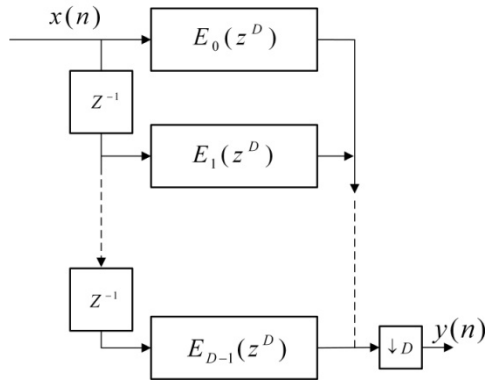

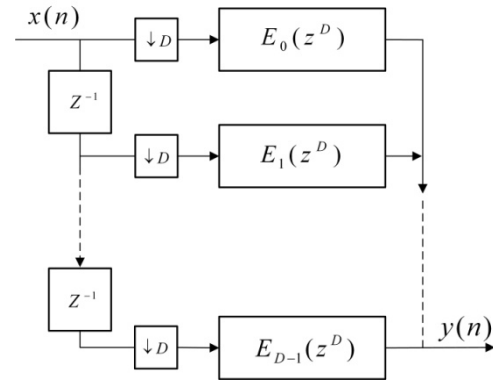Figure 3. The Polyphase Structure of the Digital Filter (Decimation)

Figure 4. The Polyphase Structure of the Decimator

Seen from the figure, the digital filter in this case is located after the decimator, thus greatly reducing the requirements on the speed of the processor and improving the real-time processing capability.

Similarly, we can give another expression of the polyphase filter structure suitable for the interpolator:

$$H(z) = \sum_{n=0}^{I-1} z^{-(I-1-K)} \cdot R_K(z^I) \tag{3}$$

$$R_K(z^I) = E_{(I-1-K)}(z^I) \tag{4}$$

Seen from the Equation (3) and Equation (4), the digital filter located before the interpolator ↑ I, which means that the digital filter is located before speed up.

3. The Characteristics of the Sub-filters of the Polyphase Filter

The name of polyphase filter, mainly because of the polyphase filtering process formula divided the system function H (z) into a set of sub-filters. And the only difference between the sub-filters is their phase response. Here we focus on the characteristics of the sub-filters.

For simple and clear, it is assumed that the original input signal is 100KHz sine wave, the original sampling rate is 1.5625MHz, assuming the application needs to signal 64 times interpolation signal data rate of 100MHz. In order to achieve good harmonic suppression needs, we select 1024 order equiripple FIR low-pass filter, the passband is 8KHz,and the stop frequency is16000Hz.As shown in Figure 5.

According polyphase filter structure, then the above filter will be divided into 64 sub-filters, respectively: $h_0, h_1, h_2 \ldots h_{63}$.

$$h_0[k] = \left[h[0], h[64], h[128] \cdots h[960] \right]$$

$$h_1[k] = \left[h[1], h[65], h[129] \cdots h[961] \right]$$

(5)

$$h_2[k] = \left[h[2], h[66], h[130] \cdots h[962] \right]$$

$$\vdots$$

$$h_{63}[k] = \left[h[63], h[127], h[191] \cdots h[1023] \right]$$

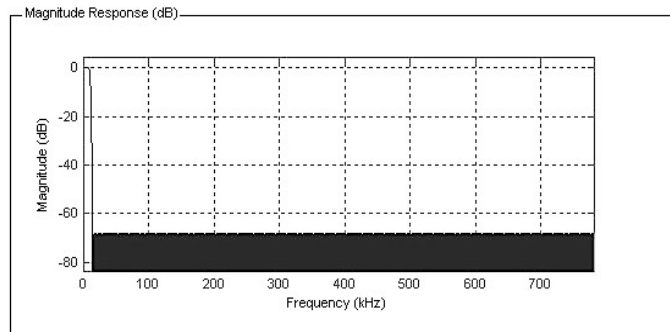The relationship between the sub-filters will be compared soon.

Figure 5. Frequence Response of the Equiripple FIR Low-pass Filter

Here, we have chosen the three sub-filters for demonstration, a 100KHz sine wave go through h_0, h_{19}, h_{63} respectively. Drawing the result with 1.5625MHz sampling rate, that is, the time resolution is 640ns, then we got:
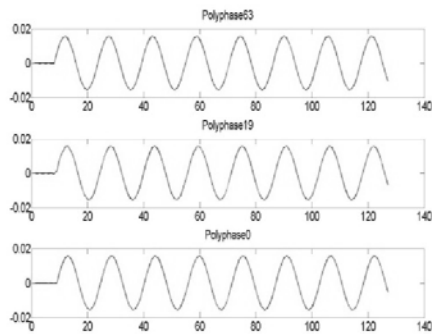

Figure 6. Sine Wave goes through the Sub-filter (640ns Time Resolution)
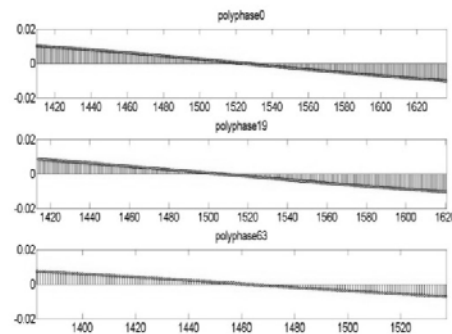

Figure 7. Sine Wave goes through the Sub-filter (10ns Time Resolution)

As shown in Figure 6, when the time resolution of 640ns, we could not tell the difference between the three groups filter what is the difference between the original signal affect the phase and frequency consistent. If we are 64 times the signal interpolation processing, the sampling rates up to 100MHz, which is the time resolution of 10ns, and then we can get the following results.

Next, pay attention the position of the second Zero-crossing point for each signal. From Figure 7, we can obtain that the position of the zero-crossing point through the filter h_0 is 1525, the position of the zero-crossing point through the filter h_{19} is, and the position of the zero-crossing point through the filter h_{63} is 1462. Similarly, all the 64 sub-filters were tested; we can

find that each sub-filter delay one sampling point compared with the previous sub-filter. Therefore, we can get the following conclusion, between the sub-filters, the frequency response and the amplitude response are the same, and the only difference between them is the phase response. Based on the characteristics of the sub-filter, we can simplify the design in some applications. Next we will give an example of polyphase filter bank to achieve the multipath delay.

4. Application of the Sub-filters in Multi-path Delay

Channel model, especially complex urban environment, need to use the multipath to describe signal reach the receiver through direct path, reflection path, and refraction path and so on. For the multipath parameters, the multi-path delay is an important one, which describes the difference among the times of the signal reaches the receiver via different paths. Typically, in order to achieve the multi-path delay, channel emulator must have a huge cache for the signal. That requires the processor has a high-speed processing speed and a lot of storage space.

For example, the International Telecommunication Union ITU has developed a series of standard channel, in where a channel model called cost207BUx12alt which describes to the Bad Urban Environment. This channel has 12 paths, first road no delay, the second delay of 10ns, and the 12 path delays 100ms.

In order to meet the resolved minimum delay of 10ns, the sampling rate of the signal of the baseband signal is at least 100MHz, the signal processing clock of the channel emulator is at least about to reach 200MHz to achieve the parallel processing, meanwhile, to store more than 100 microseconds baseband data (assuming that the I/ Q dual-way are all 16bits) it requires at least 320K memory space. If the baseband signal bandwidth is much smaller than 100MHz, such as 2MHz, then the 100MHz processing speed is a big waste for the processing resources, if Using FPGA chip implementation of signal processing, and finally integrated out the Fmax there may not be sufficient.

To minimize the overhead of resources and to reduce processing speed, we can use the following methods to implement the channel simulation.
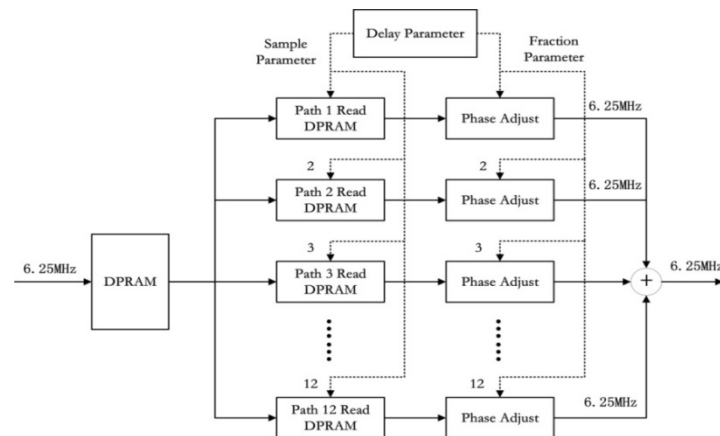

Figure 8. Structure of the Sample Delay and the Fraction Delay

First, considering to the constitution of the polyphase filter, the original 100MHz low-pass filter is divided into 16 sub-filters. According to the description of the above section, the processing speed of the baseband signal requires only 6.25MHz, and the storage space of the signal requires only 20KB, The 6.25MHz also meet the 4Mhz Nyquist frequency. For the implementation process, the delay is divided into two parts, the sample point delay and the fractional delay. Sample point delay is to select the position of the read signal based on sample point interval; the interval between the two samples is 160ns. Fractional delay is by selecting the

sub-filter, to achieve the purpose of adjusting the phase, so that the signal units precise value to 10ns.

5. Conclusion

By the above method, we can reduce the work clock by 16 times, and saving the baseband signal storage space greatly, improving the stability of processor. This method, which also can be applied to digital receiver synchronization operation, can greatly reduce the receiver processing work load, improve the precision of the synchronization operation.

Acknowledgements

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