Indonesian Journal of Electrical Engineering and Computer Science
Vol. 19, No. 1, July 2020, pp. 171~177
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v19.i1.pp171-177

Design of 130nm RFCMOS differential low noise amplifier

Maizan Muhamad[1], Hanim Hussin[2], Norhayati Soin[3]
[1,2]Faculty of Electrical Engineering, Universiti Teknologi MARA, Malaysia
[3]Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Malaysia

Article Info

Article history:

Received Nov 11, 2019
Revised Feb 1, 2020
Accepted Feb 13, 2020

Keywords:

CMOS
Differential
Low noise amplifier (LNA)
Noise figure (NF)

ABSTRACT

In this paper, an inductively degenerated CMOS differential low noise amplifier circuit topology is presented. This low noise amplifier is intended to be used for wireless LAN application. The differential low noise amplifier proposed provide high gain, low noise and large superior out of band IIP3. The LNA is designed in 130 nm CMOS technology. Simulated results of gain and NF at 2.4GHz are 20.46 dB and 2.59 dB, respectively. While the simulated S11 and S22 are −11.18 dB and −9.49 dB, respectively. The IIP3 is −9.05 dBm. The LNA consumes 3.4 mW power from 1.2V supply.

Corresponding Author:

Maizan Muhamad,
Faculty of Electrical Engineering, Universiti Teknologi MARA,
40450, ShahAlam, Malaysia.
Email: maizan@uitm.edu.my

1. INTRODUCTION

Nowadays the wireless communication demand is increasing due to the development of technology. A wireless system comprises of a back-end and front-end section. Analog signal is being process in the front-end section in the high radio frequency. While analog and digital signal is processed at the back-end section in baseband of low frequency range. Radio frequency (RF) refers to the frequency range in the electromagnetic spectrum that is used for radio communications [1] . Typically, the frequency lies from 100 kHz to 100 GHz. In general baseband frequency is below 1 GHz while those bigger than 1 GHz describes as RF. The mainstay of radio frequency communication receiver is the Low Noise Amplifier (LNA). Low noise amplifier which is in the RF front-end circuit has the great value in this field [2]. It main purpose is to provide gain while preserving the input signal-to-noise ratio of the output which is important characteristic because the receiver signals usually weak [3, 4]. Besides that, the characteristic of good LNA is shown in Figure 1.

There are many topologies in the LNA which are series shunt feedback, resistive termination, common gate connection and inductive degeneration. In LNA circuit architecture, inductively degenerated common source is the most used topology as the ability of good input impedance matching. Due to the basic topology of the inductively degenerated cascode LNA it is chosen to be implement to most of varsities of presently available of LNA. It allow maximum gain under low power constraint [5-7].

This paper present a design of 2.4 GHz RFMOS Differential LNA which is used to improve performance of differential LNA. The aim of this paper is to provide differential LNA that have low power consumption but still have acceptable performance of noise, linearity that acceptable and high range of dynamic.

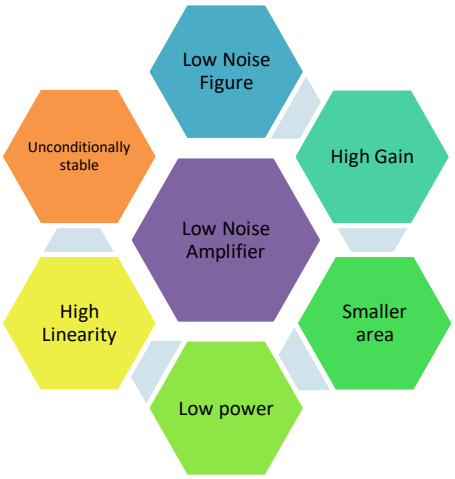

Figure 1. Characteristics of low noise amplifier

2. RESEARCH METHOD

In order to gain simultaneous input and noise matching, the source inductor is used. The value of desired input resistance is 50 Ohm. Structure of cascode is a combination of a common-gate load and it effect the increasing of output impedance. Device of additional cascode has a diode. The inductor between the cascode source and supply blocks any RF is leaking to the supply rail and maybe varied in value to optimize the gain response of the LNA. Figure 2 represents a half of final differential LNA. By using the inductive degeneration Ls the topology is matched to 50 Ω. The parameter is often expressed by S11. LNA input impedance expression is defined in (1).

$$Z_{in}(s) = L_s \parallel (LGS + LSS + \frac{1}{Cts} + \frac{gm1Ls}{Ct}) \quad (1)$$

The Zin should be 50 Ω to achieve input matching, so:

$$Z_{in} = gm/C_{gs}L_s \quad (2)$$

in most LNA design the value of Ls was assumed and the values of gm and Cgs are calculated based on the formula to find the required for Zin [8]:

$$\omega_T \cong \frac{gm}{Cgs} = \frac{Rs}{Ls} \quad (3)$$

where ωT is defined as a cut-off frequency. The value of the Rs is 50Ω [9], the optimal Q factor of inductor;

$$Q_L = \sqrt{1 + (\frac{1}{\rho})} \quad (4)$$

where $\rho = \frac{\sigma.\alpha^2}{5.\gamma}$, For parameter p usually depend on the RFCMOS technology, but typically γ is set between 2-3, σ is set to 2-3 times the value of Y and the α assumed to be 0.8-1 [9]. The gate inductance, Lg obtained based on;

$$L_g = \frac{QL.Rs}{\omega o} . Ls \quad (5)$$

while the gate source capacitance, Cgs was determined by ;

$$C_{gs} = \frac{1}{\omega o^2 (Lg+Ls)} \quad (6)$$

$$C_{gs} = \frac{2}{3} Cox.W.Lmin \quad (7)$$

$$W=\frac{3}{2}\frac{Cgs}{2Cox.Lmin} \quad (8)$$

$\varepsilon_{ox}=\varepsilon_{Si}.\varepsilon_{o}$, Where ε_o = dielectric constant for free space 8.854E^{-14} F/cm and ε_{Si}= dielectric constant for silicon 3.9 [9]. Then, the optimum noise figure, NF_{Opt} can be found as below in (9):

$$NF_{Opt}=1+\frac{2\gamma}{\alpha}\left(\frac{\omega o}{\omega T}\right)\sqrt{p}\ \left(|c|+\sqrt{p}+\sqrt{1+p}\right) \quad (9)$$

circuit is stable unconditionally when K>1 it means that Δ<1. According to the meaning of the stability figure;

$$K=\frac{1-|S11|^2-|S22|^2+|\Delta|}{2|S22S12|} \quad (10)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (11)$$

Figure 2(a) shows the schematic circuit of a single ended cascode common source amplifier for input impedance matching with the gate inductor. The differential of LNA schematic circuit is shown in Figure 2(b). Many advantages can be gain by the differential LNA over single ended LNA. A stable reference point is offer by the DLNA compared to the single ended. Second, the noise in the circuit can be reduced by using the differential LNA. The composite signal swing of the differential signal can be twice that of the single ended swing on the same power supply, increasing the signal-to-noise ratio [10-12]. The amplifier alternatively can be increased on the same power supply, distortion will be low, or a low power supply voltage can be used in order to provide same signal swing and lowering the power dissipation [13-15]. Besides that, an image rejection scheme and the use of Gilbert mixers are required to be fed from a differential source [16].

The signal of the differential amplification ensures an attenuation of the common mode signal which is in the most system the common mode signal will be noise [17]. The virtual ground formed at the tail removes the sensitivity to parasitic ground inductances which makes the real part of the input impedance purely controlled by Ls [18, 19]. The balun transformer supply the differential input voltage in the circuit. The balun (a contraction of balanced-unbalanced) is a two-port component placed between a source and load when a differential, balanced RF functional block must connect to a single-ended, ground-referenced one [20]. While at the tail of this stage the ideal current source is added. Source impedance of an ideal current source is an infinite. Table 1 shows the list of components and value for the differential LNA design.

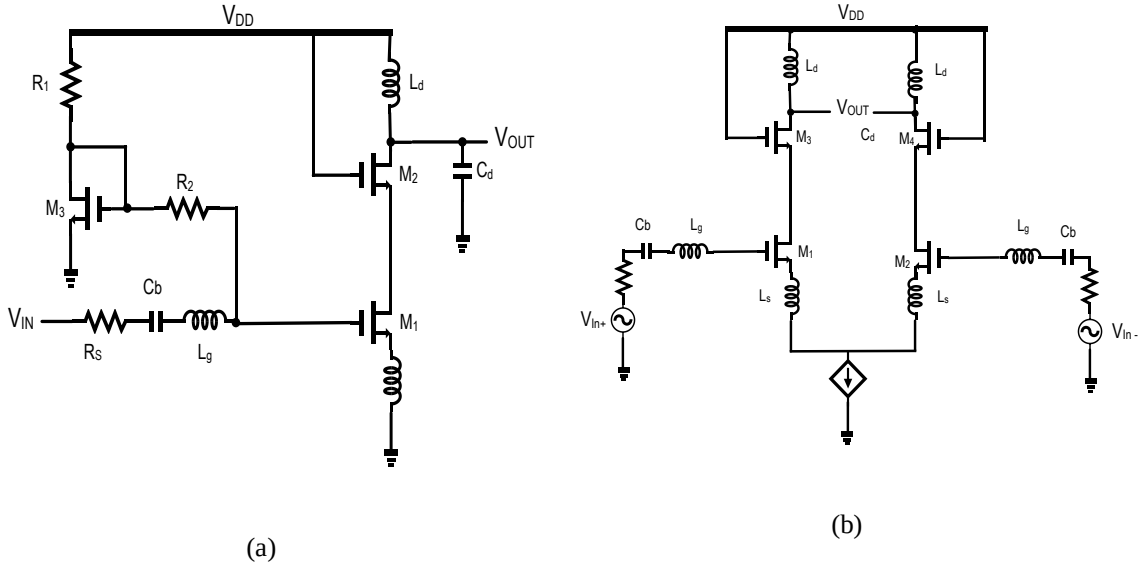

Figure 2. Circuit representation of inductively degenerated cascode LNA: (a) single ended, (b) differential topology

Table 1. List of components and values

Components	Value
R_1	10 KOhm
R_2	10 KOhm
C_1, C_2, C_3, C_4	10 pF
L_g	0.5nH
L_s	9nH
M_1, M_4	W= 2 um
	L= 0.13um
M_2,	W= 126 um
	L= 0.13um
M_3,	W= 136 um
	L= 0.13um

3. RESULTS AND ANALYSIS

The S-parameter plots, and noise performances are shown in Figure 3 to Figure 4 respectively. As can be seen from Figure 4, the circuit's input and output were matched to the 50 Ω required at the operating frequency of 2.4 GHz. The LNA is simulated using 0.13 um technology of CMOS process with 1.2 V supply.

From the Figure 3(a), the simulation of LNA show the input matching, S11 gained versus frequency is -11.18 dB. The maximum gain that the differential amplifier provides is 23.46 dB as shown in Figure 3(a) while the output macthing S22 is -9.492 dB. The S12 is -39.71 dB at 2.4 GHz. As depicted in Figure 4, the noise figure reading is 2.58 dB and the IIP3 is -9.05dBm.

From all the above result gained from the simulation, the circuit provide high gain, high stability, low noise figure and low IIP3. In Table 2, a comparison of the simulated LNA characteristic is included. The proposed CMOS LNA in this paper is reported to have a best value among the other CMOS LNA while comparing the characteristic.

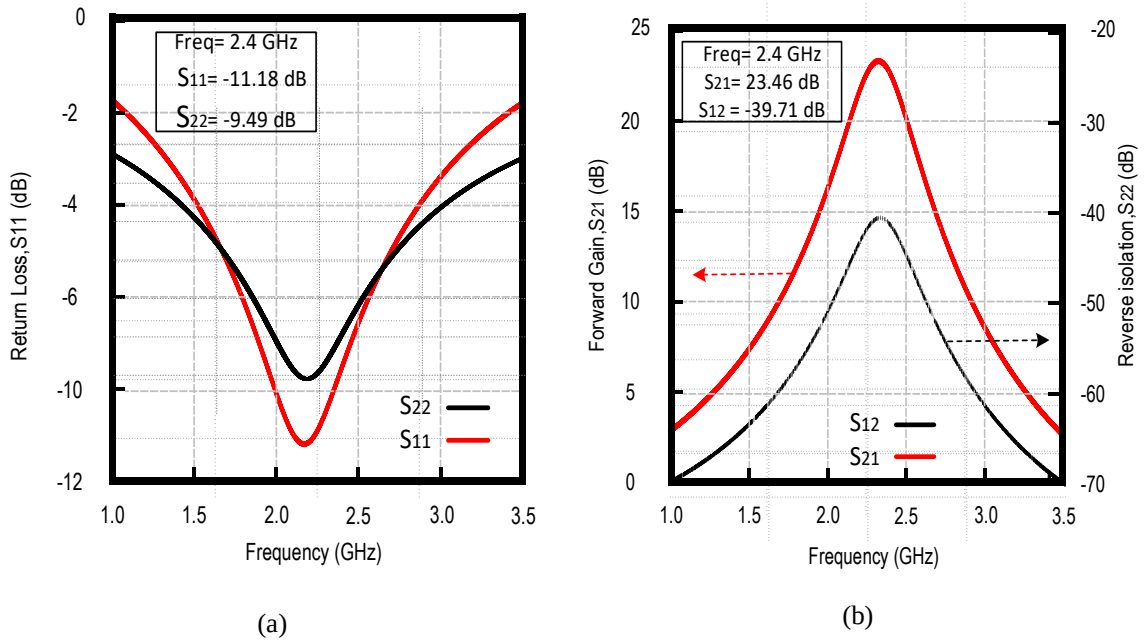

Figure 3. Graph of simulated s-parameter for pre-layout performance of differential LNA: (a) S_{11} and S_{22}, (b) S_{21} and S_{12}

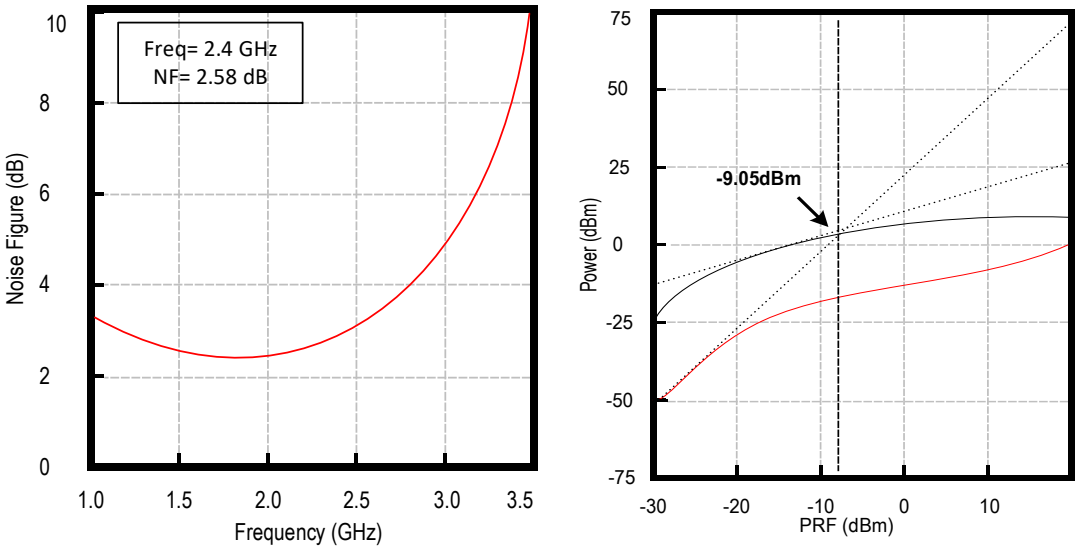

Figure 4. Graph of simulated NF performance and IIP_3

Table 2. Comparison table for LNA performance

Ref.	Tech (µm)	Freq GHz	Gain (dB)	NF (dB)	Power (mW)	S_{11} (dB)	IIP_3 (dBm)
[21]	0.13	3.1-10.6	10.2	0.9-4.1	17.2	-	6.80
[22]	0.18	3.1-10.3	9.6	3.9	13.4	<-9	-3
[23]	0.13	3-5	9.5	3.5	16.5	<-10	-
[24]	0.13	0.1-2	7.6	4.15	3	<-10	0.5
[25]	0.18	0-1.4	16	3	12.8	<-10	<13
[26]	0.065	0.2-5.2	13-15.6	<3.5	21	<-14	0
This work	**0.13**	**2.4**	**23.46**	**2.59**	**3.24**	**<-11.18**	**9.05**

4. CONCLUSION

This paper presenst a simulation of 2.4 GHz CMOS differential LNA using 0.13um technology. The designed LNA achieved a power gain (S21) of 23.46 dB and it mminimum noise figure (NF) of 2.5 dB from a supply of voltage 1.2V. While the power consumption of the proposed designed is 3.24 mW. All the result obtained meets the specifications of RFCMOS Differential LNA which is low NF, high gain performance, high stability and low consumption power.

ACKNOWLEDGEMENTS

This project was funded under FRGS grant FRGS/1/2018/TK04/UITM/02/20 and supported by Faculty of Electrical Engineering, Universiti Teknologi MARA (UiTM) Selangor.

REFERENCES

[1] X. Chen, Q. Feng, and S. Li, "Design of a 2.5GHz Differential CMOS LNA," in *Progress In Electromagnetics Research Symposium*, no. 1, pp. 203–206, 2008.
[2] T. Kanthi and D. Sharath Babu Rao, "Design And Analysis Of CMOS Low Noise Amplifier Circuit For 5-GHz Cascode and Folded Cascode In 180nm Technology," *International Journal of Reconfigurable and Embedded Systems (IJRES)*, vol. 7, no. 3, pp. 149-156, November 2018.
[3] R. Jafarnejad, A. Jannesari, and J. Sobhi, "A sub-2-dB noise figure linear wideband low noise amplifier in 0.18 µm CMOS," *Microelectronics Journal*, vol. 67, pp. 135–142, September 2017.
[4] A. Karagounis, A. Kanapitsas, B. Kotsos, C. Tsonos, A. Polyzos, and E. Petropoulou, "The impact of process faults on specific parameters of a 2.3GHz CMOS LNA," *2010 27th International Conference on Microelectronics Proceedings*, Nis, pp. 299-303, 2010.
[5] B. Prameela and A. Elizabeth, "Design of Low Noise Amplifier for IEEE standard 802.11b using Cascode and Modified Cascode Techniques," *Procedia Technology*, vol. 25, pp. 443–449, 2016.
[6] S. Arshad, R. Ramzan, and Q. ul Wahab, "50–830 MHz noise and distortion canceling CMOS low noise amplifier," *Integration*, vol. 60, pp. 63–73, January 2018.

[7] F. Eshghabadi, F. Banitorfian, N. M. Noh, M. T. Mustaffa, and A. A. Manaf, "Fully-hybrid computer-aided RF LNA design and evaluation for GSM-1900 standard band," *Proc. 6th Asia Symp. Qual. Electron. Des. ASQED 2015*, pp. 177–180, 2015.
[8] C. Microelectronic *et al.*, "Systematic Width Determination for the Design of Power-Constrained Noise Optimization Inductively Degenerated Low Noise Amplifier," in *IETE Journal of Research*, vol. 56, no. 5, pp. 249–256, September 2010.
[9] J. Silver, "MOS Differential LNA Design Tutorial," *RF, RFIC and Microwave theory, Design*, pp. 1–14.
[10] M. Abdulaziz, W. Ahmad, M. Tormanen, and H. Sjoland, "A Linearization Technique for Differential OTAs," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 64, no. 9, pp. 1002–1006, 2017.
[11] H. Zhang, S. Member, E. Sánchez-sinencio, L. Fellow, and I. Paper, "Linearization Techniques for CMOS Low Noise Amplifiers : A Tutorial," vol. 58, no. 1, pp. 22–36, 2011.
[12] L. Duan, W. Huang, C. Ma, X. He, Y. Jin, and T. Ye, "A single-to-differential low-noise amplifier with low differential output imbalance," in *Journal of Semiconductors*, vol. 33, no. 3, pp. 035002, 2012.
[13] C. L. Ler, A. K. Bin A'Ain, and A. V. Kordesch, "Compact, high-Q, and low-current dissipation CMOS differential active inductor," *IEEE Microw. Wirel. Components Lett.*, vol. 18, no. 10, pp. 683–685, 2008.
[14] F. Gatta, E. Sacchi, F. Svelto, P. Vilmercati, and R. Castello, "A 2-dB noise figure 900-MHz differential CMOS LNA," *Solid-State Circuits, IEEE Journal*, vol. 36, no. 10, pp. 1444–1452, 2001.
[15] R. Hajare and C. Lakshminarayana, "Design and software characterization of FinFET based Full Adders," *International Journal of Reconfigurable Embedded Systems (IJRES)*, vol. 8, no. 1, pp. 51-60, March 2019.
[16] R. Khatri and D. K. Mishra, "Comparative Analysis of CMOS RF Receiver Front End for Ultra-Wide-Band Applications," *Int. J. Electron. Eng. Res.*, vol. 2, no. 3, pp. 365–375, 2010.
[17] J. Mariem and P. E. O. Nabih, "Design of active inductor-based Butterworth and Chebyshev microwave Bandpass filters in standard 0.18µm-CMOS technology," *Int. J. Reconfigurable Embed. Syst.*, vol. 8, no. 1, p. 27, 2019.
[18] Y. Sim, J. Park, J. Yoo, C. Lee, and C. Park, "A CMOS power amplifier using an active balun as a driver stage to enhance its gain," *Microelectronics Journal*, vol. 63, pp. 160–169, 2017.
[19] B. Guo, J. Chen, L. Li, H. Jin, and G. Yang, "A Wideband Noise-Canceling CMOS LNA with Enhanced Linearity by Using Complementary nMOS and pMOS Configurations," *IEEE Journal Solid-State Circuits*, vol. 52, no. 5, pp. 1331–1344, 2017.
[20] J. Y. Liu, J. Chen, C. Hsia, P. Yin, and C. Lu, "A Wideband Inductorless Single-to-Differential LNA in 0.18 um CMOS Technology for Digital TV Receivers," *IEEE Microw. Wirel. Components Lett.*, vol. 24, no. 7, pp. 472–474, 2014.
[21] H. Rastegar and J. Ryu, "A broadband Low Noise Ampli fi er with built-in linearizer in 0 . 13- m m CMOS process," *Microelectronics Journal*, vol. 46, no. 8, pp. 698–705, 2015.
[22] Y. Lo and J. Kiang, "Design of Wideband LNAs Using Parallel-to-Series Resonant Matching Network Between Common-Gate and Common-Source Stages," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 9, pp. 2285–2294, 2011.
[23] A. Bevilacqua, C. Sandner, A. Gerosa, and A. Neviani, "A fully integrated differential CMOS LNA for 3-5-GHz ultrawideband wireless receivers," *IEEE Microw. Wirel. Components Lett.*, vol. 16, no. 3, pp. 134–136, 2006.
[24] J. Kim and J. Silva-Martinez, "Wideband inductorless balun-LNA employing feedback for low-power low-voltage applications," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 2833–2842, 2012.
[25] J. Y. Liu, J. Chen, C. Hsia, P. Yin, and C. Lu, "A Wideband Inductorless Single-to-Differential LNA in 0.18um CMOS Technology for Digital TV Receivers," *IEEE Microw. Wirel. Components Lett.*, vol. 24, no. 7, pp. 472–474, 2014.
[26] S. C. Blaakmeer, E. A. M. Klumperink, and B. Nauta, "An Inductorless Wideband Balun-LNA in 65nm CMOS with balanced output," in *Solid State Circuits Conference*, 2007, pp. 364–367.

BIOGRAPHIES OF AUTHORS

Maizan Muhamad graduated from Universiti Tenaga Nasional (Uniten) with the B. Eng (Hons) in electrical & Electronic Engineering in 2002. She was with Panasonic Electronic Devices (Pedma) serve as a Quality Control Engineer in Petaling Jaya from 2002 until 2005. She obtained her M.Sc degree from Universiti Kebangsaan Malaysia (UKM) in 2007. She is currently a senior lecturer in Universiti Teknologi MARA (UiTM), Selangor, working in the area of RF integrated circuit (RFIC). She received her Ph.D degree in the field of analog IC design from Universiti of Malaya in 2019. Dr Muhamad is a member of the Institute of Electronics, Information, and Communication Engineers. She is a Professional Engineer registered under the Board of Engineers Malaysia.

Hanim Hussin received the B. Eng (Hons.) and M.Sc degrees from the National University of Malaya (UKM), Malaysia, in 2004 and 2006 respectively, and the Ph.D degree from the University of Malaya (UM) Malaysia, in 2015. She is currently a Senior Lecturer in Universiti Teknologi MARA and focusing on reliability issues of nano-CMOS devices and CMOS circuit application.

Norhayati Soin received the B. Eng. (Hons) degree in electrical and electronics engineering from the Liverpool Polytechnic, United Kingdom and MSc from Liverpool John Moores University in 1999. She got her PhD in Universiti Kebangsaan Malaysia (UKM) in 2006. She is currently a Professor at University of Malaya and focusing on modelling of nano-CMOS devices.