Indonesian Journal of Electrical Engineering and Computer Science
Vol. 18, No. 3, June 2020, pp. 1207~1214
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v18.i3.pp1207-1214

Optimization of 16 nm DG-FinFET using L25 orthogonal array of Taguchi statistical method

Ameer F.Roslan[1] , F.Salehuddin[2], A.S.M.Zain[3], K.E.Kaharudin[4], I.Ahmad[5]
[1,2,3,4]CeTRI, Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Malaysia
[5]College of Engineering, Universiti Tenaga Nasional (UNITEN), Malaysia

Article Info

Article history:

Received Jul 28, 2019
Revised Oct 30, 2019
Accepted Nov 13, 2019

Keywords:

Double-gate finfet
I_{ON} implantation
Nmos device
Orthogonal array
Taguchi method

ABSTRACT

The impact of the optimization using Taguchi statistical method towards the electrical properties of a 16 nm double-gate FinFET (DG-FinFET) is investigated and analyzed. The inclusion of drive current (I_{ON}), leakage current (I_{OFF}), and threshold voltage (V_{TH}) as part of electrical properties presented in this paper will be determined by the amendment of six process parameters that comprises the polysilicon doping dose, polysilicon doping tilt, Source/Drain doping dose, Source/Drain doping tilt, V_{TH} doping dose, V_{TH} doping tilt, alongside the consideration of noise factor in gate oxidation temperature and polysilicon oxidation temperature. Silvaco TCAD software is utilized in this experiment with the employment of both ATHENA and ATLAS module to perform the respective device simulation and the electrical characterization of the device. The output responses obtained from the design is then succeeded by the implementation of Taguchi statistical method to facilitate the process parameter optimization as well as its design. The effectiveness of the process parameter is opted through the factor effect percentage on Signal-to-noise ratio with considerations towards I_{ON} and I_{OFF}. The most dominant factor procured is the polysilicon doping tilt. The I_{ON} and I_{OFF} obtained after the optimization are 1726.88 μA/μm and 503.41 pA/μm for which has met the predictions of International Technology Roadmap for Semiconductors (ITRS) 2013.

Corresponding Author:

Ameer F. Roslan,
Faculty of Electronics and Computer Engineering,
Universiti Teknikal Malaysia Melaka (UTeM),
76100 Durian Tunggal, Melaka, Malaysia.
Email: ameerfarhan@aol.com

1. INTRODUCTION

The increments towards the amount of the transistors precisely in a compact integrated circuit for the last four decades has been predicted by the Moore's Law due to the needs in fulfilling the demands in various operations, with the number of transistors that doubles in each two years [1, 2]. Effectively, the shrinking of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) scale has been accomplished over the years. This occurrence has impacted the short channel effects (SCEs) to be triggered once the recalling reaches the nanometer regime for which have caused the degradation in system performance along with its reliability and workability [3]. This occurrence has impacted the system performance alongside its reliability and workability for which is degraded due to the short channel effects (SCEs) that have been triggered as the recalling attained to the nanometer regime. Several of FET technology have been developed throughout years of studies in order to overcome these issues while achieving smaller scale [4-9]. The establishment of a fin-shaped field effect transistor (FinFET) has enabled the improvement in the performance of the transistor to be furthered for which has decreased the SCEs consequently as opposed to the planar MOSFET. The manipulations of the carrier mobility, trans-conductance and several other possible

device parameters by the channel length reduction has led to the degradation towards the devices performances. In contrary to the conventional planar MOSFET, the drain potential screening of FinFET is also effectively better. This led to the improvement in short channel performance consequently as the drain-induced barrier lowering (DIBL), subthreshold swing (SS) and also threshold voltage (VTH) roll-off yields near or better to the desired results. Despite the continuous scaling, the degradation of VTH and consequently the IOFF degradation can be reduced through the application of FinFET or other multi-gate FETs (MGFET) [10].

The influence of the SCEs caused the limitations towards the electron drift characteristics within the channel other than the reformation of VTH. The considerations on the reduction of the silicon depletion depth as well as the thickness of the gate oxide are proportion of the gate length. The acquisitions of optimum VTH, drive current (ION) and leakage current (IOFF) as well as SS are driven by the influence of variations in process parameter. The challenges however prevailed in defining the electrical characterization off the variations of the process parameter [11]. The enhancement of design processes in the Polysilicon/Silicon Dioxide (PolySi/SiO2)-based DG-FinFET can be furthered in terms of its robustness through the variations of statistical method that have been implemented in numerous Nano engineering designs [12-18]. The process parameters have been optimized through the application of Taguchi method by Salehuddin et al. and Afifah et al. The aforementioned authors have highlighted the optimization of both VTH and IOFF for a 45 nm besides lowering the IOFF whilst nominalized the VTH for a 22 nm design [19-23]. In this study, simulation based fabrication is carried as this allows the experiment to be done repetitively with respect to the feasibility of cost for which is exponentially less in comparison to conducting the actual experiment other than the fact that the simulation based experimentations allows problem identifications to take its place prior to the actual experiment to take its place. Besides, this experimentation method overcomes the disadvantages of immeasurable information gathering in the actual experiment. Another factor that Taguchi with L25 orthogonal array is chosen in this research is also due to its robustness in vanquishing the high cost of the actual fabrication while also reducing the project duration and time in fabrication completion. Taguchi method also eases the processes of the actual fabrication that is increasingly complex as it approaches the nanometer regime [18].

2. RESEARCH METHOD

2.1. Device Fabrication using ATHENA and ATLAS

In this research, the construction of a 16 nm DG-FinFET device is done by employing the ATHENA and ATLAS modules from Silvaco International for the fabrication process simulation due to differences in terms of features available in each of the respective tool. That said, five geometrical parameters have been identified as well as its ability to trigger variation that takes its effects on the output responses on FinFET as in Table 1. Throughout studies by Kaharudin et. al. (2014) also found that the output responses have also been varied due to the process parameter fluctuations over local parameters variations that are 30% from the overall [19].

Table 1. The Value of the Geometrical Parameters Set

Parameters	Value (nm)
Gate Length, L_G	16
SiO_2 Thickness, T_{OX}	3.25
Main substrate (silicon) length, L_C	35
Polysilicon Length, L_{DM}	17.3
Silicon Thickness, T_{FIN}	18.7

A simulation of the physical structure mesh for the nano-scaled device is developed at start through the Silvaco TCAD as shown in Figure 1. The main substrate used that is the P-type silicon have also employed a substrate orientation of <100> while the construction of oxide layer formed on the top of silicon bulk is functioned as mask during the P-well implantation process. The infusion of Boron at 1x1017 atom/cm3 into the silicon substrate is then followed by the establishment of gate oxide at 875oC in dry oxygen condition in 3% hydrochloric acid (HCl) at 1 atmospheric pressure, subsequent to seclusion of the gate terminal from source and drain that opposes its conductive channel by a dielectric layer. The changes towards threshold voltage can be achieved through an implantation of Boron at approximately 3.845x1013 atom/cm3 with 5 keV of energy in the channel region. That said, small changes on the gate towards its concentration have caused massive changes. Such modifications enabling in procurement to the selections of parameters variation based on ones with most significant variations. The process of conformal

polysilicon process follows the polycrystalline silicon deposition on the semiconductor wafer for when the multi-layered structure is formed. A dopant is implanted using indium with 1.17x1013 atom/cm3 of amounts with 1 keV of energy for which have consequently ensures the diminution of the SCEs as the n-type doped Source/Drain (S/D) areas is doped to the sides of the p-type substrate. The surface of the silicon and polysilicon then have the sidewall spacer constructed with layer of nitride Si3N4 produced. The side capacitance is reduced through compensate implantation following the 22x1018 atom/cm3 of arsenic dose with implant energy of 3 keV in forming an S/D implantation. Prior to the structure mirroring procedure as well as defining the electrode, the metallization process has been performed via aluminium deposition and patterning based from the initial formation of the contact window in the S/D region whereby the fabricated device is simulated as shown in Figure 1. The optimization has taken its place through substitutions in values amongst the identified parameters in obtaining desired output responses. Alteration through geometrical parameter adjustments are based on the parameters identified.

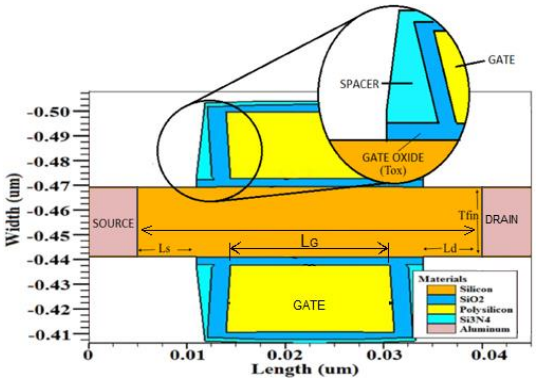

Figure 1. Simulated structure of the PolySi/SiO2-based DG-FinFET

2.2. Optimization using L_{25} Orthogonal Array for Taguchi Method

The selection of L25 orthogonal array have been concocted by its suitability in supporting six relevant process parameters and two noise factors identified for which implemented 25 times of experiments multiplied with repetitions in each level due to the combinations of noise factors. The L25 orthogonal array (OA) experimental layout is constant followed with six process parameters on five different level in Table 2, for which comprises of the polysilicon doping dose, polysilicon doping tilt, S/D doping dose, S/D doping tilt, VTH doping dose, VTH doping tilt. The inclusion of noise factor in Table 3 encompasses two of the gate oxidation temperature, Y and polysilicon oxidation temperature, Z due to remarkable changes as alteration is made against it. That said, the local parameter variation is a subset of the overall variations at 30% for which may affecting the output response variations with the local parameter variation implementation. The increments in parameter variation is recognized to have caused main barrier in scaling as the parameter fluctuation control is done due to the urge of enhancing the performance and yield of integrated circuits [19]. The total degree of freedom of parameters have also influenced in the selection of the OA. Trends of output responses' incremental or decremented pattern can be observing through determining the five-levelled OA from lowest to the highest in level 1 to level 5.

Table 2. Physical Parameters of PolySi/SiO2-based FinFET

Symbol	Process Parameter	Units	Level 1	Level 2	Level 3	Level 4	Level 5
A	VTH Doping Dose	Atom cm^{-3}	$3.825x10^{13}$	$3.845\ x10^{13}$	$3.865\ x10^{13}$	$3.885\ x10^{13}$	$3.905\ x10^{13}$
B	VTH Doping Tilt	Deg.	3	5	7	9	11
C	Polysilicon Doping Dose	Atom cm^{-3}	$2.08\ x10^{14}$	$2.10\ x10^{14}$	$2.12\ x10^{14}$	$2.14\ x10^{14}$	$2.16\ x10^{14}$
D	Polysilicon Doping Tilt	Deg.	-22	-22	-20	-18	-16
E	S/D Doping Dose	Atom cm^{-3}	$1.18\ x10^{18}$	$1.20\ x10^{18}$	$1.22\ x10^{18}$	$1.24\ x10^{18}$	$1.26\ x10^{18}$
F	S/D Doping Tilt	Deg.	70	72	74	76	78

Table 3. Noise Factor of PolySi/SiO2-based FinFET

Noise Factor	Units	Level 1	Level 2
gate oxidation temperature, Y	^oC	870	875
polysilicon oxidation temperature, Z	^oC	870	875

Over the course of 25 experiments performed using the process parameter combination in the orthogonal array, four different combination of experiments were simulated in each number of experiment due to four different unions of noise factor with combinations of two levels with two noise factors that formed Y1Z1, Y1Z2, Y2Z1, and Y2Z2. The VTH is characterized as nominal-the-best to allow the optimized values for the VTH to be near by 12.7% or equivalent to the targeted ones which is at 0.179 V. Meanwhile, the application of larger-the-best characteristics can be justified by the prediction from the ITRS 2013 for the ION to be larger than 1480 μA/μm and therefore, larger-the-best characteristic is applied for the ION to reach as large as possible without compensating other properties. The smaller-the-best characteristics are applied towards both IOFF and SS to be valued as minimum as possible whereby the IOFF is aimed to be lesser than 100 pA/μm by the ITRS 2013. The employment of (1), (4) and (5) enables the SNR (ŋ) for the respective nominal-the-best (NTB), smaller-the-best (STB) and larger-the-best (LTB) to be obtained [24-26]:

$$\eta_{NTB} = 10\log_{10}[\mu^2/\sigma^2] \quad (1)$$

Where

$$\mu = (Y_i + \cdots \ldots + Y_n)/n \quad (2)$$

and

$$\sigma^2 = \sum_{i=1}^{n}(Y_i - \mu)^2/(n-1) \quad (3)$$

$$\eta_{STB} = 10\log_{10}\left[\frac{1}{n}\sum(Y_1^2 + Y_2^2 + \cdots + Y_n^2)\right] \quad (4)$$

$$\eta_{LTB} = 10\log_{10}\left[\frac{1}{n}\sum\left(\left(\frac{1}{Y_1^2}\right) + \left(\frac{1}{Y_2^2}\right) + \cdots + \left(\frac{1}{Y_n^2}\right)\right)\right] \quad (5)$$

Concurrently, ŋ and Y_n denotes the experimental value of response characteristics, and the number of tests and the value of the experimental responses respectively. Yi is the experimental value of the threshold voltage, μ is mean and σ2 is variance. Each of the process parameter effect on the SNR can be split out at different levels due to the orthogonal nature of the experimental design. By applying (1) -(5), the mean, variance and SNR for the device is calculated as in Table 4.

Table 4. Mean, Variance and S/N Ratio for VTH, ION, IOFF and SS for PolySi/SiO2-based FinFET

Exp. No	Threshold Voltage (V_{TH})				Drive Current (I_{ON})	Leakage Current (I_{OFF})	Subthreshold Slope (SS)
	Mean	Variance	SNR (Mean) (dB)	SNR (Nominal-the-Best) (dB)	SNR (Larger-the-Better) (dB)	SNR (smaller-the-Better) (dB)	SNR(smaller-the-Better) (dB)
1	0.21	7.68E-04	17.95	-13.37	57.58	-163.95	-60.61
2	0.18	4.03E-05	29.16	-14.86	64.52	-54.67	-39.49
3	0.18	4.10E-05	29.26	-14.84	65.8	-59.85	-39.55
4	0.18	5.84E-05	29.11	-15.08	66.16	-63.22	-39.62
5	0.17	4.00E-05	28.93	-15.32	66.41	-66.12	-39.71
6	0.19	5.44E-05	29.33	-14.57	65.76	-58.64	-39.55
7	0.18	4.57E-05	29.17	-14.8	66.12	-61.94	-39.63
8	0.18	4.58E-05	29.08	-15	66.36	-64.77	-39.7
9	0.22	7.52E-04	18.36	-13	57.64	-163.82	-60.52
10	0.18	4.83E-05	29.4	-14.76	64.47	-54.17	-39.49
11	0.18	5.43E-05	29.24	-14.74	66.32	-63.58	-39.69
12	0.22	7.74E-04	17.92	-13.21	57.61	-164.1	-60.73
13	0.19	3.99E-05	29.59	-14.45	64.52	-52.97	-39.49
14	0.19	4.36E-05	29.17	-14.43	65.73	-58.03	-39.55
15	0.18	6.22E-05	29.42	-14.69	66.09	-61.45	-39.61
16	0.2	7.08E-05	29.48	-14.18	64.46	-51.67	-39.49
17	0.2	6.79E-05	29.7	-14.18	65.7	-56.88	-39.55
18	0.19	4.20E-05	29.42	-14.4	66.04	-60.08	-39.6
19	0.19	5.98E-05	29.49	-14.61	66.29	-62.98	-39.68
20	0.22	7.77E-04	18.09	-13.05	57.5	-164.04	-60.7
21	0.2	6.53E-05	29.48	-14.16	66.02	-56.88	-39.61
22	0.19	4.68E-05	29.53	-14.33	66.25	-61.7	-39.68
23	0.22	8.44E-04	17.55	-13.33	57.48	-164.34	-60.93
24	0.2	4.73E-05	29.64	-14.06	65.17	-51.04	-39.49
25	0.2	4.71E-05	29.96	-14.08	65.67	-56.4	-39.57

3. RESULTS AND ANALYSIS

3.1. ANOVA for Optimization

The variations of the output response of the process parameters can be attained through the variance decomposition using the analysis of variance (ANOVA). The SNR factor effect percentage meanwhile indicates the relative power factor for which resulting in the variation reduction thence, the significance to the performance is higher if the percentage contribution produced is higher. Based on the percentage factor contribution of physical parameters, the polysilicon doping tilt shows significance towards all of the output responses by obtaining 100% percentage in variation for VTH, IOFF and SS, with ION at 99%. These are proven by the values of SNR obtained from Table 5. In factor D, which is the polysilicon doping tilt, the SNR in level 1 achieved the lowest for VTH at 17.97 dB compared to the SNR for levels 2, 3, 4 and 5. Evidently, SNR towards ION, IOFF and SS are all obtaining at the lowest value with 57.56 dB, -164.05 dB, and -60.70 dB respectively. Retrospectively the VTH achieved 38.585% difference to its nearest value of SNR in level 5. However, factor D also shows its significance in changes in other levels as well whereby the changes in other process parameters shows less in differences in terms of the SNR values obtained. That being said, the variation in process parameters also proved to have acquired its changes towards the output response with variation occurred in the SNR values. Based on the values of SNR obtained, the best combination setting is achieved based on the combination of the best SNR values.

Table 5. Signal-to-Noise Ratio of PolySi/SiO2-based FinFET

Symbol	Process Parameter	Output Responses	Signal-to-Noise Ratio (dB)				
			Level 1	Level 2	Level 3	Level 4	Level 5
A	VTH Doping Dose	V_{TH}	26.88	27.07	27.07	27.24	27.23
		I_{ON}	64.09	64.07	64.05	64.00	64.12
		I_{OFF}	-81.56	-80.67	-80.03	-79.13	-78.07
		SS	-43.80	-43.78	-43.81	-43.80	-43.85
B	VTH Doping Tilt	V_{TH}	27.10	27.10	26.98	27.15	27.16
		I_{ON}	64.02	64.04	64.04	64.20	64.03
		I_{OFF}	-78.95	-79.86	-80.40	-79.82	-80.44
		SS	-43.79	-43.81	-43.86	-43.77	-43.81
C	Polysilicon Doping Dose	V_{TH}	27.09	26.99	27.08	27.11	27.21
		I_{ON}	64.01	64.03	64.18	64.05	64.06
		I_{OFF}	-79.59	-80.42	-80.09	-80.03	-79.34
		SS	-43.79	-43.85	-43.81	-43.82	-43.77
D	Polysilicon Doping Tilt	V_{TH}	17.97	29.45	29.49	29.32	29.26
		I_{ON}	57.56	64.63	65.73	66.09	66.33
		I_{OFF}	-164.05	-52.90	-57.96	-60.72	-63.83
		SS	-60.70	-39.49	-39.55	-39.61	-39.69
E	S/D Doping Dose	V_{TH}	27.16	27.23	27.11	27.13	26.86
		I_{ON}	64.18	64.04	64.04	64.04	64.04
		I_{OFF}	-79.62	-79.71	-79.60	-80.11	-80.42
		SS	-43.79	-43.77	-43.81	-43.81	-43.86
F	S/D Doping Tilt	V_{TH}	27.23	27.00	27.21	27.00	27.05
		I_{ON}	64.04	64.03	64.05	64.03	64.20
		I_{OFF}	-79.65	-79.68	-79.70	-80.44	-80.00
		SS	-43.80	-43.81	-43.77	-43.86	-43.82

3.2. Confirmation Test for Output Responses

Each of VTH, ION, IOFF and SS have produced optimum output responses that are characterized by nominal-the-best, larger-the-best and smaller-the-best characteristics. Thence, the selection of the overall optimized response is done by comparing each of the optimum response combinations whilst weighted by prioritization towards the threshold voltage. The prioritization of combined variation factor via SNR factor effect percentage as listed in Table 6. By exercising the best setting combination, a confirmation test is implemented that emphasised on the accuracy of the prediction. Minimal difference can be spotted within the output response whereby it conforms to the prediction while the simulation is nearer to the values estimated based on Table 7. The pre-optimized simulation in Table 7 represents the output response obtained based on the initial simulation is recorded. The estimation of the optimized results together with the actual results meanwhile can be obtained by averaging each combination of noise factor represented as the observed optimized simulation. The estimated values are obtained through the acquiring the value of the optimized SNR ranges for each parameter. Based on the results obtained, as opposed to the pre-optimized responses, the optimized output response through the implementation of Taguchi with L25 orthogonal array shows an increment towards the ION while the IOFF have been reduced by 74.665% and these have resulting in the increment of ION/IOFF ratio in contrary to the pre-optimized output responses thence requiring less power to

be consumed for the device operation based on smaller ION/IOFF ratio. ITRS 2013 prediction inclusion in Table 7 serves as benchmark as comparisons the aforementioned results and thus the simulated output is strongly consistent albeit a small difference to the estimated ones accordingly.

Table 6. Best Setting Combination for PolySi/SiO2-based FinFET

Symbol	Process Parameter	Units	Highest % Factor Combination		
			Symbol	% Factor	Value
A	VTH Doping Dose	Atom cm-3	A5	0	$3.905x10^{13}$
B	VTH Doping Tilt	Deg.	B4	0	9
C	Polysilicon Doping Dose	Atom cm-3	C5	0	$2.16x10^{14}$
D	Polysilicon Doping Tilt	Deg.	D2	100	-22
E	S/D Doping Dose	Atom cm-3	E3	0	$1.22x10^{18}$
F	S/D Doping Tilt	Deg.	F1	0	70

Table 7. Comparisons of the Best Setting Combination Between Optimized Value with Combination of A5B4C5D2E3F1 with the ITRS Prediction for PolySi/SiO2-based FinFET

Device Charactersitics	Pre-optimized Simulatiom	Optimized Simulation (Taguchi)		ITRS 2013 prediction For the year 2015 [27]
		Estimated	Observed	
Level	$A_2B_2C_2D_2E_2F_2$	$A_5B_4C_5D_2E_3F_1$		
V_{TH} (V)	0.171	0.168	0.190	0.179±12.7%
% Difference from targeted output value	4.469	5.8100	6.007	-
SNR (nominal-the-best) (dB)	28.930	27.100	30.590	-
I_{ON} (μA/μm)	2092.000	1600.000	1726.885	≥1480
% Difference from targeted output value	29.254	7.500	14.296	-
SNR (larger-the-best) (dB)	66.410	64.070	64.710	-
I_{OFF} (pA/μm)	1987.000	981.000	503.413	≤100000
% Difference from targeted output value	98.013	99.019	99.4965	-
SNR (smaller-the-best) (dB)	-66.120	-60.01	-54.20	-
I_{ON} /I_{OFF} ratio	$1.053x10^6$	$1.631x10^6$	$3.430x10^6$	≥14.80
% Difference from targeted output value	99.999	99.999	99.999	-
SNR (larger-the-best) (dB)	-	-	-	-
SS (mV/dec)	96.74	97.70	94.3948	N/A
% Difference from targeted output value	-	-	-	N/A
SNR (smaller-the-best) (dB)	-39.71	-39.8	-39.50	N/A

4. CONCLUSION

The effect of the Taguchi method towards output responses is observed whereby the optimum condition for the PolySi/SiO2-based FinFET device parameters are selected. A combination of A5B4C5D2E3F1 have been decided to produce the best setting combination for which consists of VTH doping dose at level 5 (3.905x1013 atom cm-3), VTH doping tilt dose at level 4 (9o polysilicon doping dose at level 5 (2.16x1014 atom cm-3), polysilicon doping tilt dose at level 2 (-22o), S/D doping dose at level 3 (1.22x1018 atom cm-3), and S/D doping tilt dose at level 1 (70o). The VTH obtained shows small distinction from the target at 0.23618175 which is still within the range set that is ± 12.7% from 0.179 V aimed, while the ION and IOFF obtained are within the estimated range in terms of the SNR. This is closely connected to the prioritization made for VTH to achieve the desired optimal value. The ION and IOFF proved to accomplished superior values than 1480 μA/μm while obtaining minimal IOFF that is lower than 100 pA/μm respectively albeit a slight decrement to the ION in comparison to the pre-optimized, the ION/IOFF ratio gained an increment for the optimized simulation observed. The improvement towards the ION/IOFF ratio allows the operation of the device to require less power consumption. It was concluded that the polysilicon doping tilt contributes a large effect on VTH, as well as ION, IOFF and SS towards the output responses as opposed to other process parameters. Further improvement can be made by merging current method with other suitable statistical method(s) in correlations to Taguchi to further optimize the output responses. Further, the device electrical characteristics was also deduced to have achieved the conformance of the ITRS 2013 prediction for year 2015 requirement.

ACKNOWLEDGEMENTS

The authors would like to thank the Ministry of Higher Education (MOHE) for sponsoring this work under project (FRGS/1/2017/TK04/FKEKK-CeTRI/F00335) and MiNE (Micro and Nano Electronics),

CeTRI, Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for the moral support throughout the project.

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BIOGRAPHIES OF AUTHORS

Ameer F. Roslan received the B.Sc. Degree in Telecommunication Engineering from Technical University of Malaysia Melaka (UTeM), in 2017. He is currently pursuing his M.Sc. degree in electronics and doing research on the DG-FinFET device at Centre for Telecommunication Research and Innovation, Faculty of Electronics and Computer Engineering, Technical University of Malaysia Melaka (UTeM). His research interest includes the DG-FinFET architecture and statistical optimization.

F. Salehuddin received the B.Sc. degree in electrical engineering (Communication) from Universiti Teknologi Mara (UiTM), Malaysia in 2001 and the M.Sc. degree in Electrical, Electronic and System Engineering from Universiti Kebangsaan Malaysia, in 2003. She received the Ph.D. degree in Microelectronics Engineering from Universiti Tenaga Nasional (UNITEN), Malaysia in 2012. She joined Universiti Teknikal Malaysia Melaka (UTeM) in December 2001 as a tutor and is currently a senior lecturer at Faculty of Electronic and Computer Engineering (FKEKK), UTeM. Her research interest includes process and device simulation of nanoscale MOSFETs device, advanced CMOS design and optimization approach (DOE).

A. S. M. Zain received the B.Eng degree in electrical, Electronic and System engineering and M. Sc in Microelectronics from National University of Malaysia (UKM), Malaysia She received the Ph.D. degree in Nanoelectronics Engineering from University of Glasgow, UK in 2013. She is currently working as a senior lecturer at Faculty of Electronic and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM). Her research interest includes Nanoscale Device Design and Simulation, Variability and Reliability of Emerging Technology Devices, IC Design for Biomedical Applications.

K. E. Kaharudin received Ph.D in Electronic Engineering and M. Eng degree in Computer Engineering from Technical University of Malaysia Melaka (UTeM), in 2017 and 2013 respectively. His Ph.D project focused on the process optimization of vertical double gate MOSFET. His research's interests include CMOS design, microelectronics, semiconductors, engineering optimization and artificial intelligence. Recently, his efforts emphasize on the simulation design of Junctionless MOSFET, silicon-on-insulator (SOI) MOSFET, high-*k*/metal-gate stack technology and design of experiment (DoE).

I. Ahmad received the B.Sc. degree in Physics in 1980 from Universiti Kebangsaan Malaysia (UKM). He received the M.Sc. degree in Nuclear Science and Analytical Physics from UKM and University of Wales respectively, in year of 1991 and 1992. He received the Ph.D. degree in Electrical, Electronic and System Engineering from UKM in 2007. He joins the Department of Electrical, Electronic and System Engineering, UKM as a lecturer in 1997 to 2002, and as Associate Professor from 2002 to 2007. He involved in several management and technical positions with MINT, MIMOS and UKM. He is currently a Professor with the Department of Electronics and Communication Engineering, Universiti Tenaga Nasional, Malaysia. He is a senior member of the Institute of Electrical and Electronics Engineers (Senior MIEEE).