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Data Transmission System Based on PCI Bus and Fiber-Optical Link

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Abstract

To achieve real-time monitoring and control of a measurement and control system is often applied in industrial control, with the host computer. In accordance with the requirements of real-time data transmission, a hardware system with a FPGA as the main control unit for the logical interface, the PCI bus and the high-speed fiber-optic link as the data transmission channels communicating with the host computer and a measurement control system respectively is built; the debugging are completed for the HSSL IP core and the PCI interface module; the system test is fulfilled among the host computer, the data transmission board and the specific monitoring control board.

Keywords: *PCI, high-speed fiber-optic link, data transmission system, FPGA*

1. Introduction

In order to achieve real-time monitoring control of certain measurement control system through the host computer, it is necessary to establish a data transmission system between the measurement control system and the host computer. Relative to the common bus RS232 or RS485, PCI bus transfer rate is faster and more stable [1] [2]. Regardless of the digital or analog signals, the optical fiber has a huge transmission capacity and having excellent characteristics such as radio-frequency interference and electromagnetic interference [3-6]. Now, FPGA is applied fairly widely [7-9].Through the analysis of the demand for data transmission, a data transmission with a FPGA as the main control unit for the logical interface, the PCI bus and the high-speed fiber-optic link as the data transmission channels communicating with the host computer and a monitoring control system respectively is built. Its feasibility and usability has been verified by rigorous experiments.

2. The Proposed Method

The measurement control system transmits some data to the host computer each servo cycle through the data transmission system; then he host computer analyses and processes the data. At the same time, the host computer transfers instruction and data to the measurement control system according to the actual situation.

2.1. System Performance Requirements

The data transmission characteristics of the measurement control system are as follows:

- Optical fiber transmission, the transmission rate is 1.25G / s;
- The servo cycle is 200μs, up to send the 1K Byte (256 x 32bits) data each servo cycle;
- Provide the receive data buffer, the size of 1K Byte (256 × 32bits);

According to the data transmission characteristics of the measurement control system, to calculate the maximum transmission rate through the optical fiber:

$$\frac{1000}{200}(KHz)\times 1\left(KByte/Hz\right)=5\,MByte/s \quad (1)$$

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In order to communicate with the optical fiber of the measurement control system, the optical fiber interface of the data transmission system must be fully compatible with the fiber-optic interface used in the measurement control system. In addition, the maximum transmission speed of the PCI bus is 132MB/s [1], far more than 5MB/s，and fully meets the transmission requirements.

2.2. System Architecture

The data transmission system is the bridge between the measurement control system and the host computer. The upstream data from a specific measurement control system is sent to the data transmission system via fiber optic, and then is sent to the host computer via the PCI bus after the data transmission system receives it. The host computer modifies the data buffer area via the PCI bus, and then starts the transmission operation; the data transmission system sends the data to the measurement control system through the fiber optic, after it receives the transmission instruction. The whole procedure is the downstream data flow. The architecture of the Data Transmission System is illustrated in Figure 1.

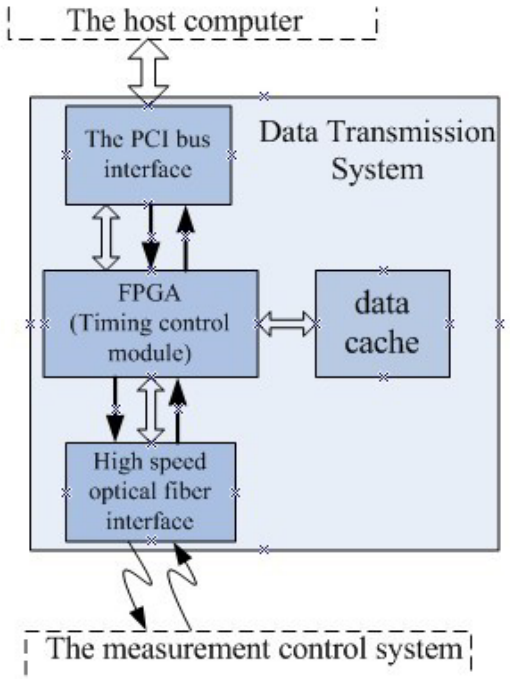

Figure 1. Architecture of Data Transmission System

The data transmission system is divided into four functional modules, namely, a high-speed optical interface module, the PCI bus interface module and the timing control module and a data buffer area. The high-speed optical interface module is divided into the optical transmitter module and the optical receiver module. In accordance with the transmission characteristics of the optical fiber the optical transmitter module will encode the transmission data and serialize it, and modulate from the electrical signal to the light signal transmitted through the optical fiber; the optical receiver module detects the received optical signal, and convert it into an electric signal, and then extract the clock and recover the data. The PCI device convert the complex PCI timing to the simple timing, in order to access it via the programmable logic controller, and can even be directly connected to the processor. Designers can save some time and effort to understand the working principle of the PCI bus and its complex timing, if the interface chips are used for the PCI interface. And the PCI interface has good stability, high reliability, and can also greatly simplify the difficulty of development, improve work efficiency, shorten the development cycle.

The interface timing of the high-speed fiber-optic link data transmission is not compatible with the interface timing of the PCI bus data, so the conversion needs to be done between these two interfaces. And the transmission rate of the high-speed optical fiber link with the transmission rate of the PCI bus is also inconsistent with the transmission rate of the PCI bus, so the data should to be cache. The timing control module and the data buffer area achieve these two works. The conversion timing between the high-speed fiber-optic link interface and PCI interfaces is realized by the FPGA. The amount of data sent by the measurement control system each servo cycle is not large (1Kbyte), so these data can be temporarily stored in FPGA. If done, the circuit design will be simplified; the resources and the cost will be saved.

2.3. System Hardware Structure

The hardware structure of Data Transmission System includes the optical fiber data transceiver part, the interface portion of the PCI bus, the bus timing control and timing conversion portion, the power supply system. The optical fiber data transceiver part divided into the photoelectric conversion part and the data encoding/decoding section. The special interface chip is used to achieve the PCI bus interface. The FPGA, as the main control unit, fulfils the timing conversion and timing control. The power supply system provides the other parts with operating power, its stability and reliability affects the stability and reliability of the entire system. The design of the power supply system need to analyze the power type and the power consumption for the entire system, in order to determine the types of the power supply and to choose the power chips. The host computer supply the +5V power with Data Transmission System though the PCI slot. The others power supplies, such as 3.3V, 2.5V and 1.2V need to be conversed by the various power functional chips. There must be two types 1.2V supply. One is for the internal logic array of the FPGA; the other is for the FPGA PLL [10]. The hardware structure of Data Transmission System is illustrated in Figure 2.

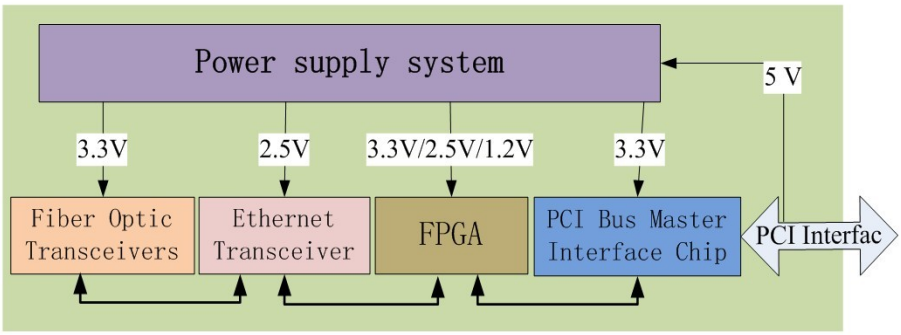

Figure 2. Hardware Structure of Data Transmission System

3. Research Method

Software implementation of Data Transmission System is based on the Quartus II development environment, using the top-down design ideas. It can be divided into the PCI interface module, PCI interrupt control module and a high speed optical fiber core. The interface diagram of Data Transmission System is illustrated in Figure 3.

3.1. PCI Interface Programming

The PCI Local Bus is a high performance 32-bit or 64-bit bus with multiplexed address and data lines [1]. The PCI interface program achieves the analysis of PCI local bus timing. It includes eight states, i.e., Idle, Jdg_Mode, Reg_write, Reg_read, Buf_write, Buf_read and Invalid_add_write, Invalid_add_read. The state transition of PCI interface program is illustrated in Figure 4.

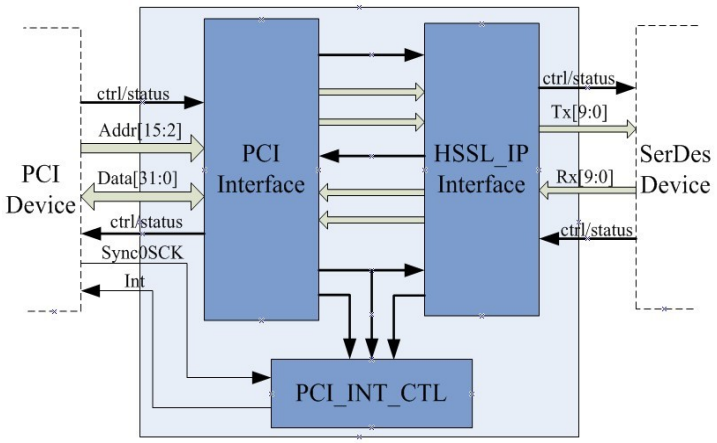

Figure 3. The interface diagram of Data Transmission System

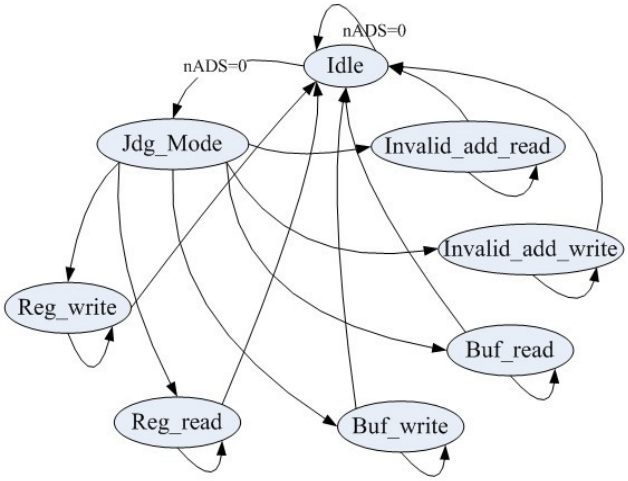

Figure 4. The state transition of PCI interface program

By default, the interface module is in the idle state. Once the signal nADS is low, the interface module will enter the “Jdg_Mode” state. Otherwise it remains in the “Idle” state. And then, once some signal is triggered, the “Jdg_Mode” state will jump to the corresponding state one of the six states outside, in addition to idle state. After completing each operation, the state will return to the "Idle" state.

3.2. Interrupt Control Module

Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. PCI interrupt signal just only one (nINTA), and issued by the PCI special interface device. When the interrupt input pin “nLINT” of the local bus detected by the PCI special interface device is low, the PCI special interface device generates PCI interrupt, and releases PCI interrupt until the input pin “nLINT” becomes high. There are three interrupt in the fiber interface IP core. These interrupts are edge interrupt and not compatible with the local interrupt of the PCI interface in the interrupt number and trigger mode. Therefore interrupt control module must be set in the PCI interface.

3.3. Optical Fiber Interface Programming

The fiber interface IP core may be divided into the sending module, SerDes control module and receiving module. The transmitter / receiver module consists of three parts, i.e., the

transmission / reception logic control, transmission / receive buffer and transmitting / receiving encoded. Optical Fiber programming interface is illustrated in Figure 5.

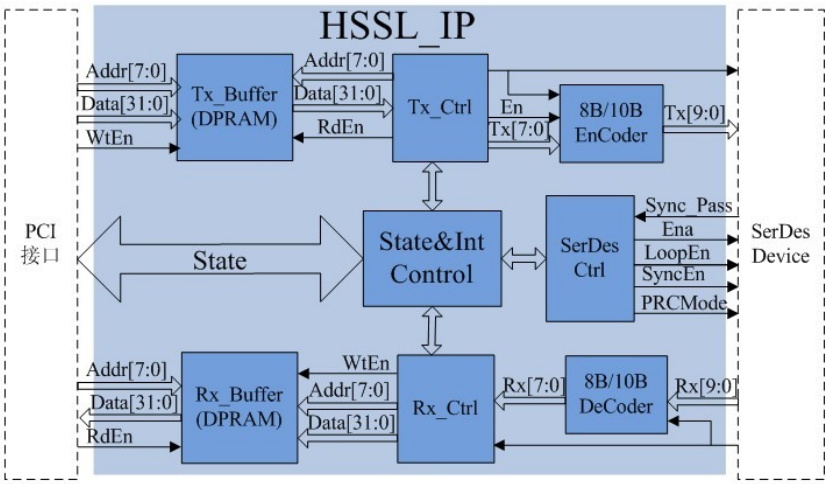

Figure 5. The interface diagram of the optical fiber programming

High speed optical fiber link core (HSSL_IP), are respectively connected to the PCI dedicated interface control module and the string and converter (SerDes).The host computer controls the Tx_Buffer write control signal of HSSL_IP transfers the 32-bit data to the Tx_Buffer of HSSL_IP via the PCI interface. Then the data transmission controller of HSSL_IP issue the read signal, trigger to transfer the data with the 32-bit long word format to the transmission control module, and in the transmission control module convert the 32-bit long word into the 8-bit word, and transfers it to the 8B /10B encoder. In the encoder the 8-bit words are converted into the 10-bit format, and transferred to the Serial-parallel converter (SerDes). This process is the data transmission. The data receiving process begins with the serial-parallel converter, transfers the 10-bit data to the 8B /10B encoder of the HSSL_IP via the data bus RX[9:0], and converts into the 8-bit format, and converts the 8-bit word into the 32-bit long word in the data receiving module, and sends to the Rx_Buffer of HSSL_IP. The host computer controls the Rx_Buffer read control signal, reads the 32-bit data, and processes32-bit them.

a) Transmission module

Transmission logic control part

According to the optical fiber data transmission protocol the transmission logic control part sends out the instruction or data by a certain order or format. The transmission controller operated by the control instructions of the application layer, supports three kinds of instruction which are the data frame, response frame and trigger frame respectively. The state transition of the transmission module is illustrated in Figure 6.

The transmission controller requires that the application layer has updated the transmission data buffer, and has set up the correct frame header information before booting the data transmission. Once the data transmission is started, the transmission process will be operated according to the frame header information. The state transition of the transmission module is implemented by the synchronous reference clock rising edge. The transition relationship of the transmission module is clear, does not involve any waiting or handshake status. The framing and data transmission of the transmission module are according with the data link protocol and its link management method strictly. In addition, in order to ensure the phase relationship of the send-receive, each long word is added in a synchronous character SYN. The start signal of the transmission logical control is sent out by host computer through the PCI interface. When the data is being sent, the SOF character is sent firstly. Then the frame-header information (including frame length and starting address) stored in a fixed address is accessed, and encapsulated into 4 words to be sent out. Subsequently, the 32-bit data is

read from the transmit buffer, packaged into a 4 words format, and compute the checksum ,and then transfer the data word by word. Finally the EOF character is sent. Data send completed.

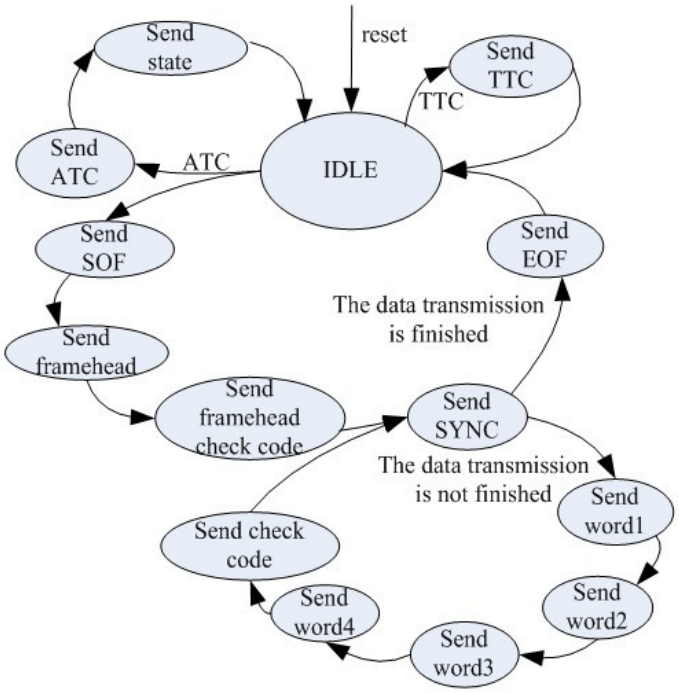

Figure 6. The state transition of the transmission module

Transmission buffer

Transmission buffer is designed into a dual port RAM. The host computer sends the data to the transmission buffer via the PCI interface; the logic control module of the optical fiber transmission read the data from the transmission buffer. A dual port RAM is designed as the transmission buffer via the Quartus II macro module, with the size of 1K (256 32-bit storage spaces), the data width of 32-bit, address width of 8-bit.

Encode module

The data sent to the encode module from the transmission control module is a 8 bit. These 8-bit data is encoded to 10-bit data in the encode module, coding module, and be sent out to the SerDes device. In accordance with the 8B/10B coding standard [11], the 8-bit data are decomposed into 3 high bit and 5 low bit, wherein the high 3 bits are encoded into 4-bit forms, the low 5 bits are encoded to 6-bit forms. The two encoded data are combined together, and form a final 10-bit data.

b) Receiver module

The design of the Receiver buffer is in common with the design of the transmission buffer, in this section will no longer be repeated.

Receiver logic control part

The received data is analyzed, stored and responded by the receiver logic control part in accordance with the data transmission protocol of the optical fiber. The state transition of the receiver module is illustrated in Figure 7.

After being reset, the receiver module directly enters into the IDLE state, and analyzing the receiving data analysis in the IDLE state. If the special characters were received, the state of the receiver module will enter into the other state to receive the data or response the command. The receive logic control module supports three types of frames received. They are

TTC frame, ATC frame and the data frame. Once the special characters of SOF are detected, the state of the receiver module enters the data receiving state. Firstly he frame head and the check information of the frame-head are received; and then the synchronization character SYNC is received. If the special character EOF is not received after the synchronous character is received, the data continue to be received. That the EOF is received means data receiving completion. The data receiving is finished; meanwhile the receiver logic control module triggers the transmission logic control module to send ATC back to the IDLE state.

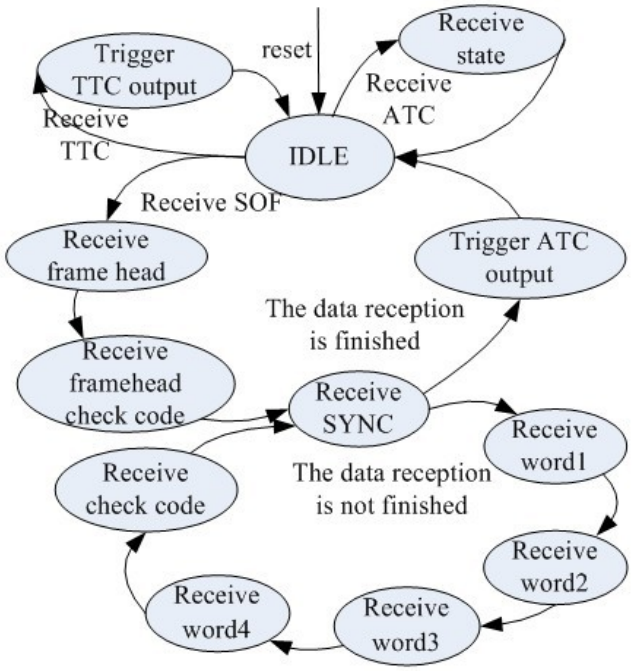

Figure 7. The state transition of the receiver module

Decode module

Receiving decoding revert the 10-bit data to the 8-bit data. Its method is similar to the coding method. The 10-bit data are decomposed into 4-bit and 6-bit, and are decoded into the 3-bit and 5-bit respectively; and then the two groups of the decoded data are grouped together into 8-bit data.

4. Results and Discussion

In order to verify the feasibility of the data transmission system hardware and software design, experiments must be made. The experimental procedure is as follows: the fiber optic interface is tested firstly. If it is stable, the PCI interface will be tested. Finally, the system board is debugging.

4.1. Test of the Fiber Optic Interface

The debugging purposes of the fiber interface checks the stability of the optic fiber link and the functions of the fiber-optic interface IP core. The material object test of the self-transmitting and self-receiving is illustrated in Figure 8.

The timing and data of the optical fiber is captured, analyzed with the SignalTap in the Quartus II. The SignalTap II logic analysis is illustrated in Figure 9.

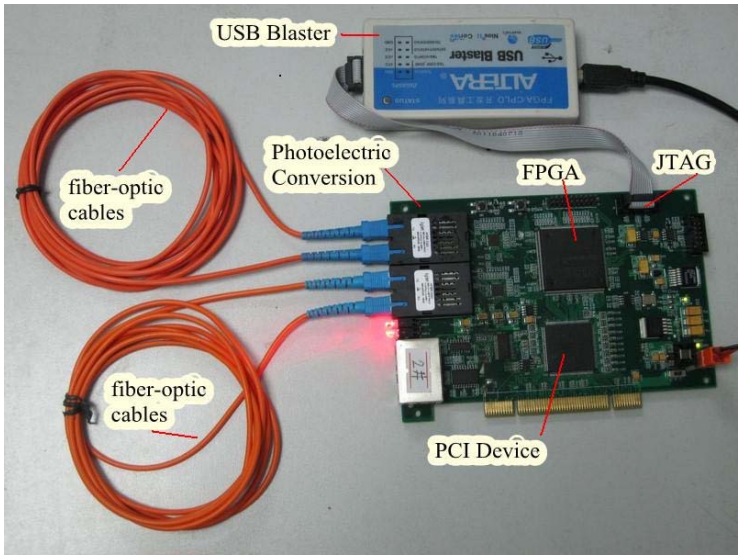

Figure 8. The test of the fiber optic interface

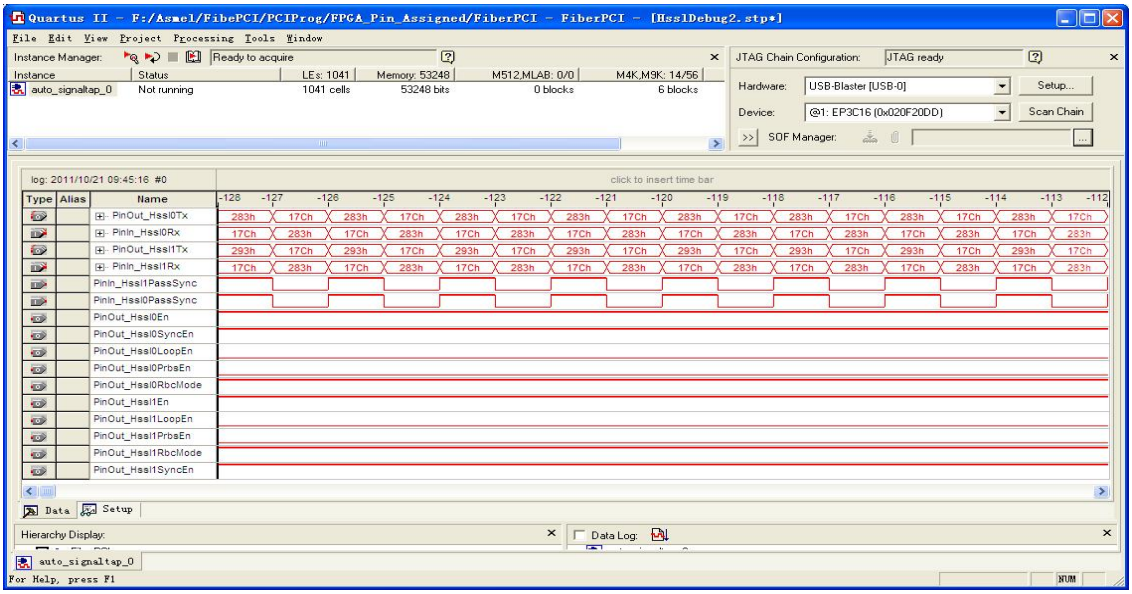

Figure 9. The Signal Tap II logic analysis

4.2. Test of the PCI Interface

The Data Transmission System card needs to be inserted into the host computer's PCI slot. The material object of the PCI interface test is illustrated in Figure 10. After t the driver program is installed on the PC, the data of the measurement control system can be accessed via the optical fiber interface and Data Transmission System.

4.3. Data Transmission System Debugging

Data Transmission System board is applied to transmission the data between the measurement control system and the host computer. It is not enough to test the system functions. So it is necessary to make the Data Transmission System debugging for the best system board.

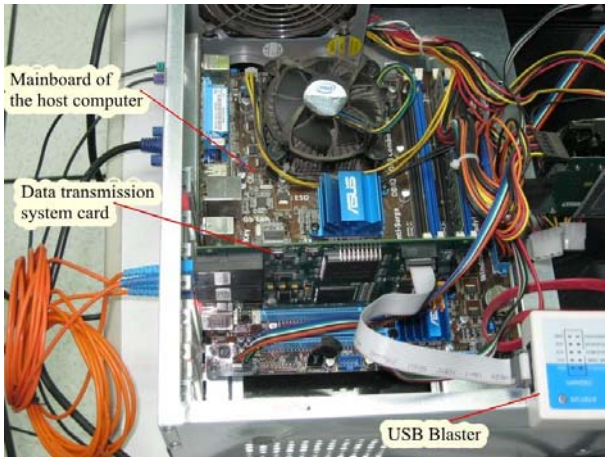

Figure 10. The test of the PCI interface

The system test includes the data transceiver test from the host computer to the optical fiber interface， the PCI interrupt function test and the data correctness. the data transmitted by the optical fiber interface 0 of the measurement control system is received by the optical fiber interface 1 of the system card; the data transmitted by the optical fiber interface 1 of the measurement control system is received by the optical fiber interface 0 of the system card . The PCI interrupt is sent after the data is received each interface. The test process is shown in Figure 11, the flowchart “a” is the main control program, and the “b” is the PCI interrupt program test. The information interact between “a” and “b” is fulfilled through checking the completion flag.

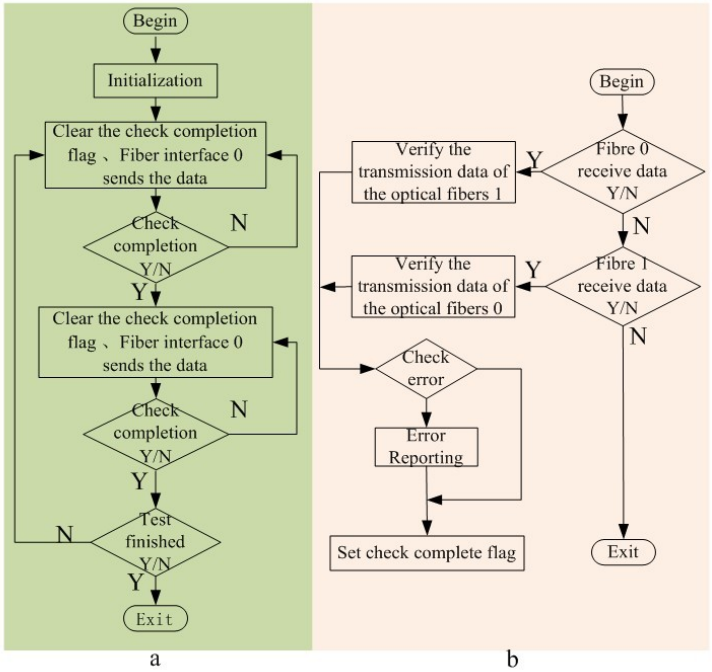

Figure 11. Test process of the Data Transmission System

During the test, the data to be sent by the measurement control system needs to be pre-defined. The measurement control system transfers these data to the host computer each

servo cycle via the optical fiber interface. In order to ensure the data received is correct, these data compare with the data sent from the measurement control system after it is received by the host computer. The material object of the system test is illustrated in Figure 12.

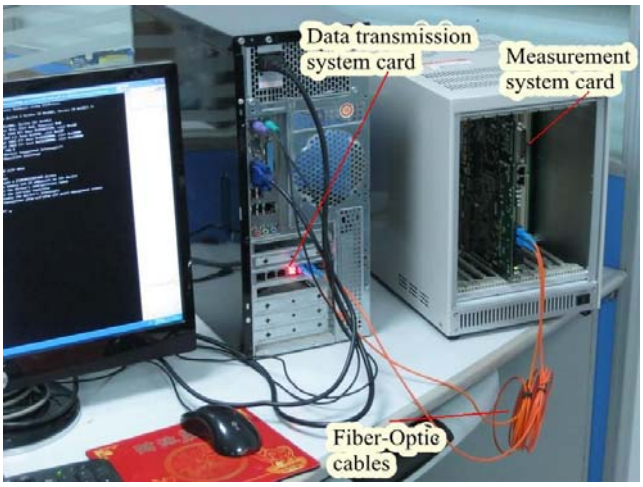

Figure 12. System test

5. Conclusion

After doing the analysis of the data transmission, the hardware architecture of Data Transmission System is set up, which is configured a FPGA as the logical master unit, the interface of the high-speed fiber link as the data communication unit between the measurement control system and the FPGA, the PCI interface as the data channel between the host computer and the FPGA. The program design of the Data Transmission System based on the Verilog is detailed. The debugging of the optical fiber interface IP core and the PCI interface is made with the SignalTap of the Quartus II, and the system test is done. The test result shows that the Data Transmission System program is feasible, and the Data Transmission System can be look as the bridge between the host computer and the measurement control system.

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