Indonesian Journal of Electrical Engineering and Computer Science
Vol. 17, No. 2, February 2020, pp. 783~792
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v17.i2.pp783-792

Optimized low voltage low power dynamic comparator robust to process, voltage and temperature variation

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Article Info

Article history:

Received May 27, 2019
Revised Jul 2, 2019
Accepted Jul 16, 2019

Keywords:

Dynamic comparator
Double-tail dynamic comparator
Low power comparator ADC
SAR ADC

ABSTRACT

Power consumption and speed are the main criteria in designing comparator for analog-to-digital converter (ADC). This paper presents an optimized low voltage low power dynamic comparator which is robust to process, voltage and temperature (PVT) variations with adequate speed. The comparator circuit was designed using 0.18µm CMOS technology with low voltage supply of 0.8V. The method used to verify the robustness of the comparator circuit across 45 PVT is presented. The circuit is simulated with 10% voltage supply variation, five process corners and temperature variation from 0°C to 100°C. The simulation result show that the proposed comparator circuit achieved significant reduction of power consumption and delay during worst case condition compared to dynamic comparator proposed from previous researchers.

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1. INTRODUCTION

Energy efficiency is the main key parameter in many emerging system-on-chip (SoC) applications such as wireless sensor networks and portable electronics devices [1, 2]. Due to the high demand of such ultra-low power applications, the needs for energy efficient analog-to-digital converter (ADC) are really essential. Among ADC architectures, successive approximation register ADC (SAR ADC) consumes relatively low power with acceptable speed and resolution [3, 4]. In SAR ADC, comparator is the main block to convert analog signal into digital code [5]. As a critical block, comparator needs to be robust enough to operate with low supply voltage in order to achieve low power consumption [5]. To ensure the robustness of a design, process corner simulation is required at the design stage. Process corner represents the extremes parameter variation of integrated circuit design which is fabricated on semiconductor wafer [6-15]. Parameter variations include range of process transistor properties, supply voltages and die temperatures [8, 9]. In nanoscale technology, scaling down of voltage supply near to threshold voltage can provide excessive savings in dynamic energy. However it will reduce the voltage headroom for cascode structure to operate correctly [7-17]. Therefore, to design low voltage and low power dynamic comparator with low supply voltage is a big challenge when the number of transistor stacking is high [16-23].

The most popular energy efficient comparator is dynamic comparator Figure 1 which only operates during regeneration time [2-18]. The additional features are high input impedance, rail to rail output swing, zero static power, low offset voltage and fast decision making that comes from strong positive feedback and

differential input architecture [1-22]. However, this topology requires high supply voltage to operate the circuit because numbers of transistors stacking are high. For this reason, this topology is perceived to be unsuitable for ultra-dep sub-micrometer CMOS technology with limited supply voltage and small voltage headroom. To overcome these issues, in [10], had proposed double-tail dynamic comparator with double-tail topology by splitting the pre-amplifier and latching stage Figure 2(a). The objective is to reduce the number of stacking transistor and at the same time improve the current flow in the small voltage headroom [1, 10, 24]. However, this topology consumes high power consumption because of pre-amp and latching stage operates at the same duration [1]. Further, the two phase latching clock method also contributes to high energy consumption, large die area and increase delay at regeneration time [12]. In [12], proposed modification of double-tail dynamic comparator which is known as pseudo differential dynamic comparator Figure 2(b). The tail transistor in latching stage was removed and only one clock phase is required to trigger the circuit. In this topology, the skew between two phases of latching clock has been eliminated and at the same time, the offset voltage can be reduced [10]. However this topology consumes high power consumption due to additional reset transistors in the circuit.

In [10] and [12], have proposed dynamic comparators with optimization on power consumption and speed. However, there are no details verification result over 45 process corners variation that have been recorded. This paper presents a new low power low voltage dynamic comparator which is robust to 45 process corners variation as shown in Section 2. A verification method used to verify the robustness of proposed comparator over 45 process corner variation is explained in Section 3. The process corner simulation result and performance comparison over PVT variation of proposed comparator. In [10] and [12], comparator is presented in Section 4. For simulation, 0.18µm CMOS technology at 0.8 supply voltage (VDD) and 0.4 voltage common mode (VCM) is set and PMOS is used as differential input transistor.

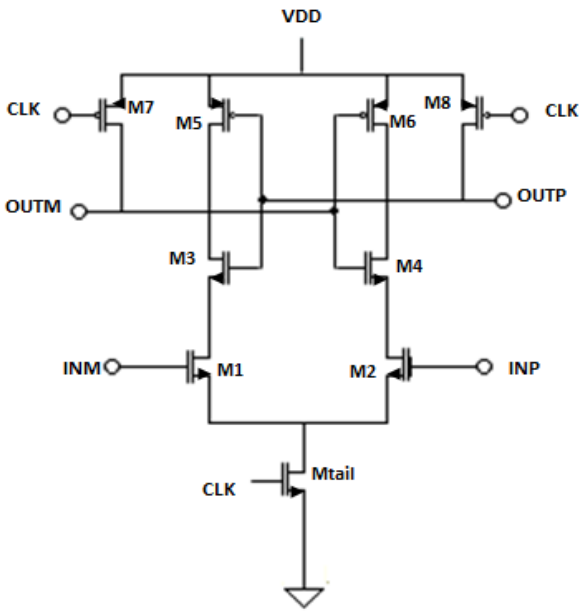


Figure 1. Schematic diagram of the conventional dynamic comparator

2. DESIGN METHODOLOGY

2.1. Conventional Double-Tail Dynamic Comparator

The first double-tail dynamic comparator was proposed by *Schinkel in 2007* Figure 2(a). In this topology, the number of stacking transistor was reduced by splitting pre-amplifier and latching stage. By introducing two stages dynamic comparator or double-tail dynamic comparator, individual tail transistors *Mtail1* and *Mtail2* are used in pre-amp and latching stages. The *Mtail1* at latching stage enables the large current to enhance latching speed while *Mtail2* allows small current flow at pre-amp stage to achieve low offset voltage at input comparator [10]. This comparator circuit operates in two conditions; reset phase and regeneration phase. During reset phase, CLK = VDD both *Mtail* are in OFF condition, transistors *M5*/*M6* reset node *fm* / *fp* to GND and pull OUTP /OUTM to VDD. In regeneration phase, CLK = GND both *Mtail* are turned ON, transistors *M5*/*M6* are turned OFF and voltage at node *fm* /*fp* start to drop with the rate of

IMtail1/C*fm*(*fp*). During this time, a voltage different at node *fm* and *fp* is developed and it becomes a gain to the latch state. This topology has less kickback noise due to the isolation between input and output node [1-10]. However, this topology consumes high power because of pre-amp and latching stage start to operate at the same duration [1-25]. Further, the two phase latching clock method also contributes to high energy consumption, large die area and increase delay at regeneration time [10].

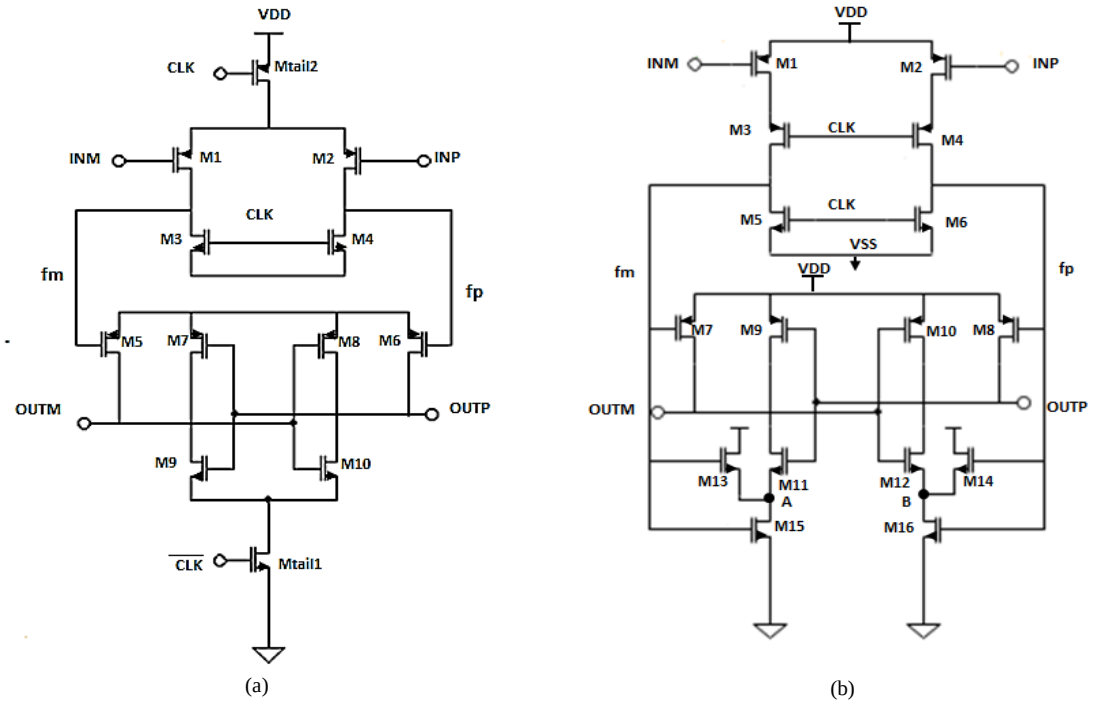


Figure 2. Schematic of (a) Schinkel's comparator (b) Paik's comparator

2.2. Pseudo Differential Dynamic Comparator

In [12], proposed pseudo differential dynamic comparator Figure 2(b). The design is based on Schinkel's 2007 comparator with modification on the tail transistor in latching stage. In this design, only one clock phase is required to trigger the circuit. The latching stage is triggered by signal from output of a pre-amplifier [12]. The operations of this comparator are similar to conventional double-tail dynamic comparator which begins by resetting phase in pre-amplifier and followed by regeneration phase. During reset phase, CLK = VDD, *M3/M4* are OFF while *M5/6* are ON. Then, the output pre-amplifier node *fm/fp* will be reset to ground. Thus, *M7/M8* at latching stage turns ON and pulls node *OUTM/OUTP* to VDD while *M13/M14* and *M15/M16* are turned off causing latching phase not to be activated. When CLK=GND, regeneration phase, *M3/M4* are ON while *M5/6* are OFF. The drain current *M3/M4* is determined by input voltage at INP and INM. The different rate of current flow per time at node *A/B* develops high voltage different as time passes by. It becomes an input gain to the latching stage. In this topology, the skew between two phases of latching clock has been eliminated and at the same time, the offset voltage can be reduced [10].

2.3. Low Voltage Low Power Comparator Design

From the performance of process corner simulation result in Paik and Schinkel comparator, we proposed new low voltage low power comparator as given in Figure 3. The improvement focuses on power consumption and delay during PVT variation as shown in Table 3. Due to good performance of Paik's comparator, some modifications have been done in order to improve the power consumption and delay of the circuit when it operates with 0.8V voltage supply and 0.8mV input voltage different (ΔVin). The same topology in Paik's comparator was used in this comparator but transistor *M13/M14* was removed. In Paik's comparator, this transistor is used to reset the node *A* and *B* to reduce mismatch between *M15/M16*. However, this feature is not necessary in medium speed because it induced additional power consumption and delay.

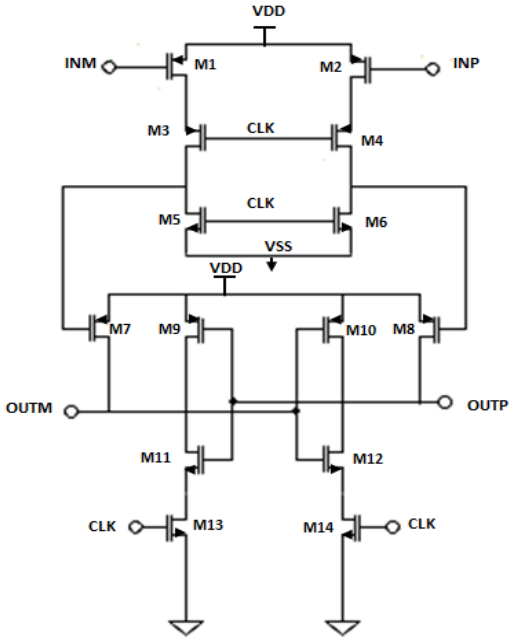


Figure 3. Schematic of proposed comparator'

2.4. PVT Verification Method

To verify the performance of each comparator, test setup as in Table 1 was used during 45 corner simulation. The clock frequency was set to 2 MHz and the period of each test sequence is set to 1µS. Both differential input positive (INP) and input negative (INM) are set in two worst condition of ΔVin, small ΔVin = 800µV and big ΔVin = 800mV. This worst condition of ΔVin selected based on the maximum and minimum different of input voltage for the proposed comparator which are 800mV and 800µV. The minimum input different 800µV is the 1/2 LSB for 10 bits digital output. The four values of input voltage are used to create input test pattern (small ΔVin = 800µV and big ΔVin = 800mV) as shown in Figure 4. For test pattern (big ΔVin), as shown in Figure 4, the test sequence 2, the INP is set at voltage 800mV and INM is set at voltage 0V. For test pattern (small ΔVin), as shown in Figure 4, the test sequence 3, the INP is set at voltage 400.4mV and INM is set at voltage 399.6mV. The order of test sequence in Table 1 is set based on the transition of input level in worst case condition. From the sequence we can observe the performance of the comparator in the worst case condition of input different and variation of process, voltage and temperature.

To verify the robustness of the circuit through fabrication process, voltage and temperature (PVT) variation, 45 process corner simulations is required. In corner simulation setup, PVT parameter was set to fabrication process corner (FS; SS; SF; TT; FF), voltage supply (VDD) (720mV; 800mV; 880mV) and temperature (0°C; 27°C; 100°C). The parameter of VDD is based on 10% voltage variation and temperature is based on low temp 0°C room temp 27°C and high temp 100°C. The detail of transistor condition over process corner variation is stated in Table 2. For process F, transistor is operating at high speed and at the same time consumes high power while for S process; transistor is in worst speed and low power condition.

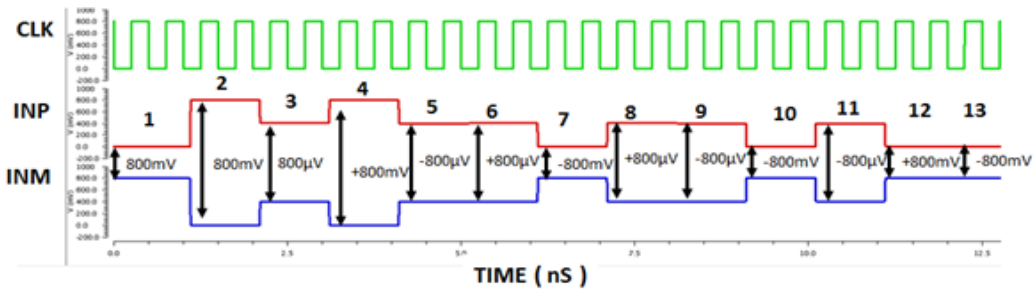


Figure 4. Waveform of input test pattern

Table 1. Details of Input Test Setup

Test Sequence	Time Period (µS)	Input INP (mV)	Input INM (mV)	Voltage Input Different
1	0-1	0	800	- ΔVin = -800mV
2	1-2	800	0	+ΔVin = +800mV
3	2-3	400.4	399.6	+ΔVin = +800uV
4	3-4	800	0	+ΔVin = +800mV
5	4-5	399.6	400.4	- ΔVin = -800µV
6	5-6	400.4	399.6	+ΔVin = +800µV
7	6-7	0	800	-ΔVin = -800mV
8	7-8	400.4	399.6	+ΔVin = +800µV
9	8-9	399.6	400.4	-ΔVin = -800µV
10	9-10	0	800	-ΔVin = -800mV
11	10-11	399.6	400.4	-ΔVin = -800µV
12	11-12	800	0	+ΔVin = +800mV
13	12-13	0	800	-ΔVin = -800mV

Table 2. Standard Fabrication Process Corner Parameter

Corner Parameter	Condition NMOS	Condition PMOS
FF	FAST – high mobility	FAST – high mobility
SS	SLOW - low mobility	SLOW - low mobility
TT	TYPICAL - nominal	TYPICAL - nominal
FS	FAST – high mobility	SLOW - low mobility
SF	SLOW - low mobility	FAST – high mobility

2.5. Power Consumption and Delay Measurement Method

To measure average power consumption from the comparator circuits, the expression (1) was set in Calculator tools in Virtuoso Visualization Analysis XL and Analog Design Environment (ADE). In calculator windows, select option *average* from Function Panel for measuring average power consumption, and then choose *IT* from Schematic Selection Toolbar for *transient current*. The *V20/PLUS* in (1) represents voltage supply for comparator circuit. To measure the maximum and minimum power consumption, the expression (1) needs to be set in process corner simulation setup. Worst case delay measured at voltage VDD/2 is shown in Figure 5.

*(average (IT("/V20/PLUS")) * 0.8)* (1)

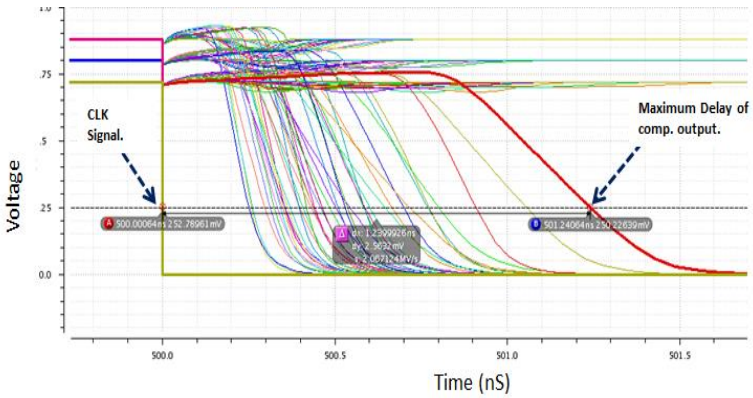


Figure 5. Maximum delay process corner simulation result of proposed comparator

3. SIMULATION RESULT AND DISCUSSION

The simulation result and comparison of the proposed design with *Paik's* and *Schinkel's* comparator is presented in this section.

3.1. Functional Simulation

Figure 6 shows 45 process corner simulation of proposed comparator design. The comparator passes all 45 process corner in clock frequency 2MHz. As shown in Figure 6, the proposed design able to operate in

critical input sequence set in INP /INM signal. The output positive OUTP and output negative OUTN will reset high to VDD and toggle to 0V referring to INP /INM signal and every negative edge of clock CLK signal.

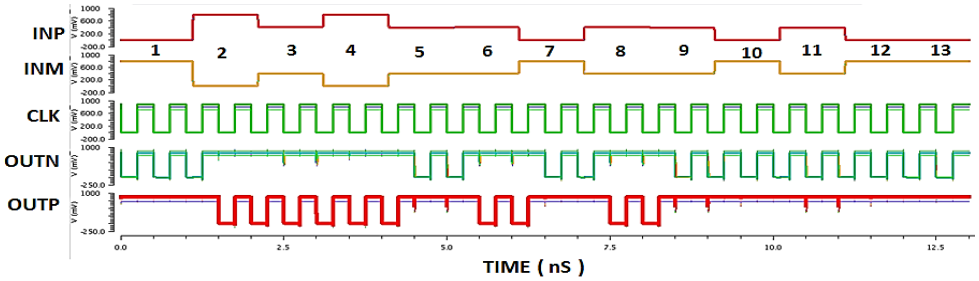


Figure 6. 45 Process corner simulation result of proposed comparator

Figure 7 shows details of 45 process corners simulation result from *Schinkel's* comparator circuit. The details of failure capture in output positive (OUTP) signal. From the simulation result, it failed at 3 process corners which are at (SS;800mV;0°C), (FS;720mV;0°C), and (SF;720mV;0°C).

For process corner (FS;720mV;0°C), failure occurred in test sequence number (3, 6, 8, 9,11). The failure occurred in minimum positive input INP is 400.4mV. At this process corner variation, transistor NMOS is set in high mobility, transistor PMOS is in low mobility, VDD supplies is set to 10% lower than nominal VDD 720mV and low temperature 0°C. The transistor PMOS take longer time to operate in weak condition and results in low gain at input latch.

For (SS;800mV;0°C) process corner, the failure occurred at test sequence number (3, 6, 8, 9). The failure occurred in minimum positive input INP is 400.4mV. At this process corner variation, transistor NMOS and PMOS both set in low mobility, VDD supplies is set to nominal VDD 800mV and low temperature 0°C. The weak condition of both transistor cause longer time required to operate.

For (SS;720mV;0°C) process corner, the failure occurred at test sequence number (5, 8). The failure occurred in minimum positive input INP is 400.4mV and minimum negative input INP is 399.6mV. At this process corner variation, transistor NMOS and PMOS both set in low mobility, VDD supplies is set to 10% lower than nominal VDD 720mV and low temperature 0°C. Transistors take longer time to operate in weak condition and results in low gain at input latch. From the test sequence 3, 5, 6, 8, 9, 11 we can detect the existence of offset voltage in *Schinkel's* comparator which affects the performance while operating in FS and SS process corner, VDD 800mV and 720mV, temperature 0°C condition.

Figure 8 shows the corner simulation result from Paik's comparator circuit in [4]. From the corner simulation result, Paik's comparator able to compare the sequence of input different set according to test setup in Table 1. However, at test sequence 5, 9, 11 which at input different 800µV, we can see the delay occurred in OUTN. The delay will increase the power consumption of the comparator circuit. The details of power consumption during worst case condition are presented in Table 3.

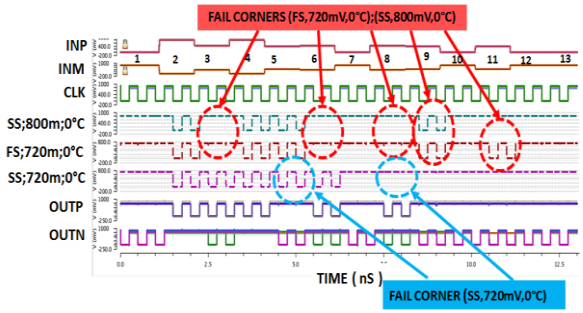


Figure 7. 45 process corners simulation result of *Schinkel's* comparator circuit with failing at 3 process corners which are at (FS;720mV; 0°C), (SS;720mV; 0°C) and (SF;880mV;100°C).

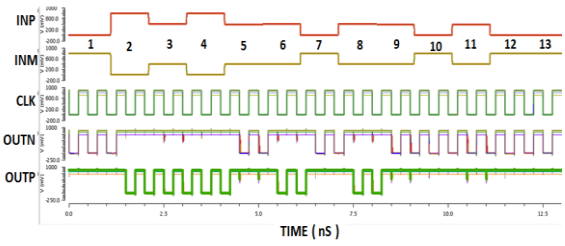
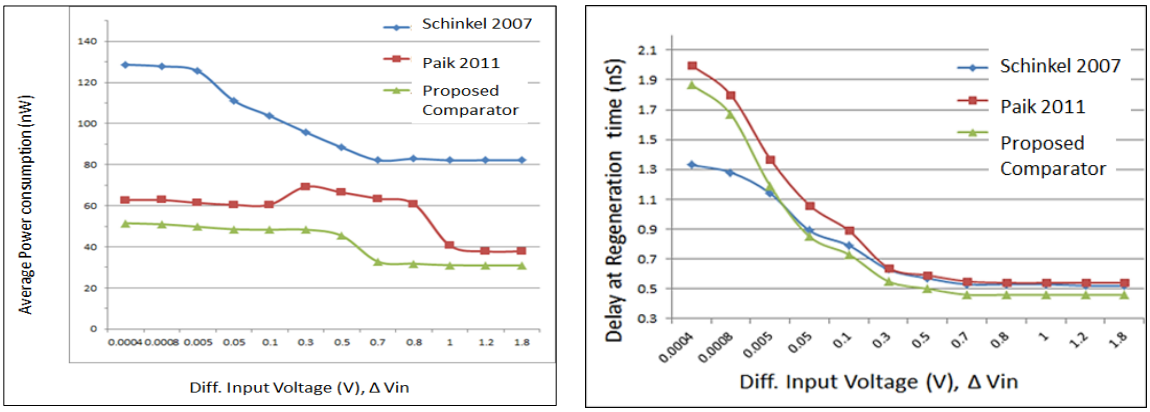


Figure 8. 45 corners simulation result of *Paik's* comparator circuit

The comparison of average power consumption versus different input voltage (ΔVin) at typical corner simulation of proposed comparator with *Paik's* and *Schinkel's* comparator is tabulated in Figure 9 (a). During typical corner simulation, proposed comparator is able to reduce the average power consumption from Schinkel's comparator up to 60% and 18% from Paik's comparator while operating in small ΔVin=800µV. At ΔVin = 800mV, average power consumption of proposed comparator is reduced to 48% from *Paik's* comparator and 62% from *Schinkel's* comparator. Figure 9(b) depicts the simulated regeneration delay versus differential input voltage (ΔVin). At ΔVin= 800µV, delay for proposed comparator is 60% faster than *Schinkel's* comparator and 18% faster than *Paik's* comparator. The delay of all comparators in Figure 9(b) decreases when ΔVin is greater than 0.7V.



(a) (b)

Figure 9. (a) Average power consumption (nW) versus different input voltage (ΔVin) at typical corner simulation, (b) Delay regeneration time (nS) versus different input voltage (ΔVin) at typical corner simulation

3.2. Performance Comparison

Table 3 shows comparison of proposed comparator with *Paik's* and *Schinkel's* comparator. From the 45 process corner simulation, the maximum average power consumption of proposed comparator at (VDD=880mV; Temp.=100°C; Process Corner = FF) is 77nW, which is 87% lower than *Paik's* comparator and 73% lower than *Schinkel's* comparator. Besides the minimum average power consumption at VDD = 720V, temp.= 0°C and SS process corner is 33nW, 26% lower than *Paik's* comparator and 57% lower than *Schinkel's* comparator. The maximum delay of comparator at corner parameter VDD = 880mV, temp. = 100°C, FF process corner is 1.2nS when the input different is 800mV. It reduces to 250pS at VDD=720mV, temp. =0°C, SS process corner [14-26].

Table 3. Performance Comparison over PVT Variation

Comparator Configuration	Schinkel's Comparator	Paik's Comparator	Proposed Comparator
CMOS Technology	0.18 µm	0.18 µm	0.18 µm
Supply Voltage	0.8 V	0.8 V	0.8 V
Clock Frequency	2 MHz	2 MHz	2 MHz
Max. Average Power consumption (VDD=0.88V; Temp. =100°C; Process FF)	288 nW	600 nW	77 nW
Min. Average Power consumption (VDD=0.72V; Temp.= 0°C; Process SS)	87 nW	50 nW	36 nW
Max Regeneration Delay; ΔVin=800mV (VDD = 0.72V; Temp.= 0°C; Process SS)	1.3 nS	1.5 nS	1.2 nS
Min Regeneration Delay ; ΔVin=800mV, (VDD=0.88V; Temp. =100°C; Process FF)	298 pS	293 pS	250 pS

4. CONCLUSION

In this paper, we have presented a verified new dynamic comparator with low voltage and low power performance. Proposed comparator passed all 45 process corner simulations with significant improvement of power consumption during worst case condition compared to *Paik's* and *Schinkel's* comparators. From the

simulation of maximum worst case condition, the average power consumption of proposed comparator is 77nW which is 87% lower than Paik's comparator and 73% lower than Schinkel's comparator. The regeneration delay is improved 7% compared to Schinkel's and 20% than Paik's comparator. At the minimum worst case condition during ΔVin 800μV, average power consumption is 36nW and regeneration delay is 250 pS. In typical condition simulation, the average power consumption of proposed comparator is 69% lower from *Schinkel's* comparator and 18% from *Paik's* comparator. It can be concluded that the performance of proposed comparator improved in term of power consumption during the typical and worst case condition compared to Paik's and Schinkel's comparators. At the same time, the appropriate PVT verification method during the design stage is required in order to verify the robustness of low power low voltage dynamic comparator.

ACKNOWLEDGEMENTS

The authors acknowledge University Putra Malaysia (UPM) for supporting this research work under supervision, fund by FRGS Grant (5540076) Kementerian Pelajaran Malaysia, Institute of Advanced Technology Malaysia (ITMA), Universiti Kuala Lumpur British Malaysia Institute and MIMOS in which this work was possible.

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