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Differential input range driver for SAR ADC measurement setup

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ABSTRACT

Differential successive approximation register (SAR) of analog to digital converter (ADC) requires two balancing input signals that have same amplitude with 180º out of phase. Otherwise, it performs inaccurately and degrades the performance during ADC testing procedure. Therefore, an implementation of AD8139 chip single to differential amplifier was chosen as an ADC driver to generate sufficient differential output for the ADC. The chip was placed on a printed circuit board (PCB) to test the functionality as well as the performance of static and dynamic SAR ADC. The result shows that the single-ended input transform into differential voltage outputs. The amplitudes for the amplifier remain equal and is 180° out of phase for DC and AC voltage input signal. Besides, the fabricated 0.18µm CMOS technology of differential 10-bit SAR ADC is capable of digitising full code digital output and perform 9.5-bit effective number of bit (ENOB) from analog input driving by the ADC driver.

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1. INTRODUCTION

An Analog-to-Digital converter (ADC) is a device to map analog input in real world and translate it into digital signal to be used as a communication tool to electronic device for further application. Successive Approximation Register (SAR) ADC provides a good combination compared with pipeline and ΔΣADC in resolution, power efficiency, conversion speed, area, and circuit complexity [1-3]. The SAR ADC can be characterized by three types of input stage that depend on device functionality, namely, single ended, pseudo differential and fully differential. Fully differential SAR ADC input has advantage in rejecting common-mode noise and interference and increase system performance due to balanced input signal [4-6]. It also offers double dynamic analog voltage input range compared to single ended input. Thus, it is able to digitise from negative to positive analog input voltage over a span of ADC reference voltage.

There are many factors that degrade the ADC performance under all specified condition such as during fabrication, packaging and poorly planned test procedure. A poorly designed PCB layout for testability resulted in test failure or bad-performing designed circuit. In order to test the performance of differential SAR ADC, two analog voltages that have same amplitude with different anti-phase should pump in simultaneously. These voltages can be generated by using function generator but the supply variation of these two inputs might affect the balance of the signals. Moreover, these inputs can be generated by using programmable power supply in test equipment. This technique provides clean input signal without distortion

and noise from supply voltage. However, an extra coding technique and device, such as data acquisition (DAQ) device, need to be attached [7, 8]. Transformer-coupled circuit can also be used as differential input ADC. It provides excellent common mode rejection and distortion; though the drawback of this technique is limited for AC voltages input only [9].

Furthermore, the noise coming from the input signal is highly relative to the ADC performance especially for AC input signal. The signal with noise and distortion degrades the ADC effective number of bit (ENOB) [10, 11]. Consequently, misinterpreted result of designed chip can be avoided by selecting a correct ADC measurement technique. Differential SAR ADC is widely used in medical and industrial application [12, 13]. The digital results that are produced from analog input are valuable, but it depends on its accuracy. If the input signal oscillates, it produces unstable input signal that decreases SAR ADC accuracy. A suitable ADC driver is important to create the differential voltage range and common mode requirement of the converter. To make it simple and precise, differential ADC driver is embedded together in a same test board as the front-end of the SAR ADC as suggested in [14, 15]. Therefore, this paper aims to measure the setup of an ADC driver single to differential amplifier and the capabilities in driving input range of 10-bit SAR ADC output.

2. RESEARCH METHOD

The test chip of differential 10-bit SAR ADC was implemented in 0.18µm CMOS technology fabricated by Silterra Malaysia with the input and output pins were arranged according to the QFN 56-pin package orientation. It comprised of binary weighted digital analog converter (DAC), dynamic comparator and synchronous clock. Figure 1 illustrates the fully differential SAR ADC functionality. SAR ADC accepts two analog input signals (V_{INM} and V_{INP}) that swing from 0 to 1.2V with 0.6V is common mode voltage.

Besides, the reference voltage of the ADC generated from AD3412 voltage reference chip produced 1.2V stable output for full scale reference voltage (V_{REF}). Voltage reference setup for the SAR ADC is shown in Figure 2. Meanwhile, 0.6V voltage common mode (V_{CM}) is generated by dividing the 1.2V output using voltage divider technique. The V_{CM} that always half of V_{REF} ($V_{REF}/2$) is produced by tuning the divider resistor R27 and R28. The V_{REF} and V_{CM} output is connected to AD8616 buffer to maintain the voltage drive capability for ADC.

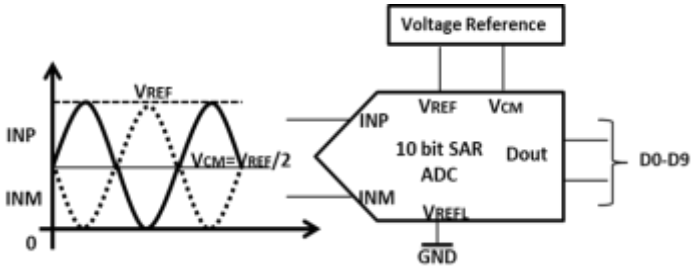

Figure 1. Fully differential SAR ADC system

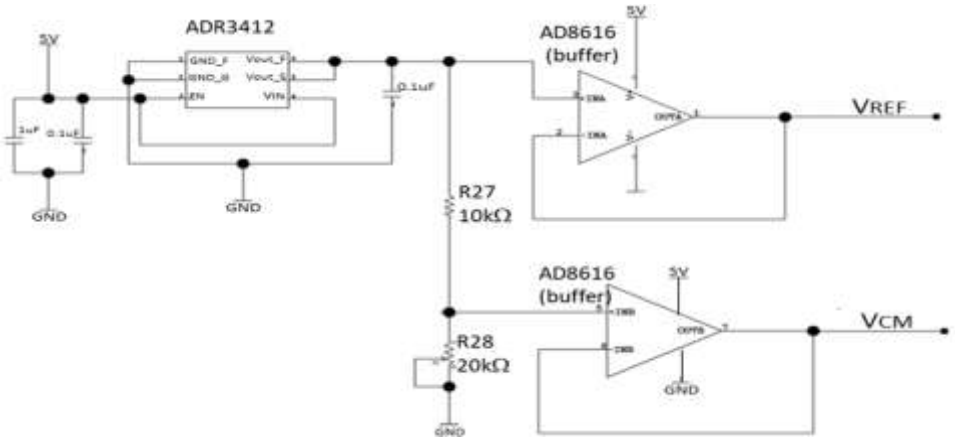

Figure 2. Voltage reference setup for SAR ADC

2.1. ADC Driver for Differential SAR ADC

The purpose of the ADC driver is to transfer source signal to the SAR ADC input, conditioning it as necessary to optimize performance, while minimizing added distortion, noise, and settling time errors [16]. For this test procedure, AD8139 differential amplifier was chosen to transform the single-ended analog signal into a differential ADC input. It was designed to provide two closely balance differential outputs in response to single ended input signals that has advantage in ultra low noise and high performance rail-to-rail output [17]. This chip characterization is the most suitable input driver for the differential SAR ADC due to the main feature of differential input that requires an amplitude and phase balance. It means the measurement of the amplitude equals to two outputs with 180° phase balance difference [18].

Figure 3 shows the test setup of single to differential ADC driver. A driver is used in a precise sampler or a harmonic analyser to convert the single-ended input AC or DC voltage into differential voltages. An operational amplifier combined with an RC filter should be completely right to the ADC for minimising the noise that disturbs the input voltage. By giving DC input signal, the output voltage of the amplifier generates the ADC input voltage range for full scale digital output. Thus, for an AC perspective, the amplifier should have flat bandwidth and gain such that the output signal is not attenuated by the amplifier's frequency response. It could minimise noise and distortion levels that do not affect the ADC's performance [19].

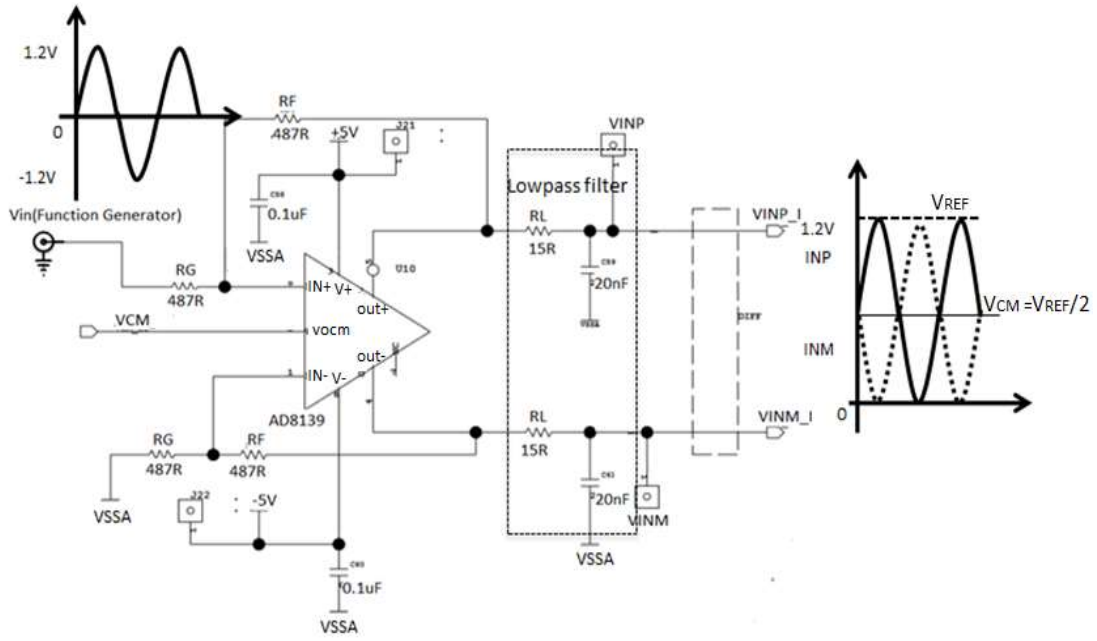

Figure 3. ADR8139 test setup

To minimise the influence of noise effect from frequency ringing in the transient response, this differential signals are filtered by lowpass filter RC network before connecting to the ADC input pin. The filter is placed between the amplifier and ADC input to maintain the bandwidth of the signal drive to the ADC. Moreover, the filter also separates the capacitive load of the ADC input from the amplifier to uphold amplifier phase margin and stability from being attenuated by the transient-charging glitches on the ADC input while the sample capacitance is switched. The value of RC determines the -3dB frequency, whereas F-3dB is given by the (1).

$$F_{-3dB} = \frac{1}{2\pi RC} \quad (1)$$

In addition, the main function of differential amplifier is to reject signals that are common to both inputs. The resistors that are connected to the driver amplifier must be chosen wisely to prevent error at the amplifier output voltage. The error triggers part of the V_{CM} to amplify the difference of the input signal. Thus, the voltage output of V_{INM} and V_{IN} are unable to be distinguished from the actual signal. The common mode voltage pin is connected to the V_{CM} output that is generated from voltage reference circuit to fulfill the condition of SAR ADC input common mode level. The basic equation to find input resistance when the

feedback factors are matched is derived in (2), where R_{IN} is the input impedance of the total value of resistance.

$$R_{IN} = \left(\frac{R_G}{1 - \frac{R_F}{2\,x\,(R_G + R_F)}} \right) \quad (2)$$

This is a general calculation for the termination resistance with amplifier gain equations are based on the assumption of a zero-impedance input source [19]. The functionality of ADR8139 test setup as illustrated in Figure 4 was simulated using Lt-Spice software and the output voltage was observed. By referring to the differential output, it was observed that the signals transformed only 86% from the full input signal. It caused the SAR ADC to digitize with 49 missing code for Low Significant Bit (LSB) and Most Significant Bit (MSB), whereas 1LSB equals to 2.34mV [0.113V/2.34mV].

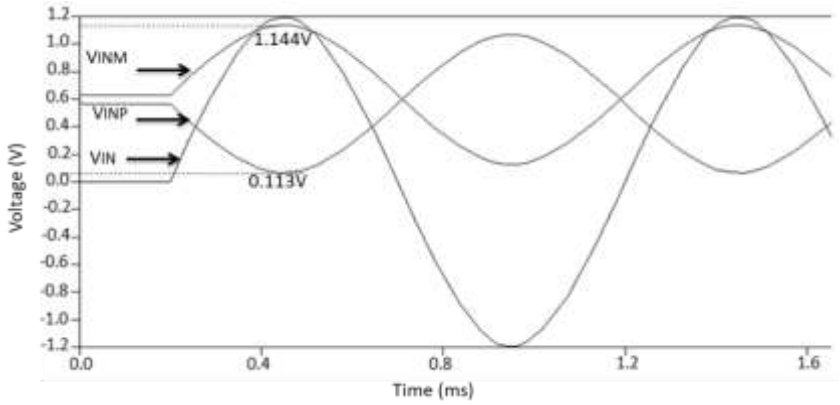

Figure 4. Simulation waveform of AD8139

This result is contributed by the mismatched impedance in the feedback networks affected by 50Ω resistive line termination placed at the load end before being connected to the function generator. This is the main aspect needs to be taken into account in designing the test setup of ADC driver. Thus, the impedance of the amplifier test setup is presented in Figure 5.

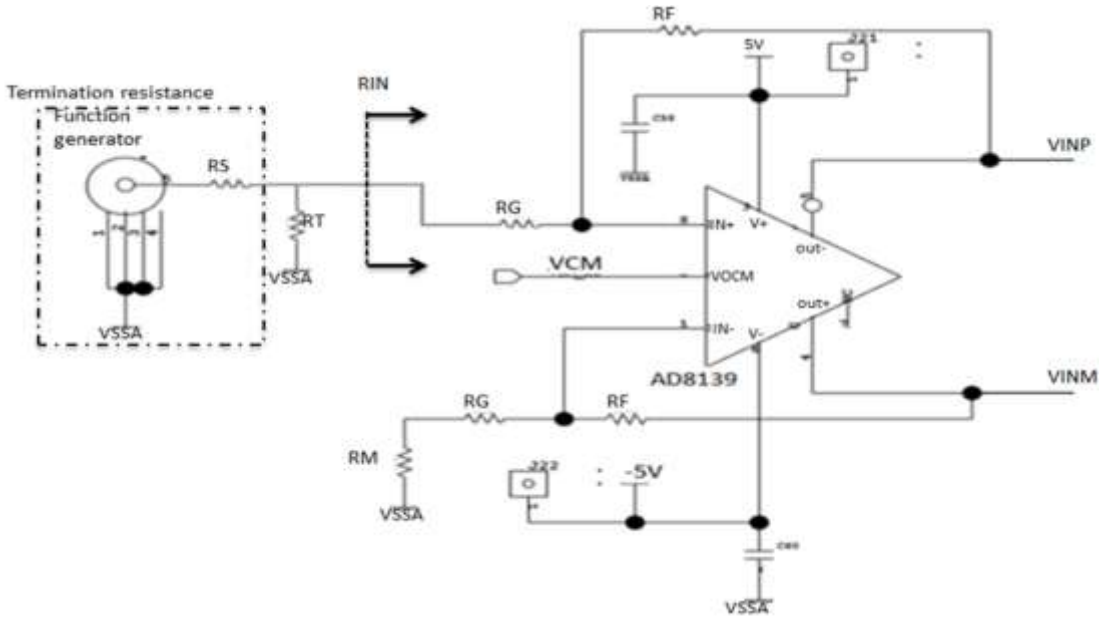

Figure 5. Test setup AD8139 with line termination

To match the circuit input impedance between source impedance (R_S) and feedback resistor, RT//RIN = RS is set with RM = RS//RT. The value of R_{IN} can be calculated as shown in (3) and (4) [19].

$$B_1 = \frac{R_G}{R_G+R_F} \quad (3)$$

$$B_2 = \frac{R_G+R_M}{R_G+R_F+R_M} \quad (4)$$

Then, input resistance (R_{IN}) is determined by using (5).

$$R_{IN} = \frac{2R_G+R_M(1-B_2)}{1+B_2} \quad (5)$$

The value of recommended resistor can be referred to in AD8139 data sheet [17]. Otherwise, the resistor value can be calculated by using differential amplifier calculator tools, provided by downloadable ADIsimDiffAmpTM that can perform the calculation within few seconds.

2.2. Measurement Setup Procedure

Printed circuit board was designed to test the functionality of the SAR ADC. The test setup of the SAR ADC is shown in Figure 6. An analog input signal is generated from function generator that is provided by Agilent. This signal is applied through the ADC driver that transforms to the bipolar voltage into differential input V_{INP} and V_{INM} of SAR ADC. The differential inputs should be out-of-phase voltages and symmetrical each other to be driven simultaneously. An input clock of 2MHz of the ADC is generated using arbitrary waveform from function generator. It creates 50% duty-cycle of square shape sampling per conversion. The digital output is observed using Agilent logic analyser (model 16900). The supply voltage of the chip is 1.8V, 3.3V for digital part and ±5V for the AD8139.

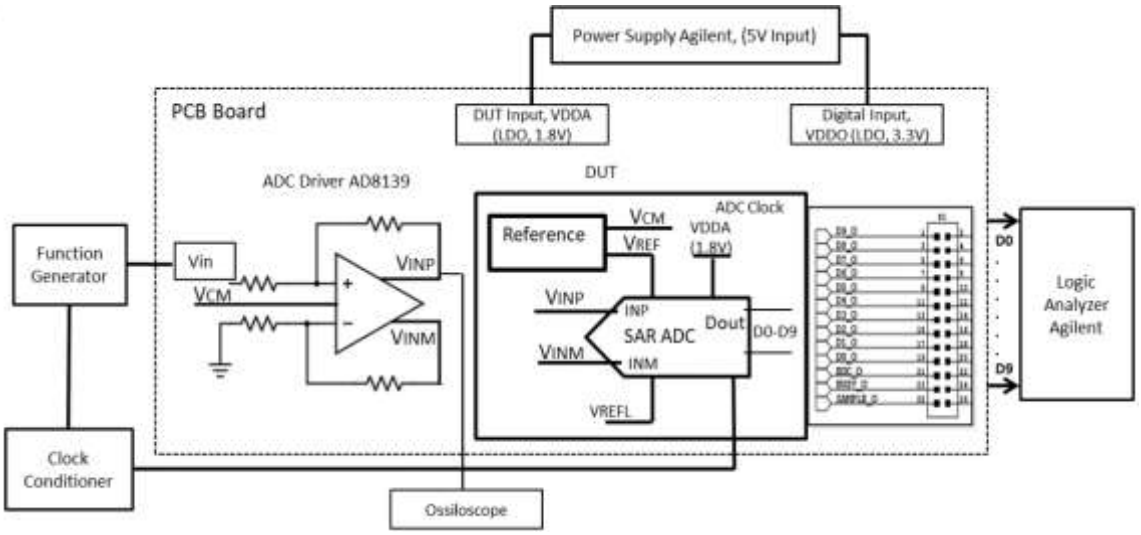

Figure 6. Scheme of the test setup

PCB layout is an important component in designing the test board. Otherwise, the performance of the device under test (DUT) could be degraded because of the poor layout design. Figure 7 shows the test board of the DUT. The test board was arranged by separating components between analog part and digital I/O part to minimise signal interference that can affect the test functionality. The performance of ADC driver was tested by embedding the AD8139 on a test board. The symmetrical resistors RF and RG were chosen to perform low distortion differential output balance and good Common mode Rejection Ratio (CMRR). The smallest possible resistor value RF is used in order to reduce phase shift due to the pole made by RF and summing node capacitance [14]. The smallest resistance minimises board's parasitic elements that prevents the phase margin from contributing ringing at output voltage. Besides, signal from power supply is exposed to the noise before entering the input circuit. Thus, by placing power supply bypass capacitors close to the amplifier pins ensures that a low impedance path is provided to yield the disturbing noise.

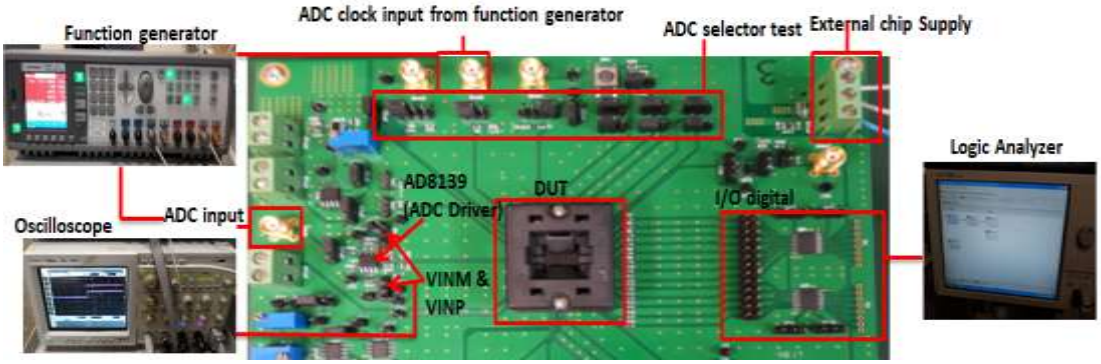

Figure 7. The test board of test procedure

3. RESULTS AND ANALYSIS

The functionality of AD8139 as a driver amplifier was evaluated by ramping ±1.2V linear triangular DC supply that used as an input of the driver. The driver was also tested by applying an AC sinusoidal input ±1.2V peak-to-peak voltage. The differential V_{INP} and V_{INM} output were captured and measured using an ossiloscope as shown in Figure 8 for DC input. Meanwhile, the output for the sinusoidal voltage input is shown in Figure 9.

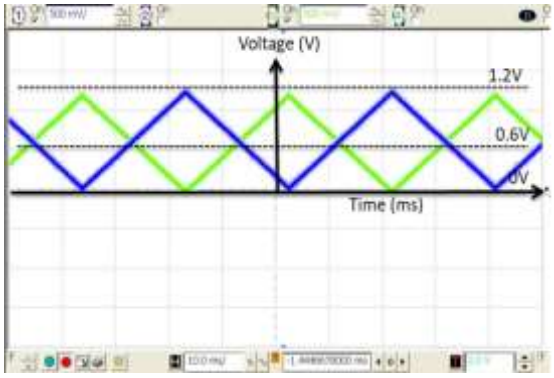

Figure 8. Differential output for DC input voltage

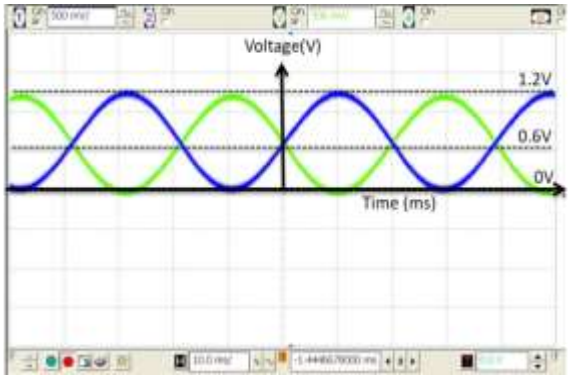

Figure 9. Differential output for sinusoidal input voltage

The differential waveforms for DC and AC signals indicate that both of them are equal in amplitude with minimum noise and 180º in phase with corresponds to a common mode voltage as expected. It swings within the range of ±1.2V that centred on 0.6V common mode voltage of the amplifier. It proves that the differential output waveforms were complementary drive and symmetrical in amplitude and 180º phase difference [20]. Table 1 summarises the SAR ADC digitised code from Logic Analyzer corresponding to differential input. These results estimate that the positive analog voltage input produced digital output range from $(0)_{12}$ to $(511)_{12}$. The digital output for negative analog voltage input ranging from $(512)_{12}$ to $(1023)_{12}$ was obtained.

Table 1. SAR ADC Digitized Code Equivalent to Input Driver

Input Driver (V)	VINM (V)	VINP (V)	ADC Code (decimal)
1.2	1.2	0	0
0	0.6	0.6	512
-1.2	0	1.2	1023

The performance of SAR ADC was tested using static and dynamic parameters. Static test specifications provide an information on the device behaviour at a very low frequency input signal. A linear

triangular waveform with 7Hz frequency was ramped as an input of SAR ADC driver to produce output codes ranging from 0 to full code. The SAR ADC took 6.5µs for one conversion cycle until the end-of conversion signal (EOC) goes high. The DC input that contains of length 76701 samples (78 samples/ code) was ramped from -1.2V to 1.2V and was applied to the SAR ADC. Then, the digital output was extracted from logic analyser and analysed using histogram method calculated in Matlab. The graph illustrated in Figure 10 specifies the number of samples and the digital output respectively that was collected from histogram bin produced by Matlab. This result interprets that the ADC converted the input signal with no missing code of digital output. The results can be validated by comparing with previous work [7].

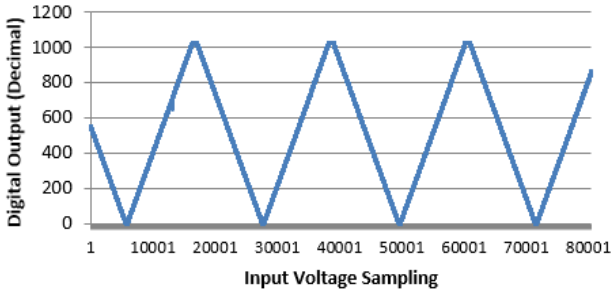

Figure 10. SAR ADC digitized output

The dynamic test was performed to investigate the SAR ADC error that is related to the function of frequency. Noise and distortion from power supply eventually become the two main specifications that degrade the performance of the ADC. The noise may come from any factor such as PCB board layout, cable, voltage reference circuit and also from ADC driver. Hence, the ADC driver should be carefully setup to minimise the influence of noise to the input SAR ADC. In dynamic performance parameter testing, sine-fit testing technique is used with full scale sinusoidal performing as an input of ADC driver. Then, the data was analysed in Fast Fourier Transform (FFT) in Matlab to determine an effective number of bit (ENOB). The analysis refers to the IEEE standard and terminology and test methods [21]. The SAR ADC produced an ENOB equals to 9.5-bit. This result shows good performance of SAR ADC comparatively with previous work in [22-26].

4. CONCLUSION

The driver circuit and test setup for fully differential SAR ADC is presented in this paper. The resistance of feedback network was chosen carefully to prevent signal distortion at the output voltage. To minimise the noise coming from ADC driver, the low pass filter was inserted after the differential amplifier. The measurement result shows the AD8139 chip single to differential amplifier produced two outputs of the same amplitude peak-to-peak voltage which is 180° out of phase. Besides, the output of the SAR ADC was measured without any missing code. The dynamic test parameter shows the 9.5-bit of ENOB. In conclusion, this result proves that the AD8139 is suitable to be used as ADC driver for differential 10-bit SAR ADC.

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Izhal bin Abdul Halin was born in Kuala Lumpur in 1975. He received his B.Sc in Electrical Engineering from the University of Hartford, CT, USA in 1999. Upon graduation, he is appointed as a tutor for Microelectronics Engineering, Universiti Putra Malaysia and obtained his M.Sc in Microelectronics Engineering in 2002 from Unversiti Putra Malaysia. He then further his studies in Nanovision Engineering and obtained his D.Eng from Shizuoka University, Japan in 2006. He currently is a Senior Lecturer at the Department of Electrical and Electronics Engineering, Universiti Putra Malaysia where his research interest is in CMOS circuits, Renewable Energy and Application of Electronics in Agriculture.