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An analysis of ADPLL applications in various fields

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Article Info	ABSTRACT
	ADPLL is now an essential component in applications like wireless sensor networks, Internet of things, health care applications, agricultural applications, etc, and also due the requirement of digital implementation by the industries. ADPLL consists of a phase detector, loop filter and digital controlled oscillator. The conventional PLL and digital PLL used for frequency synthesis, clock recovery circuit and synchronization give imprecise performance with respect to reliability, speed, power consumption, noise, locking speed, cost, etc. ADPLL overcomes the drawbacks of conventional PLL and digital PLL. In this paper, different approaches followed in All Digital Phase Locked Loop (ADPLL) for various applications are reviewed and their performance is compared based on components, modulation functions, frequency range, power utilization etc. In addition, an ADPLL with wide tuning range and frequency resolution is designed and implemented using automatic placement and routing, time to digital converter, digital loop filter and ring based oscillator. The ADPLL outputs and the results are analyzed with micro wind tool. The design gives a frequency range from 1.0-5.5GHz with low power consumption and it can also be used for Clock generation applications.

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1. INTRODUCTION

Due to the developments in CMOS technology, the ratio between the supply voltage and threshold voltage have become lesser. VCO based inverters or differential delay cell is more popular for low power ADPLL. The main drawbacks in conventional PLL are complex implementation and low locking speed. When analog blocks are present in mixed signal ICs, then the requirement of redesign is essential. So the analog circuitry reduction improves the redesign [1] Nowadays All digital PLL replaces conventional PLL. ADPLL is used to lock the input reference signal with the signal coming from the oscillator output. ADPLL achieves fast frequency acquisition as the frequency of controlled oscillator is tuned by digital codes [2].

ADPLL consists of digital phase detector, loop filter, Digital controlled oscillator. ADPLL can be utilized in two ways- Fractional –N-divider based and counter based. The counter based ADPLL is used in Wireless PAN and in some ultra low power applications and fractional–N-divider based ADPLL is used in IOT applications, health monitoring applications, etc. All digital PLL optimizes important parameters such as power dissipation, area and also it enhances testability and programmability compared to analog PLL.

IoT connects sensors to retrieve data and transmits the information using internet [3]. IoT gives benefits to the user by integrating computer and physical world [4]. In wireless sensor node applications, ADPLL is used for sensor signal modulation and also transmits the data to the base station. The important component in IoT based wireless sensor applications is local oscillator which is used for up-conversion and down conversion functions. Earlier PLL was used for generating local oscillator signal. Now a day's ADPLL

replaces PLL because it generates local oscillator signal with fast locking, less noise, low power consumption, etc. for wireless based IoT applications. ADPLL based systems will improve the data rate and communication quality because DCO is always locked by ADPLL.

Phase detector block in ADPLL is a good comparator. Some of the high speed comparators used for ADC and DAC circuits consume high power with large chip area [5]. So these comparators require separate power reduction techniques. The Bang Bang phase detector based ADPLL consumes only low power without power reduction techniques. ADPLL is an essential component in wireless based IOT and wired sensors and its various applications are medical and agricultural applications, communication, mobile applications, measurement system, security control and power applications, etc. ADPLL can be used in a circuit to perform important functions like modulation, clock recovery circuit, frequency synthesis, signal conversion, etc. The paper reviews different applications of ADPLL, combination of components used in ADPLL, algorithm, acquisition methodology, locking time, phase noise, power consumption, etc.

2.   REVIEW OF ADPLL APPLICATIONS
2.1.   ADPLL for Medical Applications
Tino Copani et al presented a small-power transceiver for medical systems [6]. The system will do important functions such as a signal reception for wake-up, BFSK based reception, and transmission respectively. The transmitter consists of full digital frequency-locked loop to force power amplification. The ADFLL uses an injection locked power oscillator for low power consumption. The output transmitter power is 5 dBm with 2.9 mW power consumption. ADPLL is used as the on-chip synthesizer for two purposes: high reconfigurability and low power utilization.

Waleed Khalil et al present a frequency synthesizer based on ADFLL for medical band applications [7]. The DCO achieves 9.5Hz frequency resolution, across the ISM 400–410-MHz band. The frequency-based approach removes the difficulty associated with PLLs. FDC approach used in this system utilizes low power, so the system becomes ultra low power system. The ADFLL total area is 0.14-mm dies with a 1.8-V supply.

Qi Zhang et al presented an ADPLL based transmitter for medical applications [8]. The important blocks are synthesizer, a boosted signal part and a processor. To get maximum energy, TX utilizes the VCO mode and the PLL mode. The PLL mode improves the data rate by presetting technique.

Hae-Moon Seo et al developed a transceiver for sensor arrangement [9]. The system important component is synthesizer with on chip VCO. The chip utilizes power consumption of 25 mW .This designed system is used for Personal Area Networks.

Simon Cimin Li et al presented an intermediate frequency (IF) receiver for medical applications [10]. An amplifier and frequency based modulator are the important blocks in IF section. The author used LC based VCO in this circuit. The receiver section gives frequency range of 915 MHz and 15 dB gain.

Shoichi Masui et al presented an energy efficient silicon on the chip [11]. RF wireless transceiver is the main component used in health care applications. The ADPLL based transmitter is used to support different modulation schemes. The data rate for the transceiver is 3.6 Mb/s .The system gives low power consumption and fidelity, so that it is used for a wide range of medical sensor node applications.

Xue-jiao Zhang et al present a system based on ADPLL [12]. The system is designed with three different modes for avoiding unwanted power utilization. ADPLL consists of phase accumulator, PI filter, DCO and Variable phase accumulator. The biological sensors are attached to the human body. During emergency situations, the system is enabled by abnormal signal to transmit the emergency situation information to SOS. The collected information is modulated by ADPLL based RF frequency transmitter. The entire system is targeted for elderly people. The system can also be used in occasions of natural disasters.

Alan chi wai wong et al presented a system for biotelemetry and wireless sensor applications [13]. In the wireless transceiver section, ADPLL consist of a charge pump, filter and LC based VCO. ADPLL is used to synthesize local oscillator frequencies. The ADPLL synthesizer reduces the locking time. The current consumption of the transceiver is 2.6mA .The transceiver uses GFSK modulation for making wireless connection between sensor points and base station in a network.

Baoyong chi et al presented a transceiver for endoscopy appliance [14]. The Local Oscillator signals are generated by differential negative resistance LC oscillator. The oscillator utilizes low power consumption with comfortable phase noise performance. The system consists of an amplifier, gain controller, ASK demodulator and ADPLL.

Nezhad Ahmadi et al designed a 400 MHz transceiver for wireless hearing aid communication systems [15]. ADPLL based frequency synthesizer generates a LO signal with an on chip loop filter. A cross coupled LC oscillator is used and it consumes low power.

Inferences

Most authors utilize ADPLL for frequency synthesizer and to do modulation for health care applications. The parameters considered are low power consumption, high frequency range (ISM Band) and less locking time. A fractional type ADPLL is used by an author for generating Local oscillator signal and modulation. ADPLL is used for BFSK direct-digital modulation utilizing ring oscillator DCO.

For reducing power consumption, injection locked oscillator is used. Ring oscillator is also preferred over LC oscillator for its low power consumption and small area utilization. The presetting technique presets the carrier frequency in DCO and improves the data rate. The low power utilization and flexibility of fully integrated SOC pave the way for a wide range of medical sensor node applications.

In wireless endoscopy applications, ADPLL based transceiver placed inside the capsule consume low power. The integration technique reduces the capsule size, displaying images with good resolution.

2.2. ADPLL for Wireless and Wireless Sensor Applications

Robert Bogdan Staszewsk et al developed a mathematical model for a phase field ADPLL [16] targeted for GSM applications. Denis.C.Daly et al presented transceiver for short range wireless sensor networks [17]. The 916.5 MHz On-Off keying transceiver operates on a channel with a center frequency of 916.5MHz. The transmitter consumes power in the range of 3.8mW to 9.1mW. The locking time is less compared to the previous models.

Philipp Greiner et al presented a new approach for a wireless transmitter [18]. The PLL is designed for generating higher frequencies. Digital PLL consists of a charge pump detector, filter and fractional Ring based DCO. The system utilizes less number of external devices.

David Ruffieux et al presented a design for biomedical applications [19]. The Bulk acoustic wave merits are used in this system to obtain a less noise fixed frequency DCO. ADPLL achieves a fast wake up time. The frequency synthesizer needs an external crystal. The DCO gives a 125 dBc/Hz at a frequency of 1 MHz offset.

Inferences

BAW resonators based oscillators achieve minimum phase noise with less power consumption and the tuning range is also low. ADPLL along with resonators increases the tuning range. ADPLL based transceiver with some microelectromechanical devices can be used in some important areas such as WSN, WBAN and medical applications. ADPLL provides higher data rate in these applications. ADPLL is used to generate high frequencies in wireless sensor applications.

2.3. ADPLL Applications in Communications

Eugene koskin et al proposed an ADPLL system to deliver distributed clocking signal [20] which achieves synchronization in frequency and phase for transmission related to antenna arrays.

David,M,Moore et al proposed an wide tuning range ADPLL with automatic place and route technology, TDC and phase interpolation technique which gives wide tuning range and frequency resolution [21]. ADPLL is used as a clock generator and isfabricated in a 14 nm FinFET process.

Marijn Verbeke et al presented a first 25 Gb/s ADPLL recovery circuit [22]. The transceiver is used for extracting synchronous clock and recovering received data. A four stage ring is used in oscillator. The total circuit consumes a power of 46 mW.

Wanghua Wu Marvell et al proposed a mm-wave digital transmitter for FMCW radar applications [23]. ADPLL utilizes a 60 GHz DCO for this application. In earlier techniques, loop bandwidth is required to be more for accommodating modulation. So the author proposed a digitally-intensive modulator operating at mm-wave frequencies.

Ching-Che Chung et al proposed an ADPLL for video pixel [24]. The output pixel clock should have an in-phase relationship with the horizontal synchronization signal to avoid blurry image. The system is designed in such a way to perform the fast phase tracking.

Ching-Che Chung et al presented a full digital frequency synthesizer for multimedia interface application [25]. The proposed frequency synthesizer achieves locking in short duration and also stabilized loop. The frequency search algorithm is used in ADPLL to achieve low-jitter performance.

Inferences

High speed data recovery circuit is needed in transceiver for optical networks. Earlier techniques give drawbacks like jitter problems and pulse distortion. For this high frequency ADPLL can be used. The design achieves phase-locking in 37.5 ns. This circuit can be also used in photonic switching.

For antenna arrays operating synchronously, each antenna should receive a common clocking signal. It is a tough task of delivering a clocking signal to a large chip. ADPLL produces a common clocking signal

and achieves a frequency and phase synchronization with few restrictions on the control parameters. ADPLL can be used for synchronization in antenna applications.

2.4. ADPLL based Measurement System & SOC Applications

Robert Neal Dean et al presented a DFLL for Capacitance Measurement [26]. A relaxation oscillator converts capacitance to frequency. The relationship existing between output frequency and input capacitance is inverse. The measurement system has been demonstrated using a PCB fringing field sensor.

Dennis M. Fischette et al presented a circuit for the characterization of PLL response [27]. The ADPLL consists of charge pump based phase frequency detector, loop filter and ring based VCO. The system estimates PLL bandwidth with minimum time. It is used for wafer to package level testing.

Jim Dunning, et al presented an ADPLL suitable for high performance microprocessors [28]. The frequency range of DCO is 50-550 MHz. The ADPLL is designed with separate locking scheme for frequency and phase. ADPLL for microprocessor applications need high-volume, high-performance with low-power.

Po-Hui Yang et al present a controlled loop for SOC [29]. Utilising the ability of SOC to increase the clock frequency to a high level, the author designs a clock generator by using PLL and PWCL so that simultaneous adjustment is possible in phase locking and pulse width. The test chip is designed with a very low voltage of about 1.8V.

Seunghyeon Ki et al presented a RF transceiver for TV [30]. The phase interpolator circuit is used to generate two different phases of local oscillator signals. The maximum frequency obtained is 806 MHz.

Inferences

ADPLL can be used as a frequency synthesizer for high performance microprocessors. The author optimizes phase acquisition mode and frequency acquisition mode individually. ADPLL designed can be used in high performance microprocessors with low power consumption. Some authors have aimed for lesser PLL response time with less expense. The loop response of the PLL is summarized by its bandwidth and peak characteristics. ADPLL is also used in pulse width control loop for controlling the duty cycle of signal. For this, the important constraints followed are low voltage and clock pulse width adjusted in a wider way. ADPLL provides Phase locking and pulse width adjustment and the two operations can be done simultaneously.

2.5. ADPLL for IOT & BLE Applications

Ming Ding et al presented a wakeup timer for the (IoT applications [31]. ADPLL consists of a bang-bang DFLL architecture and a self-biased DCO. This is designed with less area occupancy, low power consumption and high resolution. The system achieves high energy 0.43 pJ/cycle with low voltage 0.7 V.

Yao-Hong Liu et al presented a DPLL for IoT applications [32]. A snapshot time-to-digital converter is used to achieve improvement in gain which reduces power consumption. It consists of phase selector, Digital loop filter, LC based DCO and an LMS algorithm. The Sub Sampling-DPLL designed for IoT purpose with low cost, and the frequency in the range of 1.7-2.7 GHz.

David E. Bellasi et al presented an ADPLL based clock generation for IoT sensors [33]. The idea of Transient Clocking is used by an author to stabilize the supply voltage. The system gives a maximum frequency of 2.4 GHz. The important modules of ADFLL are DCO, FDC, a filter and a clock divider.

Feng-Wei Kuo et al presented a minimum power transceiver for IoT [34]. ADPLL based transmitter (TX) utilizes a current-source (DC) and amplification section for achieving high efficiency. The entire system utilizes low power with the receiver side consuming 2.75 mW and transmitter side consuming 3.7 mW.

Masoud Babaie et al proposed a new transmitter architecture to operate on a low supply voltage [35]. The DCO with switching current sources is used. The entire system consumes 3.6 mW/5.5 mW in Bluetooth Low-Energy mode. The scaling methodology is used to reduce the power.

Akihide Sai et al proposed a hybrid-loop receiver structure based on ADPLL [36]. The Time to Digital converter will improve the receiver dynamic range. The ADC reduces the power utilization of the receiver. Interference reduction necessary for BLE applications is achieved with ADPLL.

SeongJin Oh et al proposed a FSK transmitter with ADPLL for Bluetooth low energy application [37]. The functional blocks are DPLL components, modulation section and amplifier section. The transmitter power utilization is 3.9 mW and at the same time output power is 1.6 dBm.

Naser Pourmousavian et al proposed a very low voltage utilization fractional-N ADPLL [38]. The ADPLL undergoes a two-point modulation. An extra loop to the PLL indicate PVT variations and also to obtain a set resolution for TDC. ADPLL consists of TDC Loop filter, Ring type DCO, DC-DC doubler. The power is only 0.8 mW, due to the switching possibility of DCO to the second loop.

Inferences

In the wake up timer based on frequency locked loop, accurate frequency and improvement of stability is achieved by the usage of chopping. Chopping is also used to diminish the noise to enhance the frequency resolution. The combination of chopped comparator and a self-biased DCO gives good progress in stability.

The author used the sub-sampling technique in digital PLLs to reduce the TDC operation speed. The author utilizes a self gating technique to reduce the sampling rate. The divider-less ADPLLs speed up frequency acquisition. The frequency extension is possible in the digital PLL sub sampling technique compared to conventional PLL. The author utilizes ADFLL instead of ADPLL for generic IoT applications.

2.6. ADPLL for Security Control/ Power Operations

Hua Geng et al proposed a novel Full digital PLL method to predict the phase detection [39]. The features of an ADPLL are broad track-in range and short duration draw time, with low cost. The PI structure used in ADPLL reduces the steady state phase error.

Hua Geng et al proposed a ADPLL for grid interface converters [40]. The important functions of this converter are detecting the frequency and phase with zero crossings in voltage. The high clock frequency reduces the phase error and pulse jitter. The system is used in the grid fault situation.

Ching-Che Chung et al proposed a spread spectrum clock generator [41], provides an accurate programmable spreading ratio. For maintaining the frequency stability, a fast-relocked mechanism is proposed. The EMI decline is 14.61 dB at 270 MHz. The system consists of ADPLL and spreading ratio detector.

Jaehyeok Yang et al proposed a spread-spectrum based clock generator [42]. The design utilizes two modulation profiles. This combination achieves a balance between EMI fall and jitter creation. The system consists of a ADPLL, phase rotator and PRBS generator based modulation controller. The system computed EMI reduction.

I-Ting Lee et al proposed a de spreading clock generator [43]. The system consists of a conventional ADPLL, a frequency generation circuit, and a checking circuit. ADPLL consists of divider, TDC, loop filter, DCO, delta-sigma modulator (DSM). The de - spreading clock generator operates without passive filters. The same authors also proposed a spreading generator [44]. The spreading is realized by simply switching the divider. A self-calibration technique gives a triangular profile frequency and relaxes the PVT variations. The power rakishness is 23.4 mW.

Duo Sheng etal proposed a portable spreading clock generator [45]. This clock generator provides different EMI loss for different cases. The proposed method gives a good power saving with DCO. The system consists of an ADPLL and frequency dividers and achieves lessening of 9.5 dB EMI.

Inferences

In grid voltage phase detection, analog PLL techniques are weak in tracking level, locking range and jitter performance. So the author utilizes ADPLL with a feed forward control loop for enhancing the above parameters. The PI structure filter reduces output jitter and no static error. ADPLL designed for grid voltage converters improving the tracking speed with variable frequency. It is also used in low-switching converter applications.

The spreading ratio based ADPLL provides good security related to signal. The spreading ratio depends on DCO resolution. For this reason only spread spectrum based clock generator cannot provide a correct spreading ratio. Most authors utilize triangulation modulation profile because of its performance and implementation simplicity. For EMI reduction, spreading clock generator is widely used because it is a cost and area efficient solution. The author mentioned the importance of non spreading clock as it is needed in applications like digital signal processors, data converters, etc. The de spreading based clock generator can produce a non spreading clock without additional components and saves cost. The author used self calibration technique to tolerate the PVT variation.

2.7. ADPLL for Mobile Phones

Robert Bogdan Staszewsk et al proposed new multi rate ADPLL featuring phase/frequency modulation capability [46]. ADPLL supports high data rate modulation. The proposed ADPLL comprises a DCO and a TDC for phase detection. The RF performance has a large margin to the 3GPP GSM specifications.

Another ADPLL proposed by the authors utilizes a gain calibration technique and allows direct wideband frequency modulation without a support from the loop bandwidth. The technique is adopted in a polar-modulation transmitter for WCDMA systems [47].

Feng-Wei Kuo et al proposed an ADPLL for radios [48]. The system keeps up a 2-point modulation and puts away 11.5mW. ADPLL reduces the TDC range so that linearity is improved. The design supports multi band operation.

Robert Bogdan Staszewski et al is the first author to present the full digital PLL related to mobile applications [49]. ADPLL provides the frequency modulation capability. ADPLL provides frequency synthesis with TDC, phase detector, filter and DCO. The transmitter achieves GMSK modulation at 20 MHz offset. They also proposed a Gaussian based shift keying for wireless RF transmitters [50]. The current utilization is 25 mA with low supply. ADPLL consists of a variable phase accumulator, TDC, filter and DCO.

Inferences

In mobile applications, to extend the DCO range and improvement in frequency modulation, step acquisition bits are engaged. In the ADPLL modulating path, accurate arrangement of the DCO gain allows direct wideband frequency modulation. The author utilizes iterative algorithm in the adaptation technique. ADPLL is used for frequency modulation and frequency synthesis. The important advantage of ADPLL over conventional PLL is wide band modulation, high data rate, low power consumption, programmability and built-in self testability.

3. COMPARISON OF ADPLL IN DIFFERENT FIELDS

The following tables 1 till 5 show the comparison of components of ADPLL used in different fields such as mobile phones, IoT/BLE, Power control and security, Medical applications, communication applications, etc. The comparison is based on important constraints like Phase detector, loop filter, Digital control oscillator, output frequency and the VLSI chip level constraints such as area, power, etc.

Table 1. Mobile Phones and Security

Paper No.	[47]	[49]	[50]	[48]
Phase detector	TDC	TDC	TDC	phase detector
LOOP filter	Digital		Digital	Digital
DCO	Ring type	class-F DCO	LC varactor oscillator	Varactor based oscillator
Current	32 mA		42 mA	--
Power consumption	-------	11.5mW	6 dBm	1.2mW.
Output frequency	400 KHz	2 125 MHz		27-54 MHz
function of ADPLL	Phase frequency Modulation	Data frequency Modulation	Wideband frequency modulation	Clock and data recovery
Advantages	--	Multi band operation, Wide tuning range		Low power ,area, good EMI reductions
Application	Mobile	Mobile	Mobile	SoC , microprocessor based system

Table 2. For IOT & BLE

Paper No.	[35]	[33]	[34]	[37]	[38]
Phase detector	Time to digital converter	**Snapshot** Time to digital converter	Frequency to digital converter	Time to digital converter	Time to digital converter
LOOP filter	Digital Loop	Digital Loop	Dig ital	Digital	Digital
DCO	Switched Current source DCO	Cross coupled LC	Ring type	LC based oscillator	LC based oscillator
Algorithm /Methods		Sub sampling	Transient clocking	-------	--
Modulation	GFSK	GFSK	-------		FSK
Power consumption	TX:3.4 mW RX:2.75 mW	1.18 mW	1.2 μw	5.5 mW.	3..9mW(TX)
Output frequency	5 GHz	1.7 t0 2.7 GHz	2.4 GHZ	2.2 to 2.4 GHz	2.4 GHz
Advantages	Ultra low power , Good power efficency	Low power consumption, low cost ,		Enhance the interference tolerance & Low power	Low power consumption Direct Modulation
Application	IoT, BLE	IoT	IoT	BLE	BLE

Table 3. Power Control & Security

Paper No.	[40]	[43]	[44]	[45]
Phase detector	XOR gate	Bang Bang phase detectorr	TDC	TDC
LOOP filter	PI based	Digital	Digital	Digital
DCO	DCO	DCO with DSM	DCO	DCO with DSM
Modulation	-------	Dual triangular modulation profile	Triangular modulation	Triangular modulation
Power consumption	-----	15.8 mW	19.8 mW	23.4 mW
Output frequency	-----	6 GHz	1.5 GHz	1.5 GHz
function of ADPLL	phase detection of power grid voltage	Spread spectrum clock Generation	Despreads the Clock	Achieving spread spectrum clock
Advantages	wide track-in range and fast pull-in time,	balance between electromagnetic interference reduction and broadband jitter generation	Operating without a crystal oscillator and external passive filters.	EMI reduction self calibration
Application	Power grid connection	Security	Security	Security

Table 4. Medical Applications

PAPER	[11]	[12]	[8]	[13]
Phase detector	Time to Digital Converter	TDc based phase accumulator	Charge pump	Charge pump
Loop filter	Digital	PI based	Second order filter	Digital loop filter
DCO	LC based DCO	On chip Oscillator	LC based VCO	LC based DCO
Modulation	GPSK// QPSK	Two point	OOK/FSK	FSK
Output frequency	1.89 GHz	--	2.4 GHz	862-870 MHZ
function of ADPLL	Frequency modulation	Modulated the sensor information to RF level	Modulation	Modulation
Advantages	Power grid connection	Security, SOC	Security	Security
Application	Medical applications	Medical application , Natural disaster application	Wireless medical applications	Wireless body sensor networks

Table 5. Communication Applications

PAPER	[23]	[25]	[26]	[24]
Phase detector	Bang bang phase detector	TDC	TDC based DSM	Charge pump
Loop filter	Digital	Digital	Digital	Digital
DCO	four stage ring oscillator	Interpolation type DCO	DCO dithering scheme	DCO dithering
Modulation	ASK/FSK	---	---	Frequency Modulation
Output frequency	6.25 GHz	527 MHz	24 MHz	7 GHz
function of ADPLL	Clock and data recovery	design for liquid crystal display (LCD) analog video RGB)signals acquisition interface applications	Frequency synthesizer	Wideband frequency modulation
Advantages	Low power ,area, Larger Bandwidth	Small chip area, low power, fast phase tracking scheme	Large frequency multiplication ratio, low jitter performance	Good auto calibration, FMCW
Application	PON	Video pixel clock generation	-	Radar

4.   WORK AND RESULT ANALYSIS

ADPLL papers are reviewed in various categories. The performance of ADPLL depends on various factors such as wide frequency range, frequency resolution, low power consumption, low area utilization, etc. The area utilization also depends on placement and routing. So we have implemented a 0.009mm2 Wide-Tuning Range Automatically Placed-and-Routed ADPLL in 14nm Fin FET CMOS" which involves more performance factors, proposed by David.M.Moore et al.. ADPLL designed with Time to Digital Convertor (TDC) and phase interpolator technique, digital loop filter and ring oscillator. Ring Oscillator can be designed with odd number of Inverters, output of the last inverter is fed back into the first. The technical result is based on performance evaluation obtained through simulation

Dual loop PLL architecture is utilized in this design in order to avoid the timing problems associated with the conventional system. Phase detection is achieved using an embedded TDC . In an embedded TDC,

flip flops sample the internal phase signals of a ring oscillator, and the output value is decoded to indicate the location of the propagating edge inside the oscillator. This in turn directly corresponds to the phase of the oscillator. The important advantages of this ADPLL are 1.Time to Digital Convertor (TDC) and phase interpolator Combination gives wide tuning range, frequency resolution 2. Ring oscillator reduces the power consumption of ADPLL.3. Automatic Place and Routing reduces the area utilization.

The ADPLL output frequency tunes from 1.0 GHz to 5.5GHz across process corners. TDC nonlinearity was measured using the on-chip measurement system. The entire analysis is conducted in a windows 7 operating system. Micro wind is a tool for designing and simulating circuits at layout level. Figure 1 represents Layout of the design and Figure 2 represents output frequency waveform.
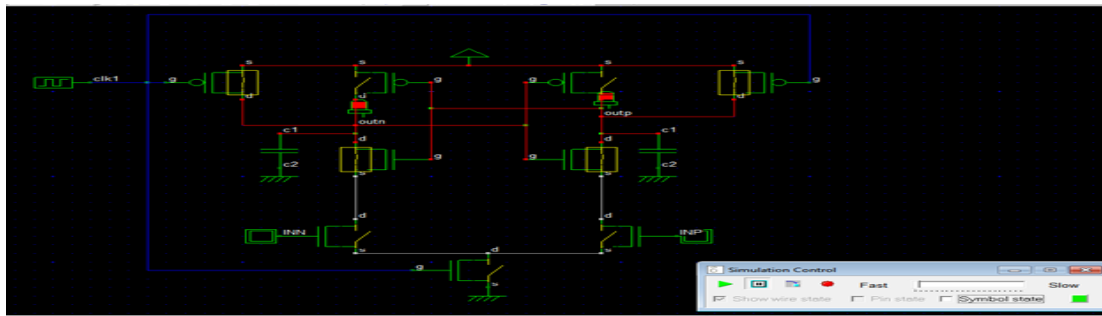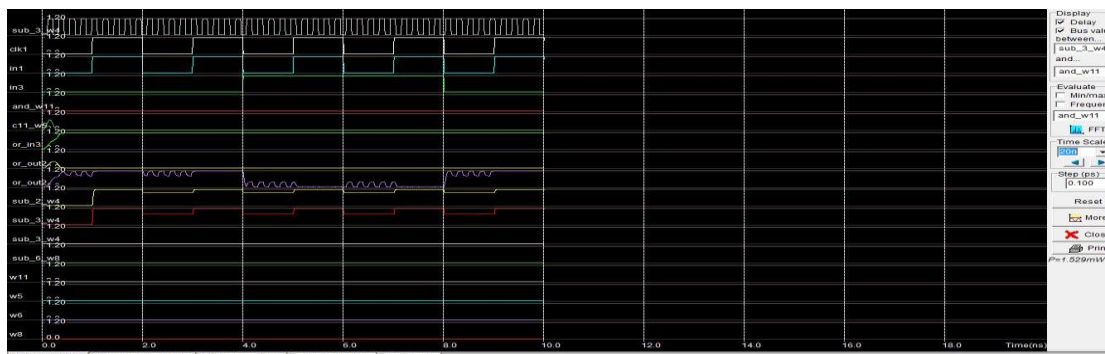

Figure 1. Proposed system design

Figure 2. Output frequency waveform

5.   RESEARCH CHALLENGES

The efficiency of ADPLL depends upon important parameters such as locking range, phase noise, loop stability, power consumption etc. The selection of phase detector and controlled oscillator depends upon the requirement of the above parameters. Bang bang detector will utilize low power and supports the locking range in a short time (below four micro seconds) compared to the various detectors like charge pump, sequential based detectors etc.

Digital controlled oscillator is a power eating component. Mostly, LC based oscillator and ring oscillators are used in ADPLL applications. LC oscillators reduce phase noise and provide good loop stability, but it consumes more power. Ring oscillators give high jitter and phase noise but it enters locked state with low power consumption. Digital filtering reduces ripples in an enhanced way compared to the analog filters. Clock gating is a technique used to reduce power consumption.

6.   CONCLUSION

The paper surveys the importance of ADPLL in different applications like bio-medical, wireless sensor networks and internet of things, radar satellite communications, power applications and in various measurement techniques. The combination of components used in ADPLL depends on various factors like locking range, locking time, power consumption, frequency resolution, phase noise, applications etc. The bang bang phase detector compared to charge pump and Time to digital converter gives the status of

reference signal and oscillator signal with representation, low power consumption with small chip area. The selection of oscillators depends on various factors like loop stability, phase noise, jitter, power utilization, etc. Digital loop filtering is used in all applications because of its precise filtering and less gate count utilization.

ADPLL utilizes interpolation techniques to improve the frequency resolution. The different modulation techniques used along with ADPLL are GPSK, QPSK, FSK, OOK, etc. ADPLL designed with feed forward compensation, fast searching algorithm, sub sampling algorithm gives fast lacking and good frequency resolution. ADPLL can generate a signal with a maximum frequency range of GHZ. ADPLL utilize to do synchronization, modulation, frequency synthesizing, clock recovery, local oscillator signal generation for RF applications, etc. Due to the important constraints in parameters like locking range, wide tuning range, power consumption and multi clock generation, frequency resolution, less gate count utilization, etc, currently ADPLL is used in wired and wireless applications.

ADPLL designed with automatic placement and routing technique is implemented, simulated and synthesized results are analyzed. TDC and phase interpolator are used to obtain wide tuning range and good frequency resolution. The design gives an output frequency range from1.0-5.5GHz with low power consumption. The phase noise is -101 dBc/Hz @ 10MHz off set. The ADPLL can be used for clock generation applications and wireless communications based applications due to the features such as low area-utilization, low power consumption, wide tuning range and frequency resolution and multi-GHz clocking.

REFERENCES

[1]   Volodymyr Kratyuk ,Pavan Kumar Hanumolu, Un-Ku Moon and Kartikeya Mayaram," A Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-Loop Analogy" *IEEE transactions on circuits and systems,*vol. 54, no. 3, march 2007.

[2]   Xin Chen ,Jun Yang ,Member, IEEE, and Long-Xing Shi, Member, IEEE, "A Fast Locking All-Digital Phase-Locked Loop via Feed-Forward Compensation Technique", *IEEE transactions on very large scale integration (vlsi) systems,* vol. 19, no. 5, may 2011.

[3]   Made Murwantara ,Hendra Tjahyadi ,Pujianto Yugopuspito , Arnold Aribowo, Irene A. Lazarusli," Towards Adaptive Sensor-cloud for Internet of Things", *TELKOMNIKA (Telecommunication, Computing, Electronics and Control)*, vol.16, no.6, December 2018, pp.2771-2781.

[4]   Yousra Abdul Alsahib S.aldeen ,Kashif Naseer Qureshi, "New Trends in Internet of Things, Applications, Challenges, and Solutions", *TELKOMNIKA (Telecommunication, Computing, Electronics and Control)*, vol.16, no.3, june 2018, pp. 1114-1119.

[5]   Anil Khatak1 , Manoj Kumar , Sanjeev Dhull, "Analysis of CMOS Comparator in 90nm Technology with Different Power Reduction Techniques", *International Journal of Electrical and Computer Engineering* (*IJECE*) vol. 8, no. 6, december 2018, pp. 4922-4931.

[6]   Tino Copani, Seungkee Min, Sridhar Shashidharan, Sudipto Chakraborty, Mark Stevens, Sayfe Kiaei, and Bertan Bakkaloglu, "A CMOS Low-Power Transceiver With Reconfigurable Antenna Interface for Medical Implant Applications", *IEEE transactions on microwave theory and techniques,* vol. 59, no. 5, may 2011.

[7]   Waleed Khalil, Sridhar sasidharan, Tino Copani, Sudipto Chakraborty, Sayfe Kineri, "A 700 Ua 405 MHz All Digital Fractional-N frequency Locked Loop for ISM band applications", *IEEE transactions on microwave theory and techniques,* Vol 19, May 2011.

[8]   Qi Zhangf, Peng feng, Zhiqing Geng, Xiaozhou Yan, "A 2.4 GHz energy efficient transmitter for wireless medical applications". *IEEE transactions on biomedical circuits and systems,* Vol 5, No 1, February 2011.

[9]   Hae-Moon Seo, YeonKug Moon, Yong-Kuk Park, Dongsu Kim, Dong-Sun Kim, Youn-Sung Lee, Kwang-Ho Won, Seong-Dong Kim, and Pyung Choi," A Low Power Fully CMOS Integrated RF Transceiver IC for Wireless Sensor Networks', *IEEE transactions on very large scale integration (VLSI) systems,* Vol. 15, no. 2, February 2007.

[10] Simon Cimin Li, Hong-Sing Kao, Chia-Pei Chen, and Chung-Chih Su," Low-Power Fully Integrated and Tunable CMOS RF Wireless Receiver for ISM Band Consumer Applications", *IEEE transactions on circuits and systems,* Vol. 52, no. 9, September 2005.

[11] Shoichi Masui S, Kouichi Kanda and Kazuaki otshi, " An ultra low power WirelessTransceiver SOC for Medical applications", *2015 IEEE International symposium on Radio Frequency Integeration Technology.*

[12] Xue-jiao Zhang,Ke-JiCui,Znuo Zuo, Li-Rong Zheng, "*A wireless portable SOS device based on All Digital Phase Locked Loop*", 2015 International conference on consumer electronics.

[13] Alan Chi Wai Wang, ganesh Kathiresan, Chung Kei Thomas chan, Omar EEljamqly, Okundu Omeny, Declan Mc Donagh, Alison .J.burdet and Christofer Toumazou, "A 1 V Wireless Transceivet for an ultra low power SOC for biotelemetry applications", *IEEE journal of solid state circuits,* Vol 43, No7, July 2008.

[14] Baoyong Chi, Jinke Yao Shuguang Han, Xiang Xie, Guolin Li And Zhihua Wangt, "Low power Transceiver Analog front end circuits for Bidirectional high data rate wireless telemetry in medical endoscopy applications", *IEEE Transaction on Bio medical Engineering,* Vol 54, No 7, July2007.

[15] M.R.NezhadAhmadi, G.Weale,A.EI-Agha, D.Griesdort, G.Tumbush,A.Hollinger,M.Matthey, H.Meiners, S.Asgarian. "A 2mW 400MHz RF transceiver SoC in 0.18 Um CMOS Technology in Wireless medical applications", *IEEE radio frequency integrated symposium.*

[16] Robert Bogdan Staszewski and Poras T. Balsara," Phase-Domain All-Digital Phase-Locked Loop", *IEEE transactions on circuits and systems,* Vol. 52, no. 3, March 2005.

[17] Denis. C. daly and Anantha.P. chandrasekaran, "An energy efficient OOK transceiver for wireless sensor networks", *IEEE journal of Solid state circuits,* Vol 42, No3, May 2007.

[18] Philipp Greiner, Graduate Student Member, IEEE, Jasmin Grosinger, Member, IEEE, Johannes Schweighofer, Christoph Steffan, Graduate Student Member, IEEE, Sandra Wilfling, Gerald Holweg, and Wolfgang Bösch, Fellow, IEEE," A System-on-Chip Crystal-Less Wireless Sub-GHz Transmitter", *IEEE Transactions on Microwave Theory and Techniques,* Vol. 66, no. 3, March 2018.

[19] David Ruffieux, jeremie Chabloz, matteo contaldo, Claude Muller Franz Xavier Pengg, PaolaTortori, Alexandre Vouilloz, Patrick Volet and Christian Ena."A Narrowband Multi-Channel 2.4 GHz MEMS-Based Transceiver", *IEEE journal of solid state circuits,* Vol 44, NO 1, January 2009.

[20] Eugene koskin, Dmitri galayko and Elena blokhina, "Concept of Synchronous ADPLL Networks in Application to Small-Scale Antenna Arrays", *IEEE Access Vol 2018.*

[21] David.M.Moore , Thucydides Xanthopoulos, Scott Meninger, and David D. Wentzloff, "A 0.009 mm2 Wide-Tuning Range Automatically Placed-and-Routed ADPLL in 14-nm FinFET CMOS", *IEEE Solid-State Circuits Letters*, Vol. 1, No. 3, March 2018.

[22] Marijn Verbeke, Pieter Rombouts, Hannes Ramon, Jochem Verbist, Johan Bauwelinck, Member, IEEE, Xin Yin, Member, IEEE, and Guy Torfs, Member, IEEE, "A 25 Gb/s All-Digital Clock and Data Recovery Circuit for Burst-Mode Applications in PONs", *Journal of lightwave technology,* Vol. 36, no. 8, april 15, 2018.

[23] WanghuaWu, Robert Bogdan staszewski and john. R. lohn. R. long, "A 56.4 to 63.4 GHz multi rate All digital fractional-N PLL for FMCW radar applications in 65 nm CMOS", *IEEE journal of solid state circuits,* Vol 49,No 5, May 2014.

[24] Ching-Che Chung, Member, IEEE, and Chiun-Yao Ko," A Fast Phase Tracking ADPLL for Video Pixel Clock Generation in 65 nm CMOS Technology", *IEEE Journal of Solid-State Circuits,* Vol. 46, No. 10, October 2011.

[25] Ching-Che Chung, Member, IEEE, Duo Sheng, Chia-Lin Chang, Wei-Da Ho, Yang-Di Lin, and Fang-Nien Lu," An All-Digital Large-N Audio Frequency Synthesizer for HDMI Applications'', *IEEE Transactions on Circuits and Systems-II: Express Briefs,* Vol. 59, No. 7, July 2012.

[26] Robert Neal Dean, Senior Member, IEEE, and Aditi Kiran Rane," A Digital Frequency-Locked Loop System for Capacitance Measurement", *IEEE Transactions on Instrumentation and Measurement,* Vol. 62, No. 4, April 2013.

[27] Dennis M Fischette, Alvin. L.s. Loke, Richard j. Desantis, and Gerry R.Talbot, "An Embedded All digital circuit to measure Pll response", *IEEE Journal of Solid State Circuits,* Vol 45,NO 8, August 2010.

[28] Jim Dunning,Gerald garcia, Jim Lundberg, and ED Nuckollis, "An All-Digital Phase-Locked Loop with 50-Cycle Lock Time Suitable for I High-Performance Microprocessors", *IEEE journal of solid state circuits,* Vol 45, no 8, August 2010.

[29] Po-Hui Yang, Member, IEEE, and Jinn-Shyan Wang, Member, IEEE, "Low-Voltage Pulsewidth Control Loops for SOC Applications'', *IEEE Journal of Solid-State Circuits,* Vol. 37, No. 10, October 2002.

[30] Seunghyeon Kim, Jihoon Sohn, and Hyunchol Shin," A CMOS UHF Harmonic Rejection Transceiver with Two-Dimensional LO Phase Calibration for TV White Space Applications", *IEEE Transactions on Circuits and Systems II: Express Briefs* Volume: 64, Issue: 11, Nov. 2017.

[31] Ming Ding, Member, IEEE, Zhihao Zhou, Yao-Hong Liu, Senior Member, IEEE,, Stefano Traferro, Christian Bachmann, Kathleen Philips, and Fabio Sebastiano, "A 0.7-V 0.43-pJ/cycle Wakeup Timer based on a Bang-bang Digital-Intensive Frequency-Locked-Loop for IoT Applications", *IEEE Solid-State Circuits Letters* Volume: 1, Issue: 2, Feb. 2018.

[32] Yao-Hong Liu, Member, IEEE, Johan van den Heuvel, Takashi Kuramochi, Benjamin Busze, Paul Mateman, Vamshi Krishna Chillara, Bindi Wang, Robert Bogdan Staszewski, Fellow, IEEE, and Kathleen Philips, Member, IEEE," An Ultra-Low Power 1.7-2.7 GHz Fractional-N Sub-Sampling Digital Frequency Synthesizer and Modulator for IoT Applications in 40 nm CMOS'', *IEEE Transactions on Circuits and Systems.*

[33] David E. Bellasi, Student Member, IEEE, and Luca Benini, Fellow, IEEE, "Smart Energy-Efficient Clock Synthesizer for Duty-Cycled Sensor SoCs in 65 nm/28 nm CMOS'', *IEEE Transactions on Circuits and Systems I: Regular Papers*, Volume: 64, Issue: 9, Sept. 2017.

[34] Feng-wei Kuo, Sandro Binsfield Ferreira, H-Neng Ron chen, Lan Chou cho, Chewn-pu jou, FU-Lung Hsueh, Iman Madadi, Mina Shahmohammadi, Masoud Babaie and Robert Bogdon Staszewski, "A Bluetooth Low energy transceiver with 3.7 mW ALL digital transmitter 2.75 mW high IF Discrete time receiver and TX/RX switchable on chip matching network", *IEEE Journal of Solid State Circuits,* Vol 52, No 4, April 2017.

[35] Masoud Babaie, Feng-Wei Kuo, Huan-Neng Ron Chen, Lan-Chou Cho, Chewn-Pu Jou, Fu-Lung Hsueh, Mina Shahmohammadi, and Robert Bogdan Staszewski, "A Fully Integrated Bluetooth Low-Energy Transmitter in 28 nm CMOS With 36% System Efficiency at 3 dBm", *IEEE Journal of Solid-State Circuits*, Volume: 51, Issue: 7, July 2016.

[36] Akihide Sai, Hidenori Okuni, Tuan Thanh Ta, Member, IEEE, Satoshi Kondo, Member, IEEE, Takashi Tokairin, Masanori Furuta, and Tetsuro Itakura," A 5.5 mW ADPLL-Based Receiver With a Hybrid Loop Interference Rejection for BLE Application in 65 nm CMOS", *IEEE Journal of Solid-State Circuits* Volume: 51, Issue: 12, Dec. 2016.

[37] SeongJin Oh, SungJin Kim, Imran Ali, Truong Thi Kim Nga, DongSoo Lee , YoungGun Pu, Sang-Sun Yoo, Minjae Lee, Keum Cheol Hwang, Youngoo Yang , and Kang-Yoon Lee, "A 3.9 mW Bluetooth Low-Energy Transmitter Using All-Digital PLL-Based Direct FSK Modulation in 55 nm CMOS", *IEEE Transactions on Circuits and Systems,* Volume: 65, Issue: 9, Sept. 2018.

[38] Naser Pourmousavian, Feng-Wei Kuo, Teerachot Siriburanon, Masoud Babaie and Robert Bogdan Staszewski, "A 0.5-V 1.6-mW 2.4-GHz Fractional-N All-Digital PLL for Bluetooth LE With PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28-nm CMOS'', *IEEE Journal of Solid-State Circuits* Volume: 53, Issue: 9, Sept. 2018.

[39] Hua Geng, Jianbo Sun, Shuai Xiao and Geng Yang" Modeling and Implementation of an All Digital Phase-Locked-Loop for Grid-Voltage Phase Detection", *IEEE Transactions on Industrial Informatics,* Vol. 9, No. 2, May 2013.

[40] Hua Geng, Dewei Xu and Bin Wu, "A Novel Hardware-Based All-Digital Phase-Locked Loop Applied to Grid-Connected Power Converters", *IEEE Transaction on Industrial Electronics,* Vol 58, No 5, May 2011.

[41] Ching-Che Chung, Duo Sheng, and Wei-Da Ho," A Low-Cost Low-Power All-Digital Spread-Spectrum Clock Generator'', *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* Volume: 23, Issue: 5, May 2015.

[42] Jaehyeok Yang, Joon-Yeong Lee, Sun-Jae Lim, and Hyeon-Min Bae, Member, IEEE," Phase-Rotator-Based All-Digital Phase-Locked Loop for a Spread-Spectrum Clock Generator", *IEEE transactions on circuits and systems,* Vol. 61, no. 11, November 2014.

[43] I-Ting Lee, Shih-Han Ku, and Shen-Iuan Liu, Fellow, IEEE," An All-Digital Despreading Clock Generator", I-Ting Lee, Shih-Han Ku, and Shen-Iuan Liu, Fellow, *IEEE.*

[44] I-Ting Lee, Shih-Han Ku, and Shen-Iuan Liu, Fellow, IEEE.," An All-Digital Spread-Spectrum Clock Generator With Self-Calibrated Bandwidth", *IEEE transactions on circuits and systems,* vol. 60, no. 11, November 2013.

[45] Duo Sheng, Ching-Che Chung, and Chen-Yi Lee," A Low-Power and Portable Spread Spectrum Clock Generator for SoC Applications", *IEEE transactions on very large scale integration (VLSI) systems,* Vol. 19, no. 6, June 2011.

[46] Robert Bogdan staszewski,Khurram Waheed, Fikret Dulger and oren E. Eliezer," Spur-Free Multirate All-Digital PLL for Mobile Phones in 65 nm CMOS", *IEEE Journal of Solid State Circuits,* Vol 46,No12, December 2011.

[47] Robert Bogdan staszewski , John wallberg, chih-ming hung, Gennady Feygin,Mitch Entezari and drink Leipoid, "LMS-Based Calibration of an RF Digitally Controlled Oscillator for Mobile Phones", *IEEE transactions on circuits and systems,* Vol 53, No 3, March 2006.

[48] Feng wei Kuo, Masoud Babaie, huan-Neng Ron chen, lan-chou cho, Chewn-pu jou, Mark chen and Robert Bogdan staszewski, "An All-Digital PLL for Cellular Mobile Phones in 28-nm CMOS with-55 dBc Fractional and-91 dBc Reference Spurs", *IEEE transactions on circuits and systems.*

[49] Robert Bogdan Staszewski, John L. Wallberg, Sameh Rezeq, Chih-Ming Hung, Oren E. Eliezer, Sudheer K. Vemulapalli, Chan Fernando, Ken Maggio, Roman Staszewski, Nathen Barton, Meng-Chang Lee, Patrick Cruise, Mitch Entezari, Khurram Muhammad, and Dirk Leipold ,"All-Digital PLL and Transmitter for Mobile Phone", *IEEE Journal of Solid State Circuits*, Vol 46,No 12, December 2011.

[50] Robert Bogdan Staszewski, Dirk Leipold, and Poras T. Balsara,"Direct Frequency Modulation of an ADPLL for Bluetooth/GSM With Injection Pulling Elimination", *IEEE transactions on circuits and systems,* Vol. 52, no. 6, June 2005.

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