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A Monolithic 0.18μm 4GHz CMOS Frequency Synthesizer

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Abstract

A 4 GHz PLL (phase-locked loop)-type frequency synthesizer has been implemented in the standard 0.18μm mixed-signal and RF 1P6M CMOS technology. It integrates a VCO, a dual-modulus prescaler, PFD, a charge pump, a control logic, various digital counters and digital registers onto a single chip. With the help of the linear model of the loop, the design and optimization of the loop parameters are discussed in detailed. The measured results show that the locked range was 4096-4288 MHz and the phase noise could reach -117 dBc/Hz at 1MHz offset from the carrier 4.154 GHz, the output power is about -3 dBm. The chip area is 0.675 mm×0.700 mm. The DC power consumption of the core part is about 24 mW under 1.8 V supply.

Keywords*: frequency synthesizer; VCO; PFD; CP; phase noise*

1. Introduction

Frequency synthesis is a process generating lots of the same stable and precise discrete frequency by reference signal source with one or more frequency stability and very high accuracy through the frequency domain linear operation. It is widely used in communication, navigation, radar and measuring equipment. Use frequency synthesis technology made a signal source called frequency synthesizer, which is the key modules in the research of analog RF transceiver system. There are three common realization approaches: direct frequency synthesis, phase lock loop type frequency synthesis and digital frequency synthesis. Among them, the phase lock loop type frequency synthesizer is widely used in RF communication system [1, 2].

2. Transceiver architecture and Frequency Plan

The architecture and frequency plan of the RF transceiver play an important role in the complexity and performance of the overall system. The simplified block diagram of a zero-second-IF dual-conversion transceiver is shown in Figure 1. The use of this architecture, the LO_IF is generated from the LO_RF using a divide-by-four counter, eliminates the need for two synthesizers and improves the transmitter's image rejection [3].

The frequency synthesizer generates the quadrature 1 GHz and 4 GHz LO frequencies used for the mixers in the receiver and transmit chains. Figure 2 shows a block diagram of the frequency synthesizer, which is made up of a phase frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), a VCO, and a down scaling circuit. The frequency band at 4 GHz is generated by the VCO, and the quadrature 1 GHz LO signals are obtained by the frequency divider working at divided-by-4 in the down scaling circuit, then K=4. In this PLL system, the down scaling circuit consists of three parts: a synchronous frequency divider working in the divide-by-4 mode, a dual-modulus prescaler (DMP), and a programmable & plus swallow divider made up of counter-M and counter-A. The DMP divides the output by P+1 until counter-A counts up to A. At this point it switches over and divides by P until counter-M counts up to M.

In the proposed frequency synthesizer, K=4, P=8, M=32, and A can be set between 3 and 10 in the programmable & plus swallow divider. Then the two counters are reset, and DMP switches back to divide-by-(P+1) at the same time. The total division ratio of the down scaling circuit is:

$$N = K(PM + A) \quad (1)$$

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The synthesizer phase locks an on-chip VCO to a 4 MHz reference frequency. The synthesized frequency can be varied from 4.144 to 4.256 GHz in a step of 16MHz, which corresponds to an RF carrier center frequency ranging from 5.18 to 5.32 GHz in a step of 20MHz. The operation frequency of the proposed transceiver in t his paper covers the 5.15～5.35GHz band.

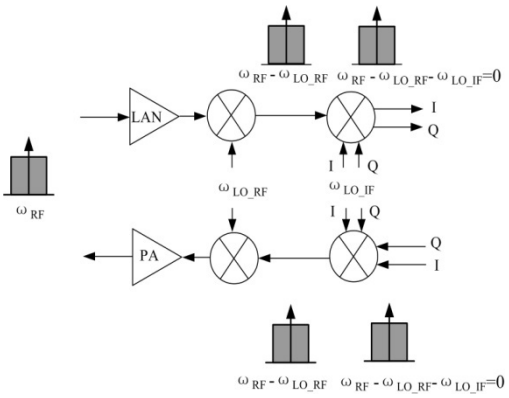

Figure 1. Simplified RF Transceiver Architecture

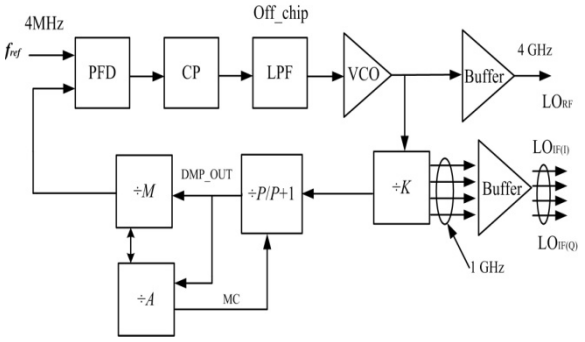

Figure 2. Block Diagram of PLL Frequency Synthesizer

3. Behavioral Simulations

The proposed CPPLL type frequency synthesizer can be modeled as a linear system. Figure 3 gives the linear model of CPPLL type frequency synthesizer. The PFD and CP are combined as one block, IP is the current of the charge pump and K_d is the gain of the block ($I_p/2\pi$). The VCO is an ideal integrator with gain K_V, and the transfer function of the LPF is defined as $F(s)$. In order to reduce the chip area, a passive third-order loop filter for the frequency synthesizer is used and realized by off-chip components.

For the third-order passive loop filter, usually, $C_3<<C_1$, C_2, the transfer function of the filter is simplified:

$$F(s) \approx \frac{1}{C_{\text{total}}} \frac{1+s\tau_2}{s(1+s\tau_1)(1+s\tau_3)} \tag{2}$$

where $C_{\text{total}} = C_1 + C_2 + C_3$, $\tau_1 = R_2 \dfrac{C_1 C_2}{C_1 + C_2}$, $\tau_2 = R_2 C_2$, $\tau_3 = R_3 C_3$.

The PLL open-loop gain $H_0(s)$ is

$$H_o(s) = \frac{K_v I_p}{2\pi N C_{\text{total}}} \frac{1+s\tau_2}{s^2(1+s\tau_1)(1+s\tau_3)} \tag{3}$$

The closed-loop transfer function $H(s)$ is

$$H(s) = \frac{NH_o(s)}{1+H_o(s)} = \frac{\dfrac{K_v I_p}{2\pi C_{\text{total}}}(1+s\tau_2)}{\tau_1\tau_3 s^4 + (\tau_1+\tau_3)s^3 + s^2 + \dfrac{K_v I_p \tau_2}{2\pi N C_{\text{total}}} s + \dfrac{K_v I_p}{2\pi N C_{\text{total}}}} \tag{4}$$

For simplicity, we ignore these high terms which are smaller than lower order terms. So the simplified second-order expression is

$$H(s) \approx \frac{\frac{K_v I_p}{2\pi C_{total}}(1+s\tau_2)}{s^2 + \frac{K_v I_p \tau_2}{2\pi N C_{total}} s + \frac{K_v I_p}{2\pi N C_{total}}} \quad (5)$$

Therefore, the damping factor and natural frequency:

$$\zeta = \frac{\tau_2}{2}\sqrt{\frac{K_v I_p}{2\pi N C_{total}}} \quad (6)$$

$$\omega_n = \sqrt{\frac{K_v I_p}{2\pi N C_{total}}} \quad (7)$$

For most design, the PLL locks in quickly and $0<\zeta<1$, hence it is reasonable to state that the lock-in time is

$$T_L \approx \frac{2\pi}{\omega_n} \quad (8)$$

The design of the LPF plays an important role to the stability of the loop and the performance of the loop trapping and tracking. SuiTable parameters of the components in the LPF not only reduce pull-in and lock-in time, but also improve the stability of the loop. In order to keep the stability of the loop, the phase margin (φ) is usually larger than 45°, the maximum phase margin occurs around the crossover frequency, where the open-loop gain is unity. Then the optimal loop bandwidth (f_n) is equal to the crossover frequency for maximum phase margin. With the help of the linear model, the simulation of the loop response and the transient response are implemented in the ADS 2005. The optimal loop parameters are listed in Table 1.

Table 1. Loop Parameters of The Frequency Synthesizer

K_v(MHz/V)	I_p(mA)	f_{ref}(MHz)	f_n(kHz)	φ(°)	C_1(pF)	R_2(kΩ)	C_2(pF)	R_3(kΩ)	C_3(pF)
160	1	4	50	52	87	4.2	1450	2.8	38

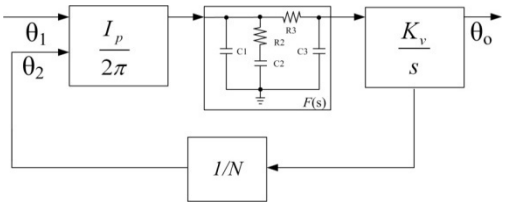

Figure 3. Linear Model for The CPLL Type Frequency Synthesizer

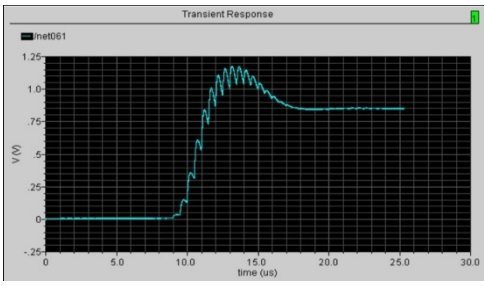

Figure 4. Transient Response of VCO Control Voltage

Based on these Loop parameters and (6), (7), the value of damping factor and natural frequency are 0.95 and 50 KHz, respectively. Based on (8), the lock-in time of the system is about 20 us. Figure 4 shows the transient response of the VCO control voltage in closed loop state when the total division ratio of the down scaling circuit is set to 1036. It can be seen that the control voltage of VCO changed very small after 20 μs, the PLL should be in the locked-state. The overall behavior of the simulation shows good agreement with the design principle and theoretical analysis.

4. Circuit design of Frequency Synthesizer

4.1. The design of VCO

Figure 5 shows schematic views of the VCO. This circuit presented in this paper is based on the negative transconductance LC oscillator [5, 6]. The proposed VCO consists of a LC-tank circuit and a negative-conductance cross-coupled differential pair. The differential transistor pairs generate the negative resistances to compensate the losses of the LC-tank. LC-tank circuit consists of the on-chip differential inductor, the on chip MIM capacitors and the MOS varactors. The relative sizes of Mn1 and Mp1 were determined by the DC value of LC-tank which was set about half of voltage supply source. It was found that when Mn1 and Mn2 share the same (minimum) length, the size of Mp1 should be three and four times as large as Mn1 for optimal phase-noise performance [7]. PMOS varactors are used in inversion mode because of the wide capacitor variation that can be obtained with a low variation of source to gate bias voltage.

4.2. The design of the down-scaled divider

The first divide-by-4 circuit is the most critical and challenging compare to other building blocks in the frequency synthesizer. First, the divider operates at the highest frequency and it must still functions properly under the process and temperature variation. Furthermore, it must generate quadrature outputs. At last, in our proposed architecture, the output load of the divide-by-4 circuit contains not only the next stage divider and wiring capacitance but also two buffers for up and down mixers. This means the load capacitance will be very large, nearly 200fF in our design.

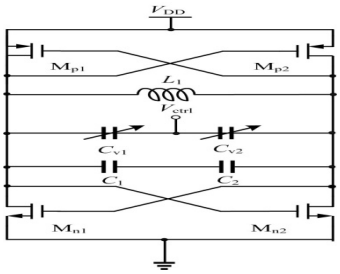

Figure 5. Circuit Schematic of The VCO

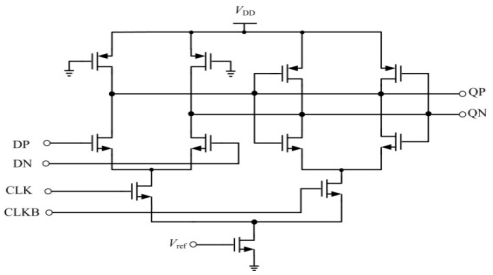

Figure 6. Circuit Schematic of The Latch Voltage

The divide-by-4 circuit consists of two divide-by-2 cascade including two D flip-flops (DFF). An improved D-latch is used to realize the master/slave DFF as shown in Figure 6. It is the source-coupled logic (SCL) with tail current source. Complementary cross-coupled pairs are used in the output part of the latch. The load of the output part is lightened to improve the operating speed. The operating speed of the latch is proportion to the charge/discharge current, and in inverse proportion to signal swing amplitude. We can increase the reference voltage Vref and tail current to improve the operating speed [8].

As shown in Figure 2, the dual-modulus (P/P+1) prescaler is combined with two programmable counters M and A, which are implemented with standard digital cells to realized a programmable divide ratio of PM+A. The implemented circuit of the DMP is shown in Figure 7, which consists of a divider-by-4/5 synchronous counter, a divider-by-2 asynchronous counter and division model control (MC) circuit. When division model control input is high, the prescaler divide ratio is 9, otherwise, the divide ratio is 8. The divider-by-4/5 synchronous counter employs three master-slave SCF D-flip-flops and two OR gates. As shown in Figure 8, a novel D-latch architecture integrated with OR logic gates is presented in this paper, DN and DP are the inputs of the OR gate, Vref is the DC reference voltage produced by the internal bias circuit. The D-latch architecture integrated with OR logic gates not only simplified the design steps, but also reduced the parasitical parameters of the single logic gate to assure the high operating speed of the DMP.

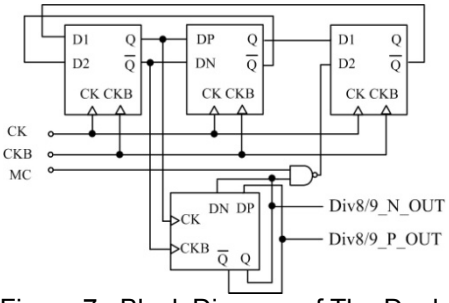

Figure 7. Block Diagram of The Dual-Modulus Divider-by-8/9 Prescaler

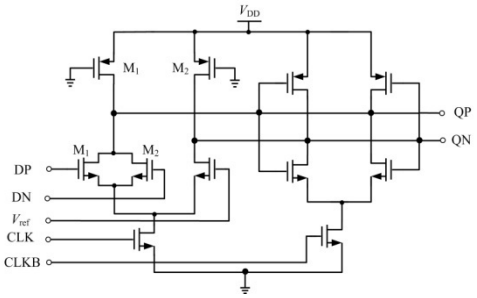

Figure 8. D-latch Architecture With OR Input

4.3. The design of the PFD and CP

Figure 9 shows the schematic of the phase/frequency detector. The PFD generates differential signals by inverter and transfer gate to drive the CP [9]. This sequential PFD has a monotonic phase error transfer (independent of the duty-cycle). The dead-zone of the PFD can be reduced by inserting inverters into the reset path to increase the reset delay.

The task of the charge pump is to hold proper voltage level to control the oscillator [10]. The charge pump, in general, shows nonideal characteristics when implemented in a circuit and its practical issues need to be considered in the design of the PLLs. One of the issues in the charge pump design is the current mismatch. In this paper the effects of the phase offset caused by the current mismatch are considered and a new charge pump circuit with nearly perfect current matching is proposed. Figure 10 is the circuit diagram of the differential charge pump based on the current steering techniques which consists of feed back circuit and band-gap voltage reference circuit. Differential charge pumps provide good rejection to common mode noise or interference [11]. The feed back circuit increases the output dynamic-range and charge/discharge symmetry. Band-gap voltage reference circuit improves the performance of the charge pump [12].

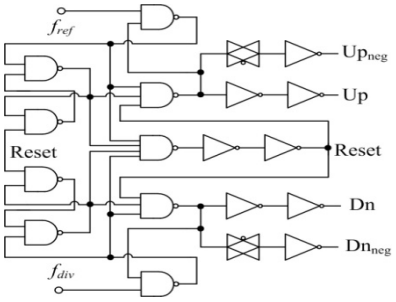

Figure 9. Block diagram of The Dual-Modulus Divider-by-8/9 Prescale

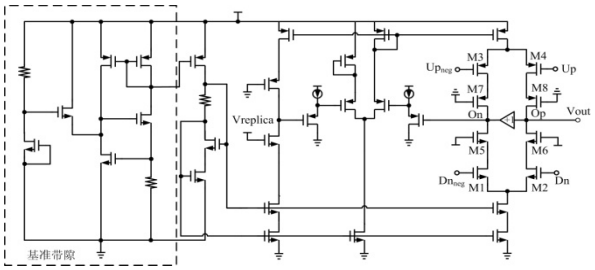

Figure10. Circuit Schematic of Charge Pump

5. Measurement Results

For demonstration, the presented CPLL type frequency synthesizer has been fabricated in SMIC's 0.18μm CMOS process. According to the ISF theory [13], the phase noise can be significantly reduced if certain symmetry properties exist in the waveform of the oscillation. Thus, the layout of the VCO design must be focused on the full symmetry. The PFD and down scaling divider belong to dynamic logic circuit and are sensitive to the parasitic capacitance of the node. Interconnections of those building blocks and connections between the FETs must be shorten as possibly to reduce the parasitic capacitance. Building blocks of the PFD and down scaling divider are encircled by double guard-rings to minimize substrate noise interference. Furthermore they are designed in the deep n-well to This paper also puts forward some methods, including designing PFD and down scaling divider circuit in the deep n-well separating the analog and digital supply, choosing appropriate filter capacitor and separating the analog

and digital ground to reduce the interference between the analog circuit and digital circuit. The size of the chip including the pads is 0.675 mm×0.7 mm. Figure 11 shows a photo of the experimental die. Figure 12 shows a photograph of the test PCB. The PCB is fixed onto the ingot by some screws, and the chip is connected with bonding wires to the microstrips at the centre of the PCB.

Figure 11. Microphotograph of The Frequency Synthesizer

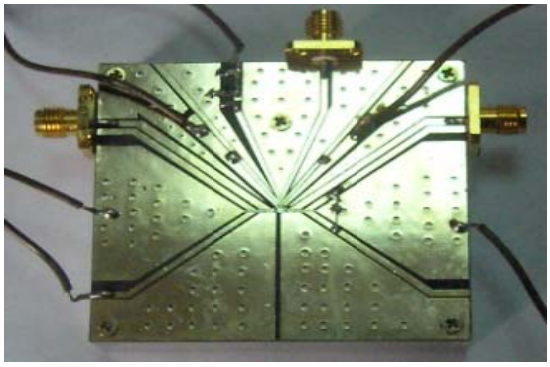

Figure 12. Photograph of The Test PCB

The chip is measured by the Advantest D3186 signal generator, Agilent E4440A spectrum analyzer and Agilent 86100A oscilloscope. Figure 13 shows a plot of the measured phase noise versus offset frequency at 4.154GHz oscillation tested alone. The phase noise at 1 MHz offset is -123.3 dBc/Hz under an independent 1.8V supply. Figure 14 shows the output waveform of the down scaling circuit in closed loop state when the total division ratio of the down scaling circuit is set to 1036. It can be seen that the frequency of the waveform is equal to 4MHz which is the frequency of the reference signal. This has proved the frequency synthesizer is in the locked-state. Figure 15 shows a plot of the measured phase noise versus offset frequency at 4.154GHz oscillation in the locked state. It can be seen that the phase noise in low frequency is caused by the reference source and VCO. The phase noise at 10kHz offset is about -88dBc/Hz. The phase noise of the frequency synthesizer is mainly caused by the VCO noise up-conversion with -30dB/decade decreasing slope, when the offset is large than the loop bandwidth (about 50kHz), but less than several MHz. The phase noise at 1MHz offset is -117.3 dBc/Hz. When the offset is large than several MHz (about 3 MHz), the phase noise of the frequency synthesizer is mainly caused by the VCO noise with -20dB/decade decreasing slope. The measured power consumption of the core circuits is about 24mW under 1.8V supply.

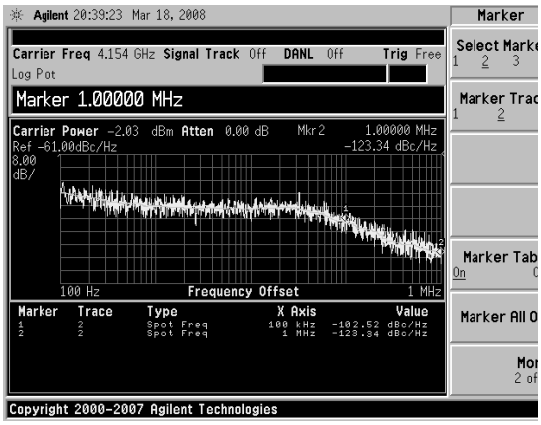

Figure 13. Measured Phase Noise of VCO

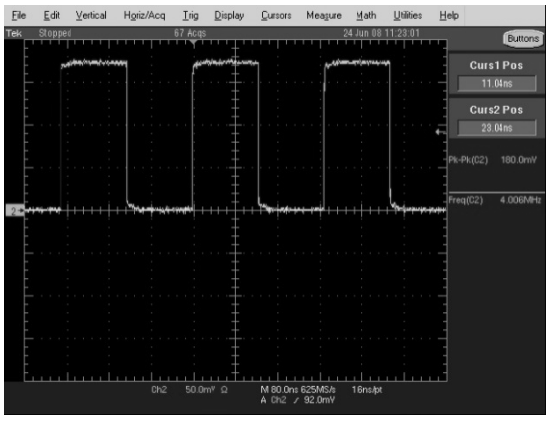

Figure 14. Waveform of Down-Scaler in The Locked State

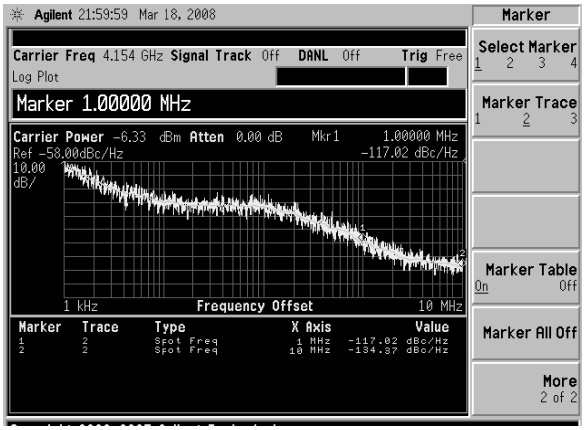

Figure 15. Measured Phase Noise of Frequency Synthesizer in The Locked State

6. Conclusion

In this paper, a 4GHz CPPLL frequency synthesizer has been demonstrated in CMOS SMIC 0.18μm technology with 1.8 V supply voltage. Based on the transceiver architecture, the frequency plan of the RF transceiver is planned. Measurement results verified the validity of the design in this paper.

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