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Development of advanced automated test equipment for digital system by using FPGA

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ABSTRACT

One of the fundamental devices in electronics, Integrated Circuit (IC), is usually applied in more complex devices. Before the IC is used, it has to pass some tests to guarantee that its function is in accordance with the specifications. Automated Test Equipment (ATE) is used to test many electronics devices, including ICs. Nowadays, with the rapid advance in electronics technology, the industry will need more advanced ATE to fulfill customers demand. One of the applicative solutions is improvement and integration of a standalone module in commercial ATE owned by the company. ASL 1000 Test System is one of the ATE that is still widely used in industry. ASL 1000 has one limitation in one of its module, Digital Driver and Detector (DDD). The limitation is how much vector pattern that can be saved in the memory. Based on the observation in DDD instrument, a standalone module that has similar specifications as DDD can be designed using Field Programmable Gate Array (FPGA) as its base component. In the standalone module plan, supporting circuits are used, these are interface circuit between FPGA and PC using RS-232 and ASIC as ATE drivers or comparators to connect FPGA and device under test (DUT). The result of the study shows that the designed module can receive and send 8-bit data at 19.200 baud rate. It can write and read 16-bit data from and to SDR SDRAM within 90 ns and 80 ns for one cycle. It can control DAC type AD5308 in standalone operation and DAC type AD5676 in daisy chain operation to generate specific voltage in specific channel. In behavioral simulation, main controller module has already worked in accordance with the desired specifications.

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1. INTRODUCTION

In recent years, electronic device and its interface for human have been developed rapidly [1,2]. Some electronic device applications, such as for health care monitoring system are reported in [3,4]. An electronic device which is integrated with more complex electronic system, must be tested in order to guarantee that it works according to specifications. Various tests must be done to confirm customer expectation [5]. The tests are arranged in semiconductor tests. Instrument used to test the electronic device is Automated Test Equipment (ATE). The ATE works automatically to conduct a series of measurements and testing of electronic devices or components to determine whether the device under test (DUT) works in accordance with the specifications provided or not [6].

A test services company offers wafer bumping, wafer probing, wafer grinding, lead frame and substrate IC packaging, wafer level CSP and RF. Other services are available, such as analog-digital-mixed signals tests, wafer back grinding, assembly packaging, final test and drop shipment. The more rapid

development of IC technology the better testing devices required. This will certainly cause the company to adjust and develop ATE according to the test requirements requested by the customer [7]. One solution was the development and integration of standalone modules on existing commercial ATE for customer testing needs.

One of the most widely used ATE is the ASL 1000 Test System. The ASL 1000 is often used for testing the device from customer because of its high reliability and low power consumption [8]. In one case, the IC that was tested had complex functionality so that a large local memory ATE was needed. The module used to store memory that contains functional test steps as well as generating vector pattern memory to provide input and compare the output of DUT is in the module called Digital Driver and Detector (DDD). The solution offered to handle memory problems is to design a standalone module that can store more than 1MB of memory and has the capability equivalent to DDD instrument to replace DDD instrument in the 1000 ASL. The designed standalone module must be integrated with the ASL 1000 main system as well.

Field Programmable Gate Array (FPGA) is widely used in many applications, such as implementation for simulated kalman filter optimization algorithm [9], bipolar stepper motor controller [10], and interactive digital signal generator [11]. FPGA is also used widely in IC technology development [12,13]. Furthermore, FPGA based digital IC tester was reported in [14,15]. Based on observations on DDD instrument, a stand alone module that has capabilities such as DDD can be designed by using the FPGA component as the main processor of the module. In the stand alone digital module to be designed, other supporting circuits are needed, namely the interface between FPGA and PC using RS-232 interface and the interface between FPGA with device under test (DUT) using ASIC as ATE drivers or comparators to balance the design module capabilities with DDD instrument.

In this paper, design of FPGA-based digital module hardware instead of DDD instrument in ASL 1000 is reported. This paper will discuss the design of FPGA-based digital module hardware with predetermined specifications.

2. RESEARCH METHOD

Research was conducted based on the following specification and designs.

2.1. Specification of FPGA-based Digital Module

Specification of FPGA-based digital module as designed module compared with instrument of DDD on ASL 1000 can be seen in Table 1. FPGA-based digital module are connected to PC and DUT as shown in Figure 1. The PC is used to send data that will be written to memory in FPGA-based digital modules and receive test results carried out by FPGA-based digital module. The designed module is connected to DUT using bidirectional pin. RS-232 is used between the designed module and PC. Inputs originating from the PC are data of vector patterns, time sets and run test commands given via Graphic User Interface (GUI) on the PC. Output of the module sent to the PC is the result of the run test, which will be received by the PC with the specified format.

Table 1.

Specification	DDD	Designed module
Number of channel	8	4
Number of memory pattern	128 KB	32 MB
Range of Vhigh	-5V – 15V	0V – 5V
Range of Vlow	-5V – 5V	-1V – 4V
Range of Vload	-2V – 8V	0V – 5V

The FPGA used in this research is Spartan 6 XC6SLX9. The external clock used is 50 MHz. Internal clock in FPGA will be generated up to 200 MHz. The memory used is SDR SDRAM type H57V2562GTR with a capacity of 32 MB. Pin electronics between FPGA and DUT using ATE Driver or Comparator MAX19005 type. There are 2 input pins to adjust the drive on the channel and 2 output pins to get compare results in each channel (there are 4 channels for 1 IC) and 4 pins for SPI communication.

Voltage reference for MAX19005 has 5 types. Octal DAC 16 bit AD5676 type is used to provide reference voltage on Drive High Voltage (DHV), Drive Low Voltage (DLV), Compare High Voltage (CHV), Compare Low Voltage (CLV). One 8-bit Octal DAC type AD5308 is used to provide a reference voltage for each Load Drive Voltage (LDV). Both AD5676 and AD5308 can be controlled using SPI serial communication.

2.2. Design of FPGA-based Digital Module Board Systems

Block diagram of overall designed module system consists of 6 main blocks., as shown in Figure 2. The main blocks are crystal clock generator, UART interface RS-232 to TTL, SDR SDRAM interface, MAX19005 interface, AD5676 interface and AD5308 interface. Figure 3 shows internal FPGA chip, there are several parts, namely the UART system, clock generator, SDR SDRAM controller, MAX19005 controller, AD5676 controller, AD5308 controller and main controller.

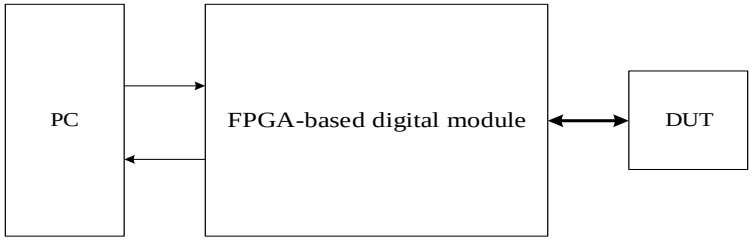

Figure 1. FPGA-based digital module is connected to PC and DUT

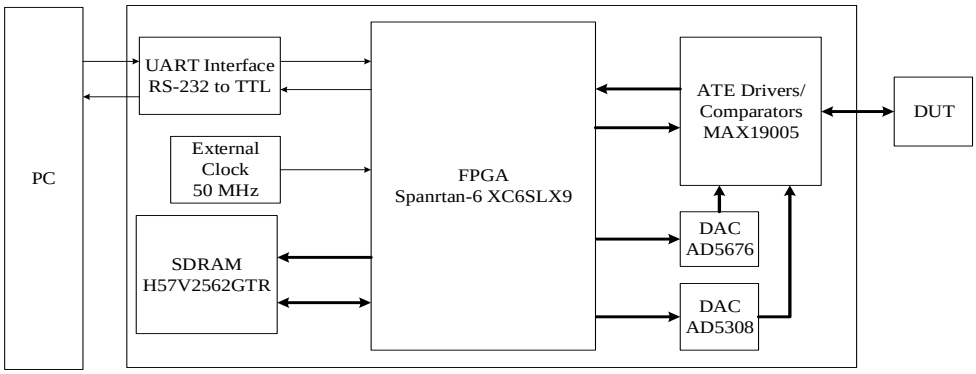

Figure 2. Block diagram of overall system

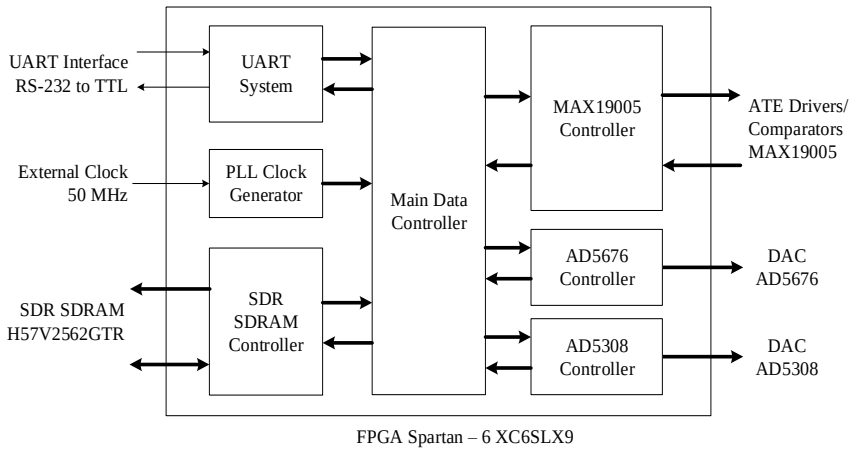

Figure 3. Block diagram of internal parts of FPGA

2.3. Design of UART System Module

UART is used for the communication with baud rate of 19200, 8 bit data without parity bit and 1 stop bit. Block diagram of the UART system is shown in Figure 4. The UART system is used to transmit and receive data serially according to the specified setting. The serial data received will be converted to parallel data and stored in the receiver buffer. The data to be sent is written in the transmitter buffer before sending it.

When the system is not sending data, the data in the transmitter buffer will be sent successively automatically until all data stored in the buffer is sent. The UART system module consists of a FIFO buffer, baud generator, receiver, and transmitter. One FIFO buffer functions for save data from the receiver, and other FIFO buffers to store data going to the transmitter. Baud generator functions to generate pulse signals in accordance with 32 predetermined baud rate values. The receiver functions to receive serial data from pin rs_232_rx and convert to parallel data and the transmitter functions to send parallel data from FIFO buffer in serial form via pin rs_232_tx.

2.4. Design of SDR SDRAM Controller

The SDR SDRAM controller module is designed based on the RD1010 reference design from Lattice Semiconductor. The module serves to simplify the process of reading and writing on SDRAM. This module simplifies the SDRAM read and write commands to be in accordance with the read and write system interface standards as shown in Figure 5. In addition to simplifying the reading and writing process, the SDR SDRAM controller module also provides an auto-refresh function and feedback cycle that is being carried out.

There are two FSM blocks (Finite State Machine), namely Initialization FSM and Command FSM. The Initialization FSM block functions to set the SDR SDRAM settings. The Command FSM block can only work if the initialization has been completed.

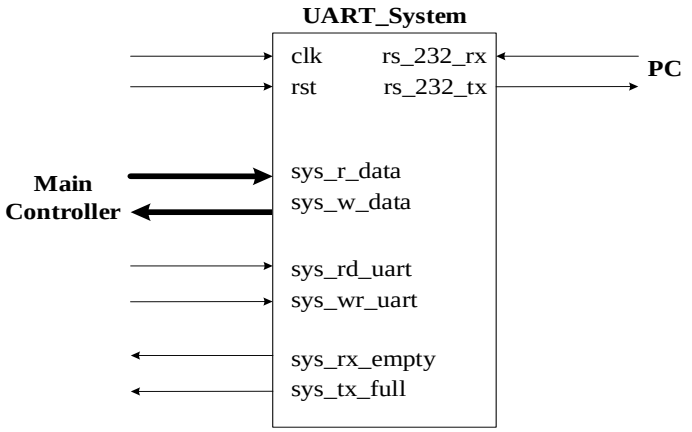

Figure 4. Block diagram of UART

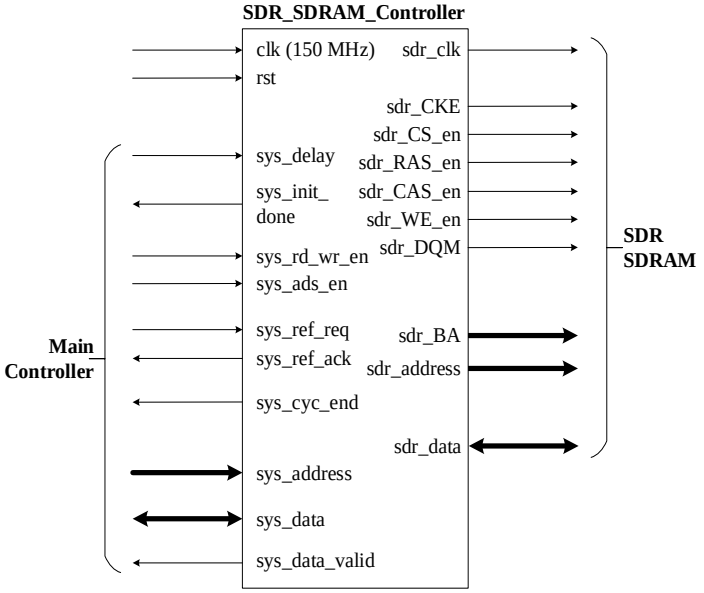

Figure 5. Block diagram of SDR SDRAM controller

2.5. Design of MAX19005 Controller Module

The block diagram of the MAX19005 controller module is shown in Figure 6. The PE controller module connects between the main controller module and one MAX19005 IC. MAX19005 controller functions to set the MAX19005 ASIC. This module commands the settings of each MAX19005 channel in the state initialization. When the test is run, the module will give a signal with high or low logic on the DATA pin and MAX19005_RCV_X according to the given vector pattern. The CMPH and CMPL pins on the IC will provide information on the logic condition of the DUT output signal. The reading of the vector pattern will continue until all the patterns have been read.

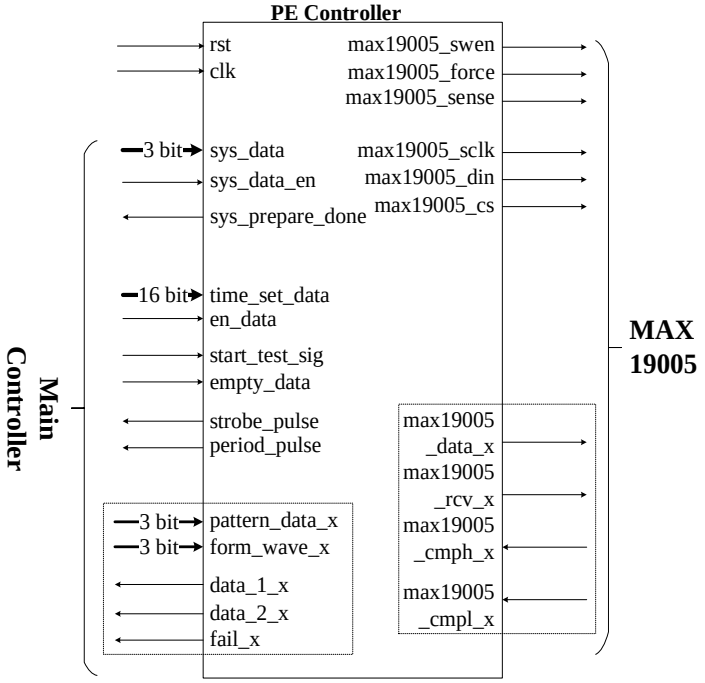

Figure 6. Block diagram of PE controller

2.6. Design of AD5308 Controller Module

AD5308 controller set the initialization of AD5308 IC based on block diagram shown in Figure 7. After the system receives the voltage data from the main controller, the AD5308 controller module will modify the data into 16-bit data according to the IC specifications then send it via serial communication that is regulated by the SPI controller block.

2.7. Design of AD5676 Controller Module

AD5676 controller will set the initialization and setting of the IC AD5676 based on block diagram shown in Figure 8. After the system receives the voltage data from the main controller, the AD5676 controller module will modify the data into 96-bit data according to the specifications and sequence of the IC then send it through serial communication which is regulated by the SPI controller block with the daisy chain method.

2.8. Design of Main Controller

As can be seen in Figure 9, the main controller is the controller of the entire controllers in the FPGA. The pins on the main controller are connected to other controllers, namely the SDRAM controller, AD5308 controller, AD5676 controller and PE controller. In the main controller, there are blocks to set and run each state of the module, such as State Controller, Init FSM, Receive FSM, Prepare FSM and FSM Test. The additional block is the UART Interface which functions to connect the input and output of the UART system to the main controller subblock as needed and SDRAM interface which serves to simplify the process of reading and writing vector patterns when state receive and state test.

3. EXPERIMENT RESULT

In this research, experiment was conducted according to UART system, SDR SDRAM controller, MAX19005 controller, AD5308 controller, AD5676 controller, and main controller.

3.1. Experiment of UART System

The UART system module is tested by 5 times sending data from characters 0 to 255 at baudrate of 19200. The results confirm that success rate of 100% is achieved for the 5 times sending. Figure 10 is experiment result of TX signal from FPGA representing character "U".

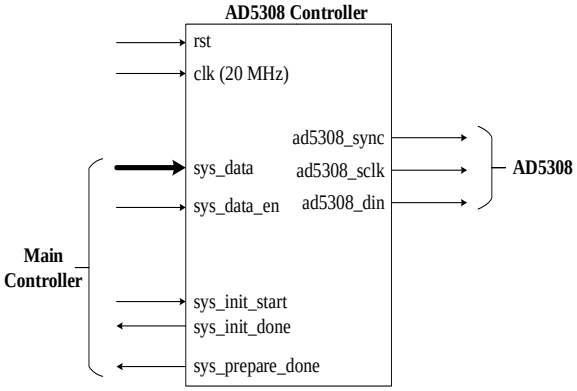

Figure 7. Block diagram of AD5308 controller

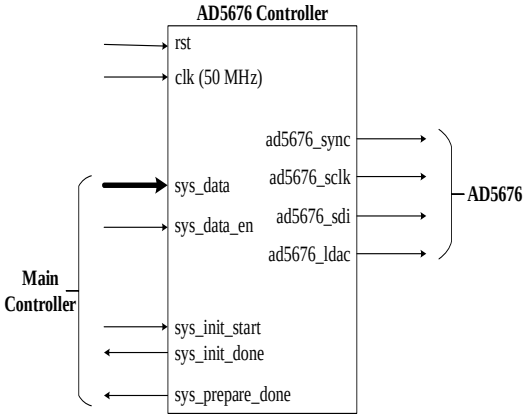

Figure 8. Block diagram of AD5676 controller

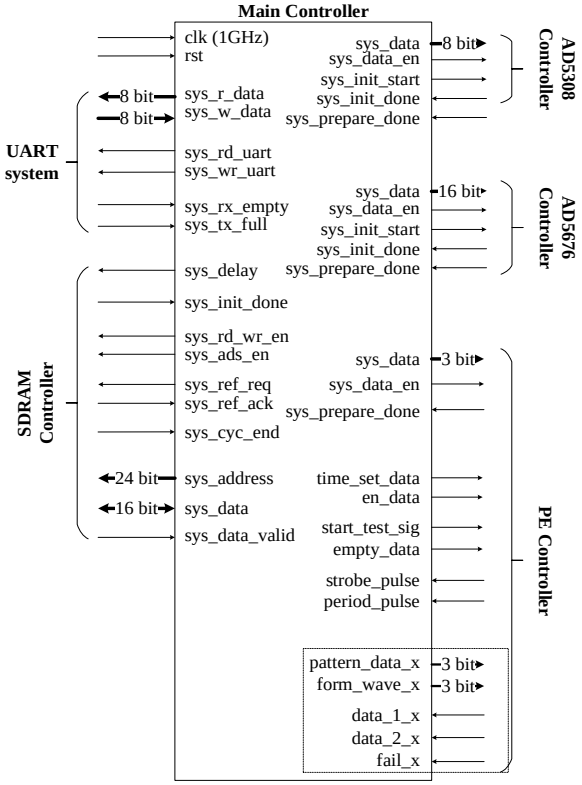

Figure 9. Block diagram of main controller

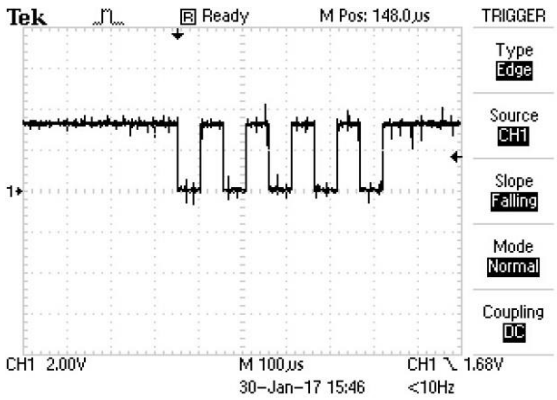

Figure 10. TX signal from FPGA represents character "U"

3.2. Experiment of SDR SDRAM Controller

The SDR SDRAM controller module is tested by sending data from PC through the UART interface and then write it to SDR SDRAM 5 times. The system will read the data after 1 ms and send it back to the PC. Using 100 MHz clock cycle, the experiment result confirms 100% success rate for 5 times tests.

3.3. Experiment of MAX19005 Controller

The MAX19005 controller module is tested using a behavioral simulation because the number of pins observed is too much. The module has succeeded in sending the settings of each channel through SPI communication when instructed. The time needed to send settings for one channel is 4,005 µs. The module can also generate logic values according to the settings and pattern of data provided by the main controller module when the start test command is given.

3.4. Experiment of AD5308 Controller

The AD5308 controller module is tested by giving digital values from 0 to 255 in each channel so that the DAC generates a sawtooth signal. The time needed to send one data packet to AD5308 is 5.120 µs. Figure 11 is the result of the testing of the AD5308 controller module. Figures 12 upper and lower show output signals of the SYNC and DIN pins, respectively.

3.5. Experiment of AD5676 Controller

The AD5676 controller module is tested by giving digital values from 0 to 255 in each channel so that all DACs generate sawtooth signals. Daisy chain operation is used to control 4 DACs, so the time needed to send one data packet to 4 DACs is 30.60 µs. Following are sawtooth waves generated by 2 pieces AD5676 controller module see in Figure 13. Figures 14 uppper and lower are output signals of the SDI and SYNC pins, respectively.

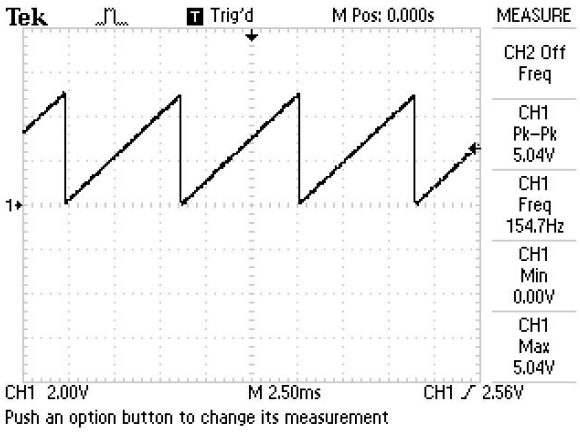

Figure 11. Sawtooth wave generated from channel 1 of AD5308

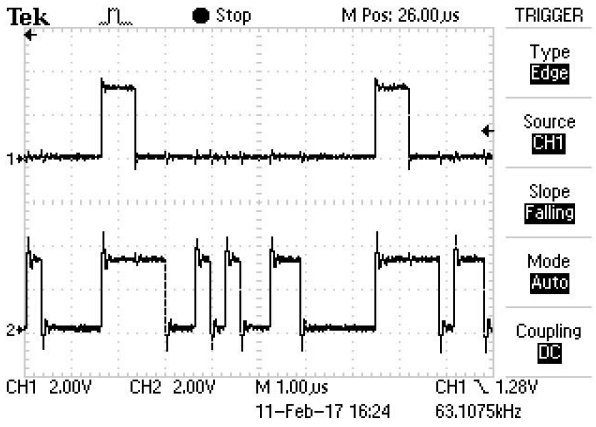

Figure 12. Output signals of SYNC (upper) and DIN (lower)

3.6. Experiment of Main Controller

The main controller module is tested through behavioral simulations because the number of pins observed is more than the pins available on the FPGA that are used. In the state initialization, the module has managed to give an initialization signal to the AD5308 controller module, the AD5676 controller module and the SDR SDRAM controller module after 100 µs and then move the state when all the modules have finished initializing. In the state write time set, the module succeeds in receiving time set data in a specific order through the UART system module and provides the data set time to the MAX19005 controller module, the AD5308 controller module and the AD5676 controller module. In state write pattern, the module successfully converts 8 bits of data vector pattern from the UART system to be written on the SDR SDRAM controller module in the form of 16 bits of data. In the state run test, the module successfully gives the pattern command data taken from memory via the SDR SDRAM module to the MAX19005 controller module to generate logic on the input pin and compare the logic to the output pin. The module can write the results of the run test, namely the data first fail, second fail and number of failed patterns on the UART system module when the test is complete.

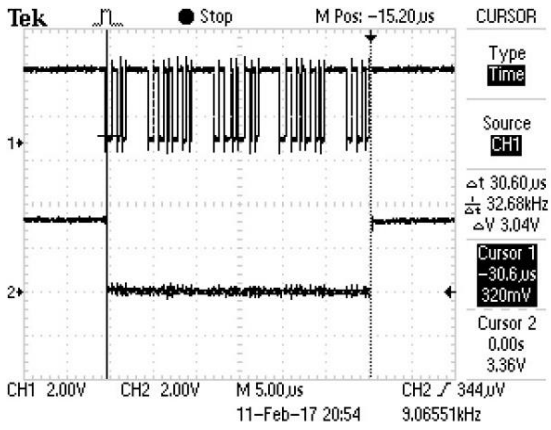

Figure 13. Sawtooth waves generated (lower) from channel 1 of 2 pieces AD5676F

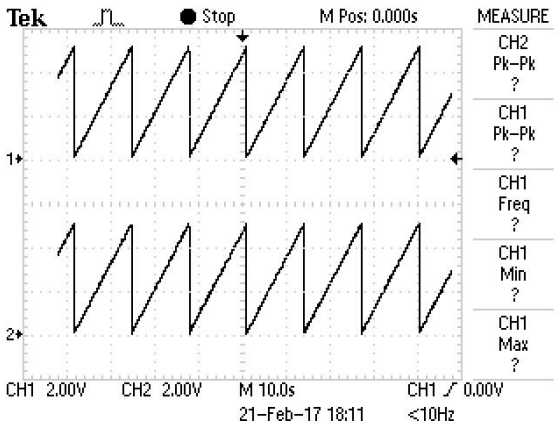

Figure 14. Output signals of SDI (upper) and SYNC

3.7. Experiment of Overall System

Experiment of overall system is presented by behavioral simulation. The behavioral simulation for overall system testing is shown in Figure 15. It could be seen that each time frame separates each state that is being experienced by the system. The first time frame shows the system is in the state initialization, then the system will go to idle state. In the second time frame, the system receives the start time set indicator, so that the system will move to the state time set then to state prepare. After the system sends data via SPI communication to IC MAX19005, AD5308 and AD5676 then the system will return to idle state. The third time frame shows the state write pattern. When the system receives a vector pattern from a PC and the system will write it to memory. After the stop pattern indicator is received, the system will return to idle state. Next is the fourth time frame, which shows the state run test.

After SDR SDRAM IC initialization is completed, the system will give an auto command refresh until the system enters state write pattern or state run test. There are some settings for the AD5308 IC and activate the daisy chain operation mode for four ICs AD5676. At the state time set and prepare, the system will receive the data set time of each channel then forward the data to IC MAX19005, AD5308 and AD5676. Time set data regarding active load and on / off channel is sent via SPI communication to MAX19005 IC. Load voltage data is sent to the IC AD5308. The third time frame shows the state write pattern. Start write pattern data indicator is sent firstly then one cycle of vector pattern is written. Value of the vector pattern written on memory matches with the vector pattern sent via serial communication. In the state run test, there are two processes that run together, namely reading process of vector pattern on memory and test process connected to DUT. So, after the reading process of vector patterns on memory, then data will be processed and stored in a buffer to be read when the test is given to the DUT. The system has managed to run each state in accordance with the design. By observing the RS-232 transmitter output and RS-232 receiver input, it can be concluded that UART communication was successfully carried out.

4. CONCLUSION AND FUTURE WORK

In this paper, research on advanced ATE for digital system by using FPGA was presented. Based on experiment results, the UART system works at a 19200 baud rate with 100% success rate. SDR SDRAM The controller manages to read and write at speeds of 80 and 90 ns per cycle. The success rate of reading and writing data is 100%. AD5308 controller successfully ordered the AD5308 to generate a certain voltage on a particular channel. AD5676 controller successfully ordered AD5676 by using daisy chain operations to generate voltage on certain ICs and channels.

Based on observations on behavioral simulations, MAX19005 controller has worked well. It takes 4,005 µs to send a data packet channel arrangement. Based on observations on behavioral simulations, the main controller module has worked well. Overall system works accordingly with the design, the system can provide initialization output on the IC used, receive time data set via serial communication then give output settings to MAX19005 and DAC used, receive vector pattern data via serial communication and write it to SDR SDRAM and the system can run tests when instructed and send test results data in accordance with the design.

Performance enhancements are needed, for example increasing the efficiency of main controller design by designing it based on a computer architecture system. By using two memories for vector patterns and result patterns, the system is expected to have the ability to store the results of each cycle pattern during the run test. By using a burst read reading system to accelerate reading of vector patterns on SDRAM, the minimum period that can be executed on a single cycle vector pattern is expected to be smaller.

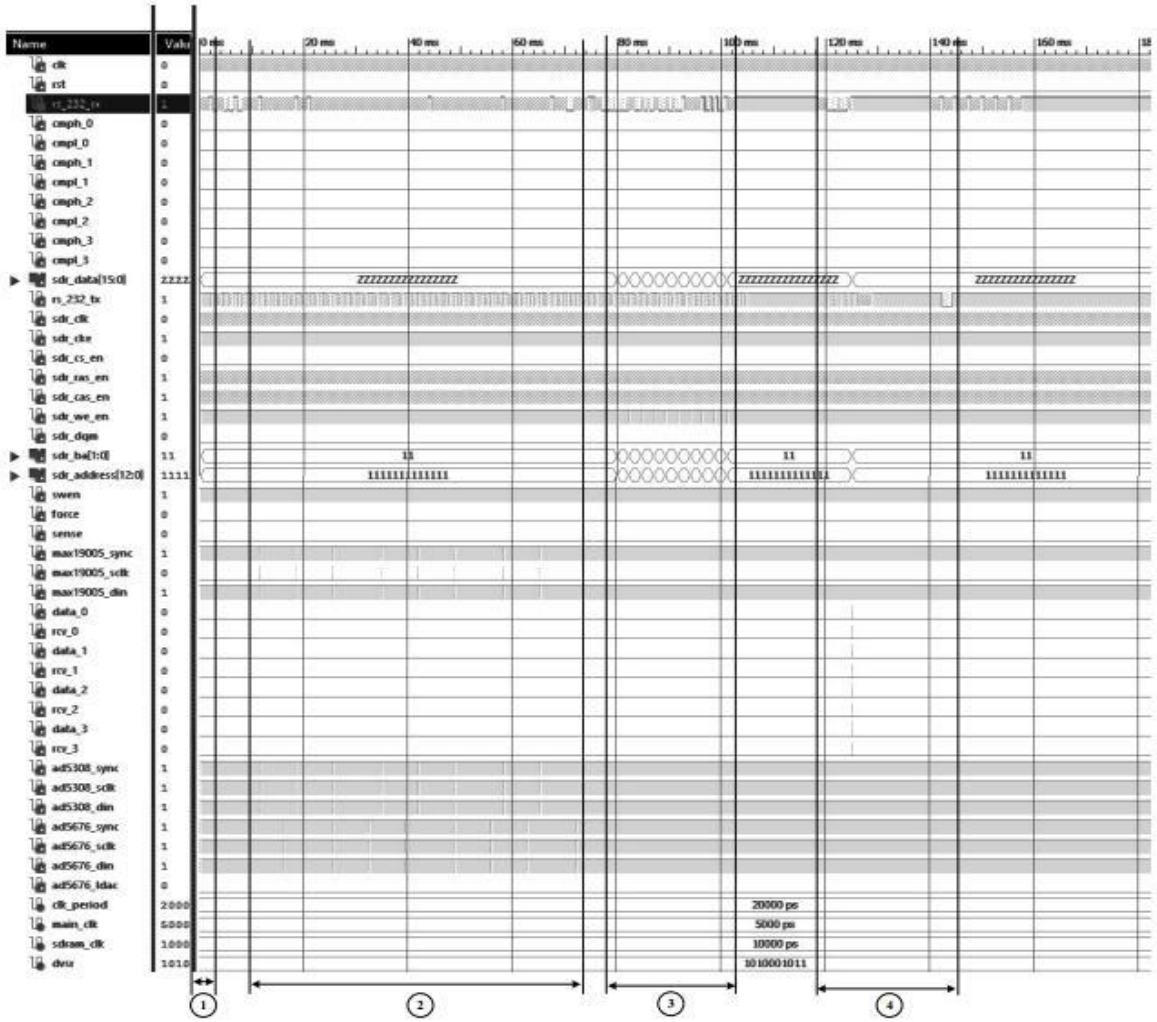

Figure 15. Behavioral simulation of overall system

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