

## Comparative analysis of positive output super lift DC-DC Luo converters

Richa Adlakha<sup>1</sup>, Anita Khosla<sup>2</sup>, Dheeraj Joshi<sup>3</sup>

<sup>1,2</sup>Manav Rachna International Institute of Research & Studies, India

<sup>3</sup>Delhi Technological University, India

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### ABSTRACT

Due to the advancement in the semiconductor technologies, DC-DC converters are gaining the importance in several industrial applications. They form the core of the switched mode power supplies which are used in real time applications. The performance of the conventional converter is affected by the parasitic elements and their voltage gain is also limited. To improve upon this, Super lift converters were developed by Luo. Voltage lift technique increases the voltage in geometric progression. These super lift converters are classified as positive output and negative output which are further classified into different series. In this paper series of Positive output Super lift converter topologies are analyzed. The proportional-integral controller is employed to these converters in the paper. These converters boost the voltage up to three times the input voltage and gaining importance in Electric vehicles and Solar powered applications. The simulations are carried in PSIM.

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### Corresponding Author:

Richa Khera,

Department Electrical & Electronics Engineering,

Faculty of Engineering,

Manav Rachna International Institute of Research & Studies, Haryana, India.

Email: richaadlakha.fet@mriu.edu.in

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## 1. INTRODUCTION

Due to the advancement in the semiconductor technology the power electronic based converter are gaining the utmost importance for the various applications in the industries. The reason behind this is due to the reduced cost of semiconductor switches and capability of the devices to work on the high frequencies. The power converter is used in the switched mode power supplies for many applications which previously use the linear regulators. These voltage regulators are based on the voltage or current dividing principle and are not efficient. These linear regulators provide the output voltage less than the input voltage. These have low frequency range but provide the high quality of the voltage. Based on this it is desired to use the switching regulator at higher frequency which comprises of the power semiconductor switch with high switching. By using this power loss is reduced in on & off state and the efficient conversion efficiency is obtained. The high switching power electronic converters are employed in DC-DC [1]. The main function of these converter are: (a) it will convert the fixed dc voltage to a variable one, (b) it will give the regulated output voltage, (c) it is used for maximum point power tracking in solar application, (d) it provides the isolation from input to the output, (e) it reduces the effect of Electromagnetic Interference. The converters are majorly classified as based on the switching i.e hard switching converter pulse width, resonant converter and soft switching converter. There are six generations of DC-DC converters which are reviewed in this paper.

These converter works either in the open loop mode or in the closed loop mode. Basic topologies of DC-DC converters [2] are buck, boost, buck boost converter. All other topologies are derived from these

fundamental [3]. They are non isolated converter but practically their performance is effected by the parasitic elements which produces ripples in the output [4, 5]. But by using higher order converter known as Luo converter which is based on the voltage lift techniques [6], the effect of the parasitic element is reduced. Advanced Luo converter is being studied in this paper. By using the Luo converter voltage boost is high and the effect of parasitic element is reduced. Thus these converters have provided efficient solution in electric vehicle applications and as a reliable power supplies.

## 2. GENERATION OF DC-DC CONVERTERS

There are various converter topologies that is more than 500. These are sequentially sorted in six generations by the Prof Luo and Dr. Ye based on the broad categorization based on basic converter, multi-quadrant operations, soft switching capabilities etc. [7] first quadrant are the classical converters and most of the popular converter comes only in this category. These first generation is also further classified as:

- a. Simple Topology: The basic converters such as Buck [8], Boost, Buck-Boost Topology comes under this fundamental category.
- b. Derived Topology: Under this category Positive output Luo Converter negative output Luo converter, double output Luo converter, cuk converter, single Ended primary inductance converter (SEPIC) comes under this criterion .
- c. Topologies including transformer: the converter topologies which include the transformer action such forward converter, push pull converter, fly back converter, half-bridge converter, bridge converter, zeta converter.
- d. Voltage Lift Topology: The topologies which are based on the voltage lifting technique are self lift converter ,positive output Luo converter ,negative output Luo converter ,double output Luo converters comes under this category.
- e. Super lift topology: In this voltage gain is increased in geometric series, they are positive/negative output super-lift luo converter, positive/negative output cascade boost converters.
- f. Ultra lift topologies: Ultra lift Luo-converter which have very high boosting capability comes in this category.

The fundamental topologies such as buck, boost, buck-boost topologies have the effect of the parasitic elements and they work in the low power [9] range and their overall power transfer efficiency is restricted. So to overcome these factors topologies based on the voltage lift (VL) techniques was developed the researcher. The VL technique is used to increase the voltage transfer gain by arithmetic series, in superlift converter voltage gain is increased by geometric progression [10]. In this paper Luo converter is simulated in its closed loop mode and the proportional Integral control is used for controlling the output voltage of the converter.

### 2.1. Super-Lift DC-DC Luo Converter

The super lift converter is one of the power full technique [11] to boost the voltage level. This technique uses geometric progression to increase the voltage by stage to stage. The Super lift converter are further classified as:

- a. Positive Output(P/O) super-Lift Luo DC-DC converter
- b. Negative Output(N/O) super-Lift Luo DC-DC converter
- c. Positive Output (P/O)cascade DC-DC boost converter
- d. Negative Output (N/O)cascade DC-DC boost converter

The Positive Output super-Lift Luo DC-DC converter [12] are simulated in this paper and closed loop integral control is used. These P/O super lift converter are divide further into four series based on the voltage increment number of the inductors, [13] capacitor and circuit topologies are different. These converters gives the high boost up in the voltage as compared to the conventional boost converters and the effect of the parasitic elements is being reduced. The subseries of these converter is as follows:

- a. Main series converter topology
- b. Additional series converter topology
- c. Enhanced series converter topology
- d. Re-enhanced series converter topology
- e. Multi enhanced series of converter topology

The main series P/O super lift converter are further classified as Elementary circuit, re-lift circuit, triple lift circuits and Additional series converter topology as additional circuit topology, additional re-lift and additional triple lift circuit.

**2.2. Analysis of P/O Superlift Converter-Elementary Circuit Topology**

The elementary topology of the main series converter consists of a switch, two diodes and a inductor and capacitor [14]. The circuit diagram with its switching states is shown in Figure 1. Now as the switch is turned on voltage across the capacitor is charged to the voltage  $V_{in}$  and the current through the inductor is increased to  $i_{L1}$  during the turn on time.

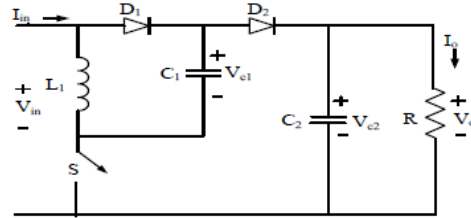


Figure 1. Elementary SL P/O converter

During the switch on time the capacitor is charged up to the input voltage and the current flowing through the inductor increases in the time  $kT$  [15]. And during the turn off time of the switch the inductor current decreases and voltage is  $(V_o-2V_{in})$ .

$$\Delta i_{in} = \frac{V_{in} \times k \times T}{L_1} = \frac{V_o - 2V_{in}(1-k)T}{L_1} \tag{1}$$

$$V_o = \left(\frac{2-k}{1-k}\right) V_{in} \tag{2}$$

$$G = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right) \tag{3}$$

Where  $G$  is the voltage transfer gain,  
Now,

$$i_{in} = i_{L1} + i_{C1} \tag{4}$$

$$i_{inon} = i_{L1on} + i_{C1on} \tag{5}$$

$$i_{inoff} = i_{L1off} = i_{C1off}$$

The value  $i_{L1}$  is generally equal to the average value of the inductor as the  $L$  is large, so:

$$i_{inoff} = i_{C1off} = I_{L1}$$

$$i_{inon} = I_{L1} + \left(\frac{1-k}{k}\right) I_{L1} = (2-k) I_{L1} \tag{6}$$

$$i_{C1on} = \left(\frac{1-k}{k}\right) I_{L1} \text{ and the value of average current is given by:}$$

$$I_{in} = k i_{inon} + (1-k) i_{inoff} = I_{L1} + (1-k) i_{L1} \tag{7}$$

Putting  $t=1/f$ ,

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_o}{I_o} = \left(\frac{1-k}{2-k}\right)^2 \tag{8}$$

And the inductor current variation ratio is given by:

$$\xi = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{k(2-k)TV_{in}}{2L_1 I_{in}} = \frac{k(1-k)^2 R}{2(2-k)fL_1} \tag{9}$$

Ripple in the output voltage is given by:

$$\Delta V_o = \frac{\Delta Q}{C_2} = \frac{I_o(1-k)}{C_2} = \frac{(1-K)V_o}{fC_2R} \tag{10}$$

Output voltage variation ratio is given by:

$$\varepsilon = \frac{V_{o/2}}{V_o} = \frac{1-k}{2RfC_2} \tag{11}$$

Similarly the relift super lift converter topology can be obtained using the more number of the energy storage elements and diodes and variations in the output voltage and current variations can be calculated [16].

The gain for the various stages of the positive output super lift Luo converter can be calculated as:

$$V_o = \left(\frac{2-k}{1-k}\right)^n V_{in} \tag{12}$$

$$G = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right)^n \tag{13}$$

- Where n = 1 for elementary circuit
- n = 2 for relift topology
- N = 3 for triple lift
- N = 4 for quad lift topology
- N = 5 quintuple lift topology

Each topology has different number of the elements. The main advantage of using these converter topologies is the reduction in the effect of the parasitic elements of the converters.

### 2.3. State Space Modeling

The state modeling of the elementary circuit of Luo converter is done [17]. When the switch is turned on then its state,

$$\dot{X} = A_1x + B_1u \text{ at Turn ON time}$$

$$\dot{X} = A_2x + B_2u \text{ at Turn Off time}$$

State space modeling is done using considering the effect of the parasitic resistance and capacitance. The turn on topology is depicted in the Figure 2.

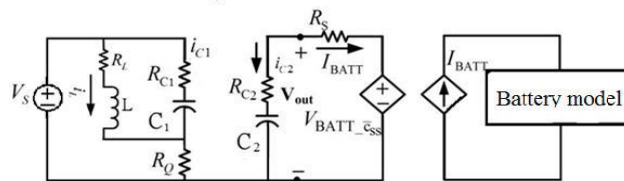


Figure 2. Turn On circuit of Elementary converter SL P/O converter

Here the capacitance,

$$I_L R_Q + I_L R_L + V_L = V_s \tag{14}$$

$$I_{C_1} R_{C_1} + V_{C_1} = I_L R_L + V_L \tag{15}$$

$$I_{BATT} * R_s + V_{BATT} = R_{C_2} I_{C_2} + V \tag{16}$$

$$\text{Where } X_1 = I_L \tag{17}$$

$$X_2 = V_{C_1} \tag{18}$$

$$X_3 = V_{C_2} \tag{19}$$

$$u_1 = V_s \tag{20}$$

$$u_2 = V_{BATT} \tag{21}$$

When switch is turned on:

$$\begin{pmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \end{pmatrix} = \begin{pmatrix} \frac{R_Q+R_L}{L} & 0 & 0 \\ -\frac{R_Q}{C_1 R_{C_1}} & -\frac{1}{(C_1 R_{C_1})} & 0 \\ 0 & 0 & \frac{-1}{(R_{C_2}+R_S)C_2} \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix} + \begin{pmatrix} \frac{1}{L} & 0 \\ \frac{1}{C_1 R_{C_1}} & 0 \\ 0 & \frac{-1}{(R_{C_2}+R_S)C_2} \end{pmatrix} \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} \tag{22}$$

And,

$$V_0 = I_{C_2} + V_{C_2} \tag{23}$$

$$V_{out} = \frac{V_{BATT}R_{C_2}}{R_{C_2}+R_S} + \frac{V_{C_2}R_S}{R_{C_2}+R_S} \tag{24}$$

$$I_{BATT} = \frac{-V_{BATT}}{R_{C_2}+R_S} + \frac{V_{C_2}}{R_{C_2}+R_S} \tag{25}$$

$$V_{out} = y_1 \tag{26}$$

$$I_{BATT} = y_2 \tag{27}$$

$$\begin{pmatrix} y_1 \\ y_2 \end{pmatrix} = \begin{pmatrix} 0 & 0 & \frac{R_S}{R_{C_2}+R_S} \\ 0 & 0 & \frac{1}{R_{C_2}+R_S} \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix} + \begin{pmatrix} 0 & \frac{R_{C_2}}{R_{C_2}+R_S} \\ 0 & \frac{1}{R_{C_2}+R_S} \end{pmatrix} \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} \tag{28}$$

Turn Off Time:

When Switch is turned off as shown in Figure 3 then the capacitor C1 and inductor L1 discharges [18 ] via load and during this period state equation are as follows:

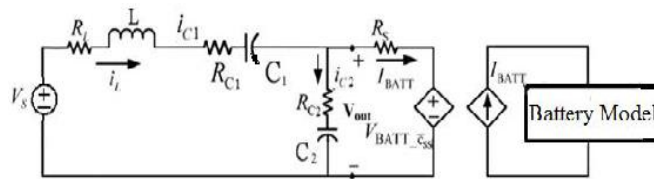


Figure 3. Turn OFF circuit of Elementary converter SL P/O converter

$$I_L = I_{C_2} + I_{BATT} \tag{29}$$

$$I_{BATT} * R_S + V_{BATT} = R_{C_2}I_{C_2} + V_{C_2} \tag{30}$$

$$\frac{dV_{C_2}}{dt} = \frac{R_S}{(R_{C_2}+R_S)C_2} + \frac{V_{BATT}}{(R_{C_2}+R_S)C_2} - \frac{V_{C_2}}{(R_{C_2}+R_S)C_2} \tag{31}$$

$$\frac{dI_L}{dt} = \frac{-((R_L+R_{C_1})(R_{C_2}+R_S)+R_{C_2}R_S)I_L}{(R_{C_2}+R_S)L} + \frac{V_{C_1}}{L} - \frac{V_{BATT}}{(R_{C_2}+R_S)L} - \frac{V_{C_2}R_S}{(R_{C_2}+R_S)L} + \frac{V_S}{L} \tag{32}$$

$$\begin{pmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \end{pmatrix} = \begin{pmatrix} \frac{-((R_L+R_{C1})(R_{C2}+R_S)+R_{C2}R_S)}{(R_{C2}+R_S)L} & \frac{1}{L} & -\frac{R_S}{(R_{C2}+R_S)L} \\ -\frac{1}{C_1} & 0 & 0 \\ \frac{R_S}{(R_{C2}+R_S)C_2} & 0 & -\frac{1}{(R_{C2}+R_S)C_2} \end{pmatrix} \begin{pmatrix} X_1 \\ X_2 \\ X_3 \end{pmatrix} + \begin{pmatrix} \frac{1}{L} & -\frac{1}{(R_{C2}+R_S)L} \\ 0 & 0 \\ 0 & \frac{1}{(R_{C2}+R_S)C_2} \end{pmatrix} * \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} \quad (33)$$

At turn off times output equations are as follows:

$$V_{out} = \frac{R_{C2}R_S I_L}{R_{C2}+R_S} - \frac{V_{BATT}R_{C2}}{R_{C2}+R_S} + \frac{V_{C2}R_S}{R_{C2}+R_S} \quad (34)$$

$$I_{BATT} = \frac{R_{C2}}{R_{C2}+R_S} I_L - \frac{V_{BATT}}{R_{C2}+R_S} + \frac{V_{C2}}{R_{C2}+R_S} \quad (35)$$

$$\begin{pmatrix} y_1 \\ y_2 \end{pmatrix} = \begin{pmatrix} \frac{R_{C2}R_S}{R_{C2}+R_S} & 0 & \frac{R_S}{R_{C2}+R_S} \\ \frac{R_{C2}}{R_{C2}+R_S} & 0 & \frac{1}{R_{C2}+R_S} \end{pmatrix} * \begin{pmatrix} X_1 \\ X_2 \\ X_3 \end{pmatrix} + \begin{pmatrix} 0 & \frac{R_{C2}}{R_{C2}+R_S} \\ 0 & -\frac{1}{R_{C2}+R_S} \end{pmatrix} * \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} \quad (36)$$

#### 2.4. Application of Averaging Technique

The state equations for both turn On time and Turn off times were obtained and the average is taken of both the conduction time to obtained the final state matrix [19].

Here,

$$d^1 = (1 - d)$$

$$\begin{pmatrix} A \\ B \end{pmatrix} = \begin{pmatrix} A_1 & A_2 \\ B_1 & B_2 \end{pmatrix} * \begin{pmatrix} d \\ d^1 \end{pmatrix}$$

$$\begin{pmatrix} C \\ D \end{pmatrix} = \begin{pmatrix} C_1 & C_2 \\ D_1 & D_2 \end{pmatrix} * \begin{pmatrix} d \\ d^1 \end{pmatrix}$$

$$A = \begin{pmatrix} \frac{-((R_Q+R_L)d+((R_L+R_{C1})(R_{C2}+R_S)+(R_{C2}R_S))d^1)}{L} & \frac{d^1}{L} & \frac{-R_S d^1}{L} \\ \frac{-R_Q d - R_{C1} d^1}{C_1 R_{C1}} & \frac{-d}{C_1 R_{C1}} & 0 \\ \frac{R_S d^1}{(R_{C2}+R_S)} & 0 & \frac{-1}{(R_{C2}+R_S)C_2} \end{pmatrix} \quad (37)$$

$$B = \begin{pmatrix} \frac{1}{L} & \frac{d^1}{(R_{C2}+R_S)L} \\ \frac{d}{C_1 R_{C1}} & 0 \\ 0 & \frac{1}{(R_{C2}+R_S)C_2} \end{pmatrix} \quad (38)$$

$$C = \begin{pmatrix} \frac{R_S R_{C2} d^1}{R_{C2}+R_S} & 0 & \frac{R_S}{R_{C2}+R_S} \\ \frac{R_{C2} d^1}{R_{C2}+R_S} & 0 & \frac{1}{R_{C2}+R_S} \end{pmatrix} \quad (39)$$

$$D = \begin{pmatrix} 0 & \frac{R_{C2}}{R_{C2}+R_S} \\ 0 & \frac{-1}{R_{C2}+R_S} \end{pmatrix} \quad (40)$$

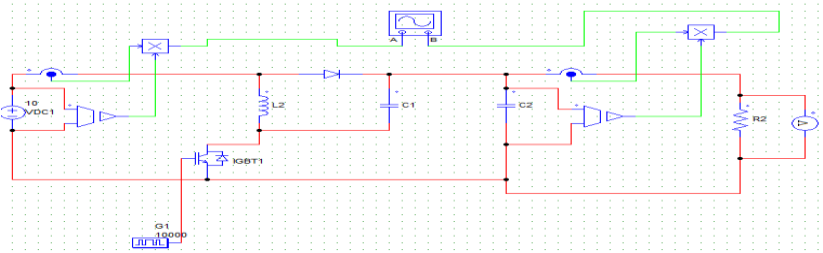
### 3. SIMULATION OF THE SUPER LIFT LUO CONVERTER

The main series of the positive output super lift converters are further classified as Elementary converter, relift converter, triple lift converter.

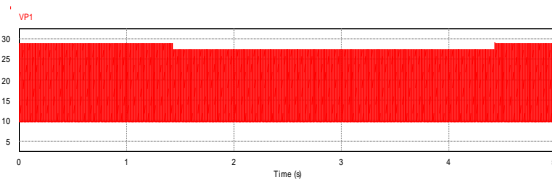
**3.1. Elementary Topology**

The elementary topology of DC-DC converter is simulated with the values of inductor 10 mH and capacitance 2uF and input voltage of 10V using the power sim (PSIM ) software package. The output voltage is boost up to 3 times the input voltage as shown in Figure 4. The elementary topology of the converter works in its open loop control mode [20]. Voltage transfer gain of the elementary topology is given by:

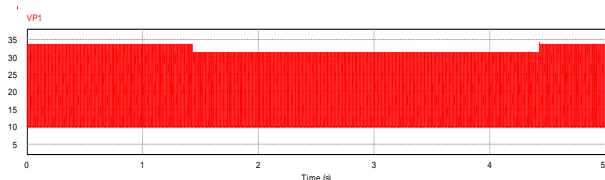
$$G = \left( \frac{2-k}{1-k} \right) \tag{41}$$



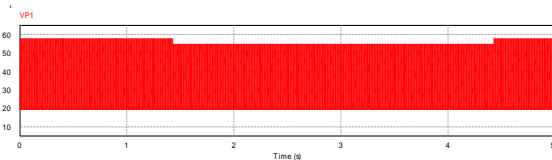
(a)



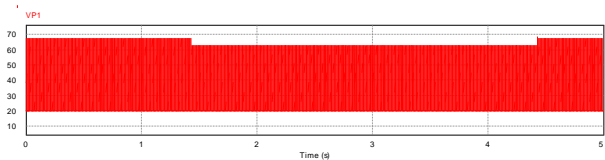
(b)



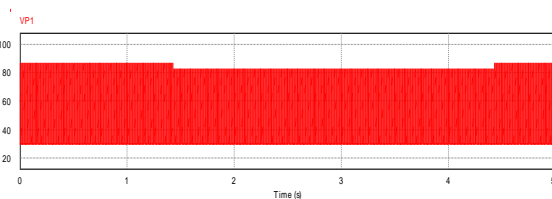
(c)



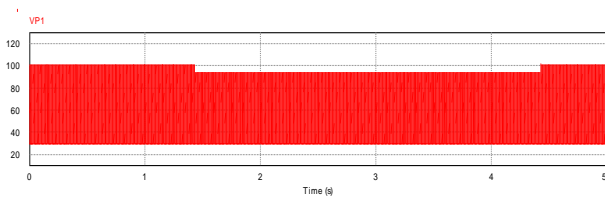
(d)



(e)



(f)

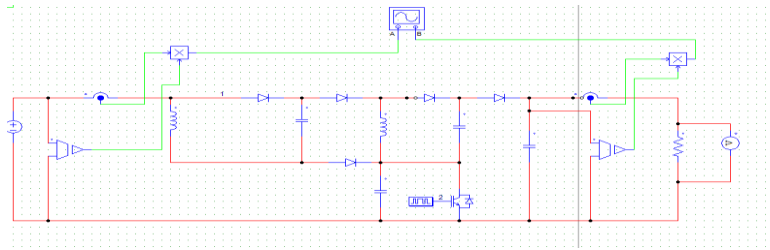


(g)

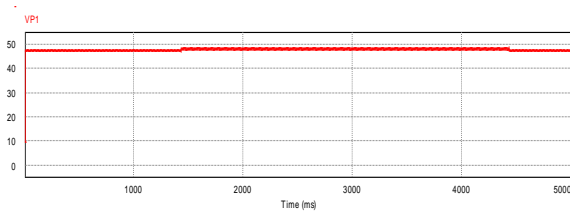
Figure 4(a). Model of elementary super lift converter in PSIM, 4(b): load voltage waveform of the elementary super lift converter without feedback control with k=.5, 4(c) Vin =10V & k=.6, (d) Vin = 20V & k=.5, 4(e) Vin = 20V & k=.6, 4(f) Vin = 30V & k=.5, 4(g) Vin = 30V & k=.6

**3.2. Relift Converter**

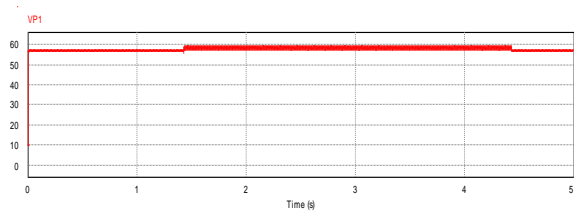
The relift converter as shown in Figure 5 is in its open loop but the number of capacitors and inductors are increased in comparison to the elementary topology [21]. The circuit is simulated in open loop with values of L1=L2=L3=L=10mH and C1=C2= 2uF in PSIM [22] with switching frequency of 10 kHz [23]. the voltage gain in relift converter is given by:



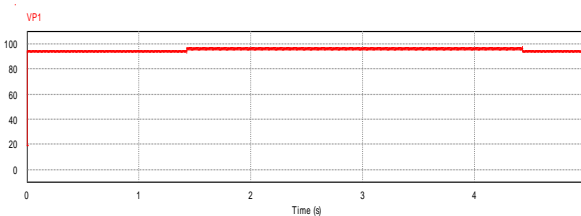
(a)



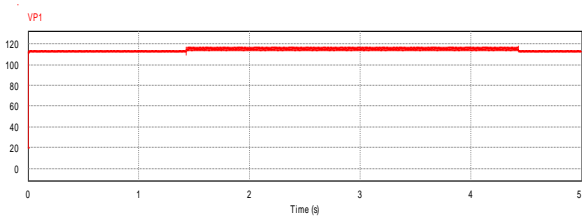
(b)



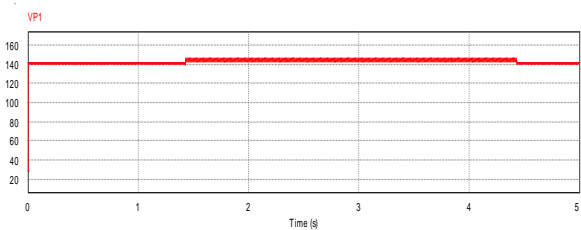
(c)



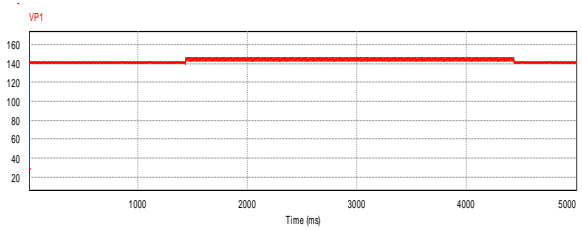
(d)



(e)



(f)



(g)

Figure 5(a). Simulation Model of Re-lift super lift converter in PSIM, 5(b): Load voltage waveform of the Re-lift topology with  $k=.5$ , 5(c)  $V_{in} = 10V$  &  $k=.6$ , 5(d)  $V_{in} = 20V$  &  $k=.5$ , 5(e)  $V_{in} = 20V$  &  $k=.6$ , 5(f)  $V_{in} = 30V$  &  $k=.5$ , 5(g)  $V_{in} = 30V$  &  $k=.6$

$$G = \left(\frac{2-k}{1-k}\right)^2 \quad (42)$$

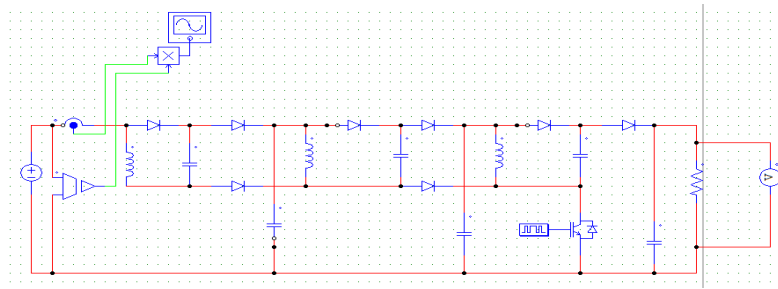
### 3.3. Triple Lift Converter

The triple lift converter topology is implemented [24] with six capacitors, eight diodes, three inductors and one semiconductor switch. With the values of  $L = 10mH$ ,  $C=2\mu F$  and switching frequency 10kHz. The output voltage waveform is shown in Figure 6.

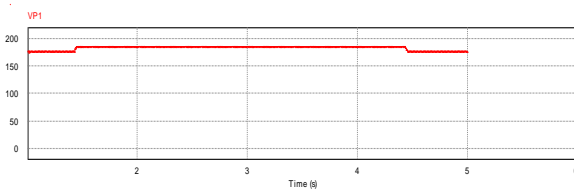
The voltage gain is given by [25]:

$$V_O = \left(\frac{2-k}{1-k}\right)^3 \quad (43)$$

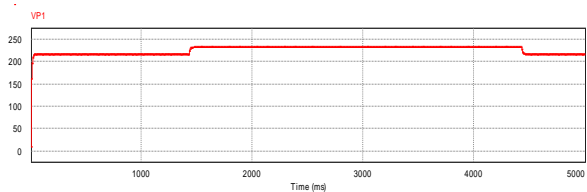




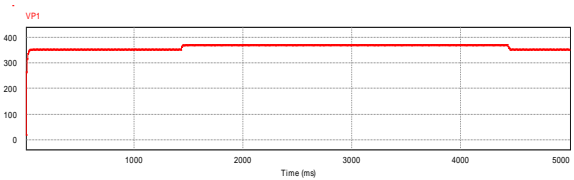
(a)



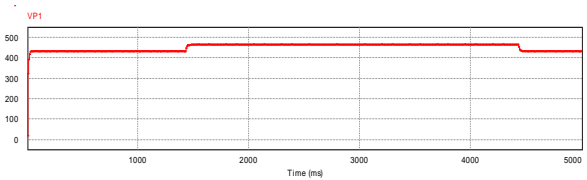
(b)



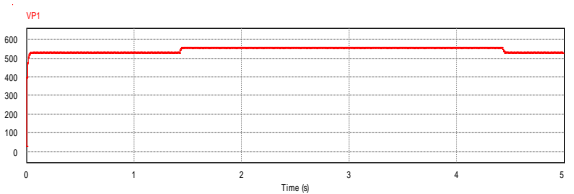
(c)



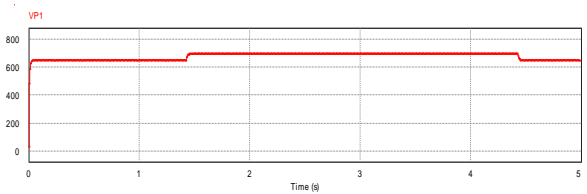
(d)



(e)



(f)



(g)

Figure 6(a). Simulation Model of Triple-lift super lift converter in PSIM, 6(b): Load voltage waveform of the Triple-lift topology with  $k=0.5$ , 6(c)  $V_{in} = 10V$  &  $k=0.6$ , 6(d)  $V_{in} = 20V$  &  $k=0.5$ , 6(e)  $V_{in} = 20V$  &  $k=0.6$ , 6(f)  $V_{in} = 30V$  &  $k=0.5$ , 6(g)  $V_{in} = 30V$  &  $k=0.6$

#### 4. CONCLUSION

This paper presented the different topologies of main series positive output Luo converter. The efficiency of the Luo converter is very high and gives high voltage gain. The analysis of the Elementary topology of the main series of the Luo superlift converter was done. The state space model of this converter topology was developed. The triple lift converter topology the voltage is boost upto maximum and the effect of the parasitic elements is much reduced and stable output is achieved. The results are validated using the theoretical analysis.

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