Indonesian Journal of Electrical Engineering and Computer Science
Vol. 14, No. 1, April 2019, pp. 407~412
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v14.i1.pp407-412

Linearity improvement of differential CMOS low noise amplifier

Maizan Muhamad[1], Norhayati Soin[2], Harikrishnan Ramiah[3]
[1]Faculty of Electrical Engineering, Universiti Teknologi MARA, ShahAlam, Malaysia
[1,2,3]Faculty of Engineering, University of Malaya, Kuala Lumpur, Malaysia

Article Info

Article history:

Received Sep 30, 2018
Revised Nov 27, 2018
Accepted Dec 15, 2018

Keywords:

CMOS
Differential
Linearity
Low noise amplifier (LNA)
Noise figure (NF)

ABSTRACT

This paper presents the linearity improvement of differential CMOS low noise amplifier integrated circuit using 0.13um CMOS technology. In this study, inductively degenerated common source topology is adopted for wireless LAN application. The linearity of the single-ended LNA was improved by using differential structures with optimum biasing technique. This technique achieved better LNA and linearity performance compare with single-ended structure. Simulation was made by using the cadence spectre RF tool. Consuming 5.8mA current at 1.2V supply voltage, the designed LNA exhibits S21 gain of 18.56 dB, noise figure (NF) of 1.85 dB, S11 of −27.63 dB, S22 of -34.33 dB, S12 of −37.09 dB and IIP3 of -7.79 dBm.

Corresponding Author:

Maizan Muhamad,
Faculty of Electrical Engineering,
Universiti Teknologi MARA,
40450, ShahAlam, Malaysia.
Email: maizan@salam.uitm.edu.my

1. INTRODUCTION

Nowadays, complementary metal oxide semiconductor (CMOS) widely used in designing wireless system because of the low cost and easy integration. Low noise amplifier (LNA) is the first building block in the wireless system. Its main purpose is to provide gain while with minimum noise as possible to the network. As the first active block in the receiver chain, the performance of an LNA controls the overall performance of receivers. Noise performance and power gain are the most important characteristics of an LNA. Beside these characteristics, the main parameters affecting the selection of a proper circuit for an LNA are DC power consumption, bandwidth, stability, linearity, supply voltage and chip area.

Even though single-end LNA input stage consumes less power and the active chip area consumption is minimum, differential topology is preferred for the following important issues [1]. Since the noise figure is the critical factor for the LNA, by using differential signalling can offer better noise performance due to the ability of rejecting the common-mode noise. Theoretically, the two sides of the circuit are identically matched and therefore the common-mode noise of each side can be viewed as the same. Secondly, not only limiting towards the noise but also for the linearity performance, the differential mode amplifier exhibits better performance [2]. Due to the inherent circuit architecture which is symmetrical, the nature ability of cancelling the even-order distortions increases the linearity of the amplifier.

The signal to noise will be degraded due to the insufficient linearity of a LNA. Therefore, having a high linearity, IIP3 LNA can reduce the degradation of carrier to noise [3]. This linearity should not be at the expenses of gain or noise figure, NF.

In integrated analogue electronics and especially in RF applications, a fully differential approach is usually preferred, due to its well-known properties of immunity to common-mode disturbances, rejection to

parasitic couplings and increased dynamic range [3]. Although the differential operation must be preserved in the chip, there are cases where the input signal is single-ended such as RF image filters and IF filters in a RF receiver. In addition, there are circuits that require differential signals to perform their function. In these situations, a stage which can convert single-ended to differential signals is needed. Several highly integrated direct-conversion CMOS front-ends achieve high performance, but at the cost of requiring a fully differential LNA that needs two RF input pins and an external RF single-ended to differential conversion [4]. This typically requires special front-end filters or an additional off-chip balun, which can incur extra loss and can degrade the system noise figure [5, 6].

2. RESEARCH METHOD

The LNA is to be designed with the following proposed specification summarized in Table 1. Generally, the 0.13µm CMOS LNA is to be designed such as to comply with the wireless local area network (WLAN) specifications whereby the LNA needs to provide a high gain with low noise figure at low power, with its centre operating frequency at 2.4 GHz.

Table 1. LNA Design Specification for WLAN Standard

Parameter	Target specification
CMOS Process technology	0.13µm
Frequency band	2.4 GHz
Power supply	≤ 1.2 V
Gain, S_{21}	> 15 dB
Input matching (S_{11})	< - 12 dB

This LNA is constructed using an inductively degenerated cascode topology. The cascode topology is adopted as it provides high gain and good input-output isolation, which improve circuit design stability and also simplify input matching. The simplified schematic of the proposed CMOS LNA for noise optimization and gain enhancement is illustrated in Figure 1(a) and the simplified small-signal equivalent circuit is shown in Figure 1(b) where V_{RF} and R_S model the antenna.

Inductively degenerated topology has the advantage of better control over the value of the real part of the input impedance. The function of the L_s is to generate the real impedance to match the input impedance to 50Ω and hence good noise performance [7]. The inductively-degenerated CS LNA is to help the input matching.The small-signal model in Figure 1 (b) is used as a guide in order to determine the input impedance of the circuit. The subsequent derivations can illustrate how the input can be simply matched to the source resistance. Z_{in} is a RLC series network circuit with a resistive term which is straightly proportional to the value of the inductance. Where at resonance, the real term in Z_{in} contains L_s [8]

$$\text{Zin} = \frac{\text{Vg}}{\text{Ig}} = \frac{\text{IgRg+Vc+j}\omega\text{IsLs}}{\text{Ig}}$$

$$\text{Zin} = \frac{\text{Ls.gm}}{\text{Cgs}}$$

Where Z_{in} is 50 Ohms. In most LNA design the value of L_s was assumed and the values of g_m and C_{gs} are calculated based on the formula to find the required for Z_{in}. Consequently, in this input matching the utilization of degenerated inductor is needed. This make the presence of L_s helps in providing a right input impedance to terminate the off-chip RF filter in the preceeding the of the LNA, in which in the typical condition,need to match to 50Ω impedance. While L_g will resonate with C_{gs} and it guarantees that the input frequency adjusted to the operating frequency of the application. Hence during resonance, the source resistance and others parameter can be determined as the expression derived below [8]:

$$\omega_T = \frac{\text{gm}}{\text{Cgs}} = \frac{\text{Rs}}{\text{Ls}}$$

Where ω_T is defined as a cut off frequency. The value of the R_s is 50 ohms

$$Q_L = \sqrt{1 + \left({}^{1}/_{\text{p}}\right)}$$

$$\text{Where } p = \frac{\sigma.a^2}{5.\gamma}$$

The parameters for the p usually depend on the RFCMOS Technology, but typically γ is set between 2-3, σ is set to 2-3 times the value of Y and the α is assumed to be 0.8-1[9].

$$Lg = \frac{QL.Rs}{\omega o}.Ls$$

Where ω_o is the center frequency.

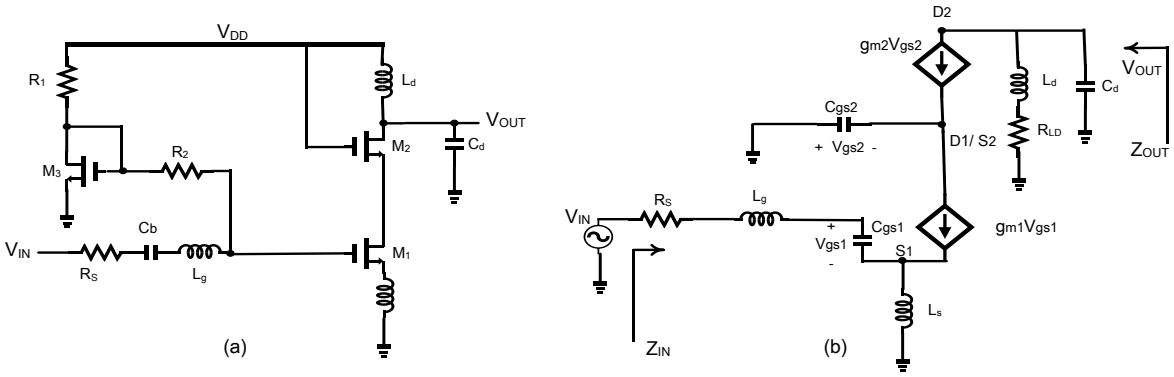


Figure 1. Simplified configuration of (a) the proposed single ended LNA and (b) the small-signal equivalent circuit

Figure 2 illustrates the modified differential LNA. The combination two circuit single ended will produce the double ended. For the sake of simplicity, the biasing circuit of differential LNA is not shown. The gate-source capacitance can be determined by below expression [8]:

$$Cgs = \frac{1}{\omega o^2(Lg+Ls)}$$

$$Cgs = \frac{2}{3}Cox.W.Lmin$$

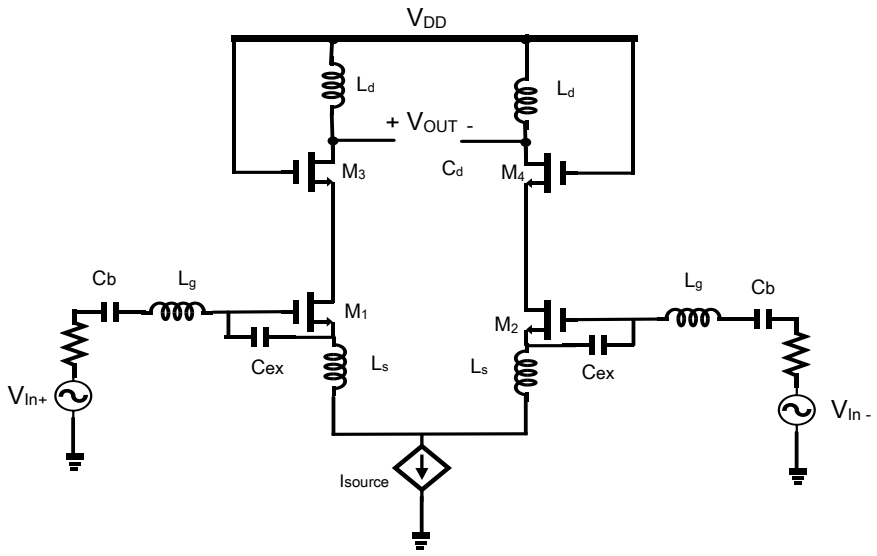


Figure 2. Inductively degenerated common source differential LNA

Which the width of transistor can be expressed as:

$$W = \frac{3}{2}\frac{Cgs}{2Cox.Lmin}$$

$$\varepsilon ox = \varepsilon ox.\varepsilon o$$

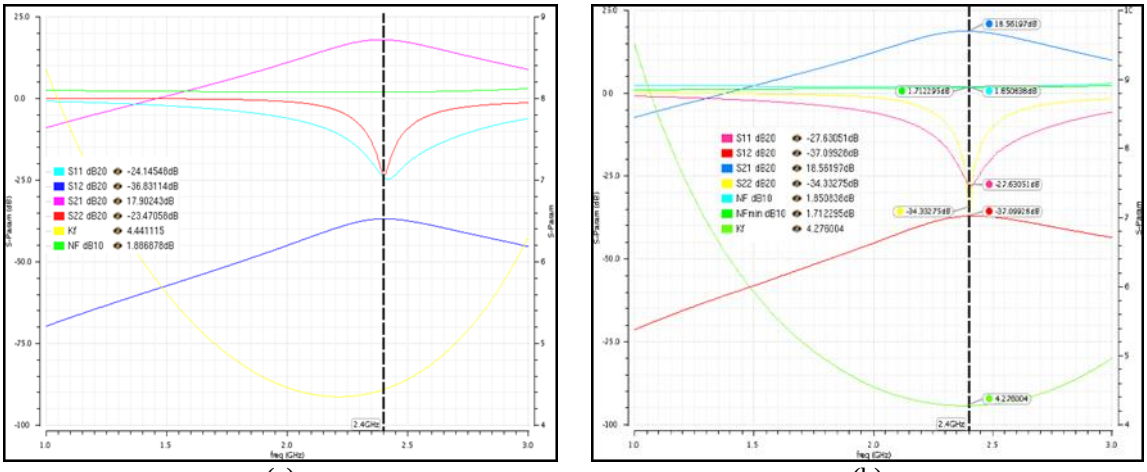
Where

$$\varepsilon o = \text{dielectric constant forfree space} = \frac{8.854E^{-14}F}{cm}$$

$$\varepsilon ox = \text{dielectric constant for silicon} = 3.9$$

3. RESULTS AND ANALYSIS

Figure 3 illustrates the simulation of s-parameters and noise figure for both single-ended and differential LNA. The S-parameter plots and noise figure performances are shown in Figure 3. As can be seen from Figure 3, the circuit's input and output were matched to the 50Ω required at the operating frequency of 2.4 GHz. Base from the curve, both structures exhibit good performance and satisfy the design requirement. The input return loss, S_{11} is -24.14 dB and -27.63 dB for single-ended and differential respectively. While the output return loss, S_{22} is -23.47 dB for single ended and -34.33 dB for differential structure. The noise figure for single ended LNA is 1.88 dB which is not much different with differential structures value 1.85 dB. The attained value of NF is believed to be good as it exceeds the requirement which is typically below 2 dB without having to trade off the power gain which also satisfies the requirement. Differential LNA obtain greater gain, S_{21} which is 18.56 dB as compared to single-ended 17.9 dB.



(a) (b)

Figure 3. S-parameters and noise figure performance: (a) single ended LNA, (b) differential LNA

Figure 4 presents the simulation performance of third order intercept point, IIP3. In order to simulate the IIP3, different value of input signal need to supply to the circuit and the fundamental frequency and the third order inter-modulation component. The single ended LNA achieved -10.6dBm while the differential manage to get -7.75 dBm. The linearity of the designed LNA improved differential improved by 2.85 dBm.

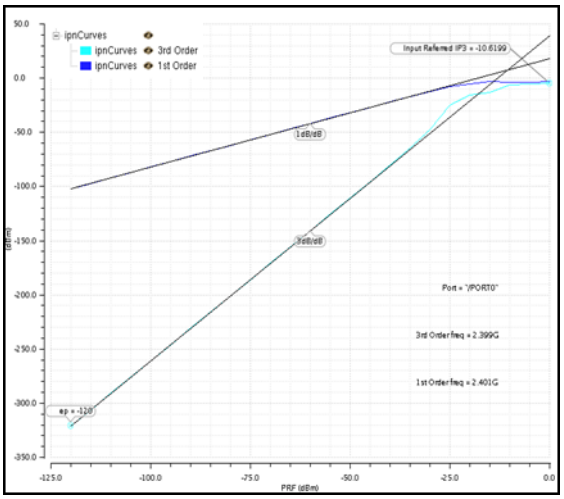


Figure 4. Simulation of Third Order Intercept Point (IIP3): (a) single ended LNA, (b) Differential LNA

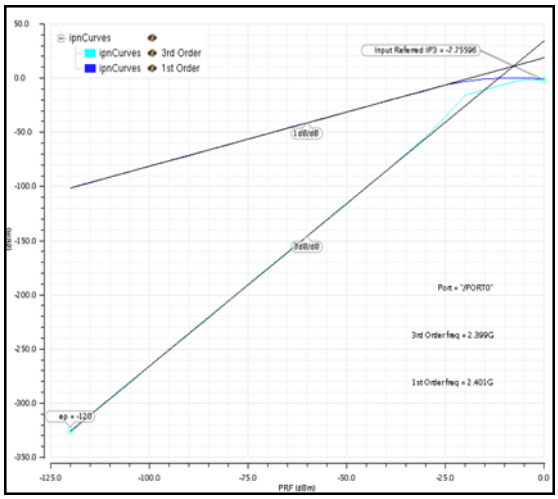


Figure 5 shows the physical representation (layout) of differential LNA using 6 octagonal spiral inductors

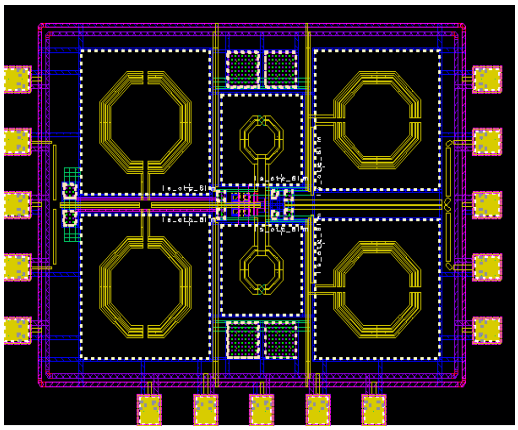


Figure 6. Layout of differential LNA

Table 2 summarize the simulation performance comparison of both structures. By using differential structures, the LNA achieved better linearity without trade off its noise figure and gain performance.

Table 2. Performance comparison of with other published work

LNA structure	S_{11} (dB)	S_{21} (dB)	S_{12} (dB)	S_{22} (dB)	NF (dB)	IIP3 (dBm)
Single-ended	-24.14	17.9	-36.83	-23.47	1.88	-10.61
Differential	-27.63	18.56	-37.09	-34.33	1.85	-7.79

4. CONCLUSION

In this paper, the design of differential LNA are successfully implemented using Silterra 130-nm CMOS technology. The LNA design exhibits high forward gain (S_{21}) of 18.56dB, high reverse isolation (S_{12}) of -37.09 dB and a good linearity IIP3 of -7.79 dBm at 2.4 GHz. The LNA shows a low NF of 1.85 dB. Linearity of the LNA is improved by using differential structures with optimum biasing technique. The LNA operates at 1.2V supply and consumes only 7mW of power.

REFERENCES

[1] Zokaei A, Amirabadi A. A 65 nm linear broad-band differential Low Noise Amplifier using post distortion technique. Microelectronics J. 2018;74(August 2017):24–33.
[2] Das DM, Srivastava A, Ananthapadmanabhan J, Ahmad M, Baghini MS. A novel low-noise fully differential CMOS instrumentation amplifier with 1.88 noise efficiency factor for biomedical and sensor applications. Microelectronics J. 2016;53:35–44.
[3] Zhang H, Member S, Sánchez-sinencio E, Fellow L, Paper I. Linearization Techniques for CMOS Low Noise Amplifiers : A Tutorial. 2011;58(1):22–36.
[4] Feng Y, Takemura G, Kawaguchi S, Kinget P. Design of a high performance 2-GHz direct-conversion front-end with a single-ended RF input in 0.13 μ m CMOS. IEEE J Solid-State Circuits. 2009;44(5):1380–90.
[5] Robens M, Wunderlich R, Heinen S. Differential Noise Figure De-Embedding: A Comparison of Available Approaches. IEEE Trans Microw Theory Tech. 2011 May;59(5):1397–407.
[6] Shim J, Jeong J. A band-selective low-noise amplifier using an improved tunable active inductor for 3–5 GHz UWB receivers. Microelectronics J. 2017;65(May):78–83.
[7] Fan XH, Zhang H, Member S, Sánchez-sinencio E. A noise reduction and linearity improvement technique for a differential cascode LNA. IEEE J Solid-State Circuits. 2008;43(3):588–99.
[8] Microelectronic C, Excellence D, Campus E, Noh NM, Zainal T, Zulkifli A, et al. Systematic Width Determination for the Design of Power-Constrained Noise Optimization Inductively Degenerated Low Noise Amplifier. IETE J Res. 2010;56(5):249–56.
[9] Microelectronic C, Excellence D, Campus E. Systematic Width Determination for the Design of Power-Constrained Noise Optimization Inductively Degenerated Low Noise Amplifier. 2011;56(5):249–56.