Indonesian Journal of Electrical Engineering and Computer Science
Vol. 14, No. 3, June 2019, pp. 1141~1147
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v14.i3.pp1141-1147

Improved reliable multilevel inverter for renewable energy systems

M. Sujatha, A.K. Parvathy
Department of Electrical and Electronics Engineering, Hindustan Institute of Technology and Science, India

Article Info

Article history:

Received Nov 20, 2018
Revised Jan 21, 2019
Accepted Feb 27, 2019

Keywords:

Mean time between failures
MIL-HDBK
Multilevel inverter
Reliability

ABSTRACT

New improved multilevel inverter (MLI) topology for Renewable energy systems is proposed in this paper. Cascaded multilevel inverters (CMLI) produce an output voltage level depending on the number of individual sources connected. The main drawback of CMLI is, as the output voltage level increases in number, the switches used in the device also increases and hence the complexity of the circuit increases. As the number of switches increases, the reliability of the circuit decreases. In this paper a novel MLI topology, which employs lesser number of switches, is proposed. A simulation model of CMLI and the proposed MLI has been built in MATLAB/SIMULINK. The reliability of the CMLI and the new topology MLI is analyzed by using MIL-HDBK-217.

Corresponding Author:

M.Sujatha,
Department of Electrical and Electronics Engineering,
Hindustan Institute of Technology and Science,
P.O. No 1, Rajiv Gandhi Salai, Padur, Chennai 600103, Tamilnadu, India.
Email: msujatha@hindustanuniv.ac.in

1. INTRODUCTION

The environmental concern and increasing power shortage has led to the world spread penetration of renewable energy. Increasing proportion of renewable energy contribution, power distribution and power quality issues have led to the advancement of new power converter topologies. Multilevel inverters can achieve high power using mature medium power semiconductor technology [1]. Multilevel inverter technology has gained popularity in industry for medium and high voltage applications. When compared with the traditional two-level inverter, the quality of output voltage produced by MLI is high. Currently, MLI are broadly used in various applications [2] such as High Voltage DC transmission, Flexible AC Transmission System (FACTS), hybrid electric vehicle systems (HEV) etc., Multilevel inverters can also be used in the grid connected systems without the use of bulky transformers.

The commercially available MLIs are Neutral Point Clamped (NPC) inverters, Flying capacitor (FC) inverters and Cascaded Multilevel Inverters (CMLI) [3]. For giving the same voltage level, different inverters follow different mechanism. Five level inverter used for photovoltaic application is broadly discussed [4]-[5]. NPC inverters have less number of capacitors than the FC inverters and CMLI. The limitation of NPC is the difficulty in the balancing of DC-link voltage [6] and because of this extra clamping diodes are needed. High number of capacitors are needed by FC inverter [7]. The CMLI [8] is designed by using H-bridges in series and its arrangement is simple than the other types of inverters. But in this, with increased output levels, the switches used for the converter operation also increases.

Main disadvantage of CMLI configuration is the increase in number of switching devices and its complex driver circuits [9]. Complexity of the system decreases the inverter's reliability. The reliability of inverter is critical for the smooth operation of connected photovoltaic system.

By developing new topology of inverters, the complexity can be decreased and hence the reliability can be increased [10]. By having inverters with less number of switches, for the similar voltage level, the reliability of the inverter can be improved.

In this paper a new multilevel inverter having lesser number of switches than the conventional CMLI is proposed and is analyzed. Further the reliability of this new inverter is compared with that of the existing CMLI and the results prove that the proposed inverter is more reliable than the CMLI.

2. CASCADED MULTILEVEL INVERTER (CMLI)

The circuit diagram of CMLI is shown in Figure 1. The CMLI is composed of a number of H-bridge units [11]. Output from either separate solar panels or individual DC units are connected to the H- bridge units as inputs. To obtain a multilevel output voltage, the AC outputs of individual H-bridge units are connected in series. For K number of individual DC sources, the number of levels of output phase voltage of CMLI is given by 2K+1. The Switch requirement of Cascaded Multilevel Inverter is given in Table 1.

Table 1. Switch Requirement for Cascaded Multilevel Inverter

Parameters	Cascaded			
Levels	7	9	11	13
Switches required	12	16	20	24

For a 7-level output phase voltage, 3 individual DC sources and 3 individual H-bridge units are required. The circuit diagram is shown in Figure 1.

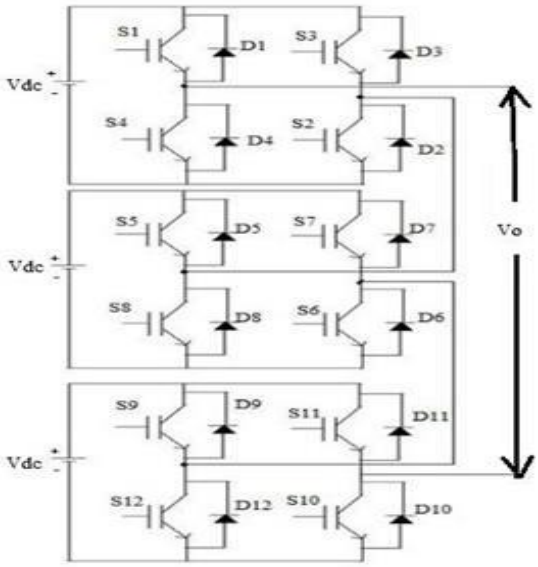

Figure 1. Circuit diagram of Cascaded Multilevel Inverter

The Switching Pattern of 7 level CMLI is given in Table 2.

Table 2. Switching Pattern of CMLI

Level	Switches in ON State	Output Voltage
3	S_1, S_2, S_5, S_6, S_9, S_{10}	+3 V_{dc}
2	S_1, S_2, S_5, S_6, S_{10}, S_{12}	+2 V_{dc}
1	S_1, S_2, S_6, S_8, S_{10}, S_{12}	+ V_{dc}
0	S_2, S_4, S_6, S_8, S_{10}, S_{12}	0
-1	S_3, S_4, S_6, S_8, S_{10}, S_{12}	-1 V_{dc}
-2	S_3, S_4, S_7, S_8, S_{10}, S_{12}	-2 V_{dc}
-3	S_3, S_4, S_7, S_8, S_{11}, S_{12}	-3 V_{dc}

Using MATLAB/SIMULINK for input voltage of $V_{dc1}=V_{dc2}=V_{dc3}=10V$, the simulation is performed and the output voltage waveform of Cascaded multilevel inverter is shown in Figure 2.

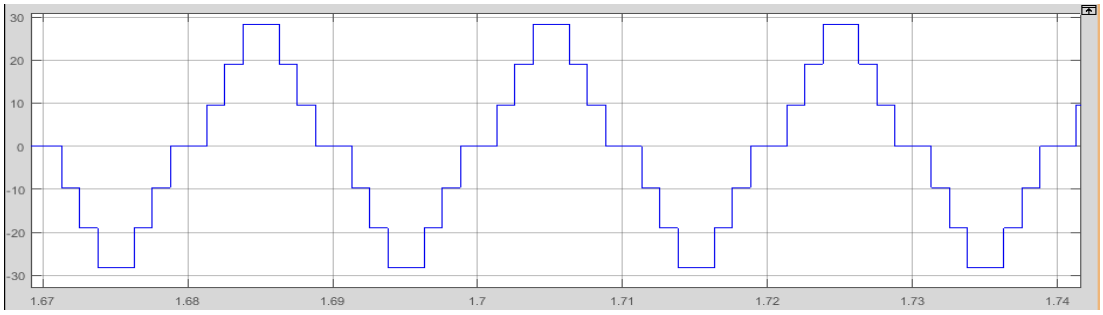

Figure 2. Simulation output of cascaded multilevel inverter

3. RELIABILITY ANALYSIS OF EXISTING CASCADED MULTILEVEL INVERTER

Reliability analysis of inverter is done using data given in Military handbook, MIL- HDBK-217 [12]. As the switch is most prone to failure, the reliability of the switch of the inverter is calculated [13]. All relations, equations and coefficients are referred from MIL- HDBK-217. For MOSFET Switch, the failure rate is given by (1),

$$\lambda_P=\lambda_b*\pi_T*\pi_A*\pi_Q*\pi_E \text{ failures/ } 10^6 \text{ Hours} \quad (1)$$

where λ_b = Base failure rate = 0.012;
π_Q= Quality Factor = 5.5; π_E= Environmental Factor = 1; π_C= Construction Factor = 1;
π_A= Application Factor = 10; π_T= Temperature Factor=exp[-1925*((1/T_j+273)+(1/298))]
$T_c = T_a + \theta_{ca} * P_{loss}$; $T_j = T_c + \theta_{jc} * P_{loss}$ $\theta_{jc} = 0.25$, $T_a = 27$, $\theta_{ca}=1$
$P_{loss}= I^2*R_{on}*D$, where R_{on} is the drain-source resistance of the MOSFET
I is the RMS value of current through the switch

For calculating the power loss of the switches and hence the reliability, the switch current waveforms are analysed. Gate pulse and Current waveforms of switches S_1, S_2, S_3 & S_4 of CMLI is shown in Figure 3.

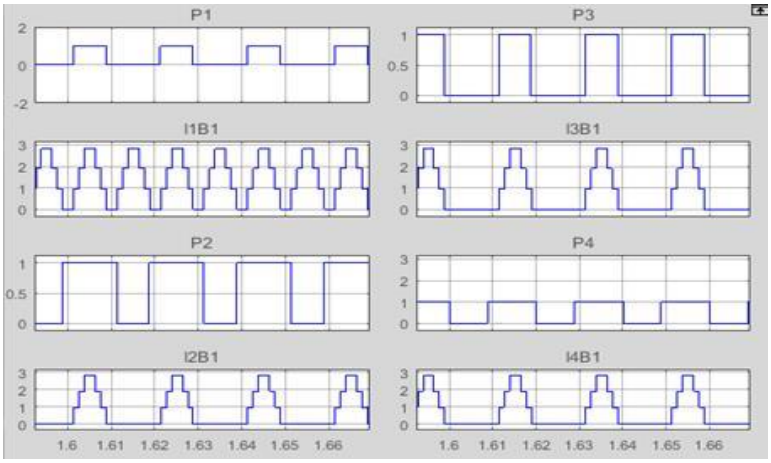

Figure 3. Gate pulse and Current waveforms of switches S_1, S_2, S_3 & S_4 of Cascaded Multilevel Inverter

The power loss in switches S_1, S_2, S_3 & S_4 of CMLI are given in Table 3. Similarly, power loss in switches S_5-S_{12} of CMLI are given in Table 4.

Table 3. Power loss in Switches S_1, S_2, S_3&S_4 of CMLI

Switch number	Current in the Switch	Duty Cycle	Ploss
S_1	2.2715	0.4	0.0206
S_2	1.6062	0.7	0.0180
S_3	1.6062	0.4	0.0103
S_4	1.6062	0.6	0.01548

Table 4. Power Loss in Switches S_5- S_{12} of CMLI

Switch number	Current in the Switch	Duty Cycle	Ploss
S_5	2.218	0.025	0.00123
S_6	1.72	0.75	0.0222
S_7	1.569	0.3	0.0074
S_8	1.1406	0.95	0.0123
S_9	1.534	0.15	0.0035
S_{10}	1.084	0.85	0.0099
S_{11}	1.084	0.15	0.0017
S_{12}	1.228	0.904	0.0136

Failure rate of all switches, and hence failure rate of the system, is calculated as,
$\lambda_{ps} = \Sigma \lambda_n = 2.028*10^{-5}$

Product Reliability [14] is quantified as MTBF (Mean Time between Failures) for repairable product. MTBF is a quantity which measures the reliability level of the product. Hours is usually its unit. The higher the MTBF, the more reliable the product is. MTBF of the CMLI is given as 49309 million hours.
% Efficiency= (Output Power/Input Power)*100

The efficiency of the CMLI is calculated by looking at the output power and input power. From the simulation results is calculated as 90.33%

4. PROPOSED NEW MULTI-LEVEL INVERTER

The switch requirement of the proposed new MLI is given in Table 5. In the proposed new inverter, the number of switches used for the same level of output is lesser when compared to Cascaded multilevel inverter. Here only two switches conduct at a time to achieve the required voltage level. This makes the gate driver circuit simple. The circuit diagram of the proposed new MLI is shown in Figure 4.

Table 5. Switch Requirement for Proposed Multilevel Inverter

Parameters	Proposed Inverter			
Levels	7	9	11	13
Switches required	8	10	12	14

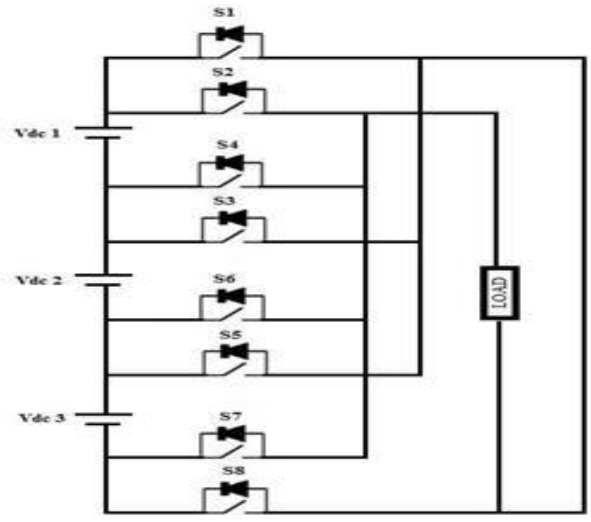

Figure 4. Circuit diagram of new proposed multilevel inverter

Table 6 shows the switches which are conducting for different voltage levels in the proposed MLI.

Table 6. Conducting Switches of Proposed Multilevel Inverter for Different Voltages

Sl.No.	Switches which are conducting	Output Voltage
1	S_6, S_8	$+V_{dc}$
2	S_4, S_8	$+2V_{dc}$
3	S_2, S_8	$+3V_{dc}$
4	Nil	0
5	S_5, S_7	$-V_{dc}$
6	S_3, S_7	$-2V_{dc}$
7	S_1, S_7	$-3V_{dc}$

Using MATLAB/SIMULINK for input voltage of $V_{dc1}=V_{dc2}=V_{dc3}=10V$, the simulation of the new MLI is performed and the waveform of the output voltage is shown in Figure 5.

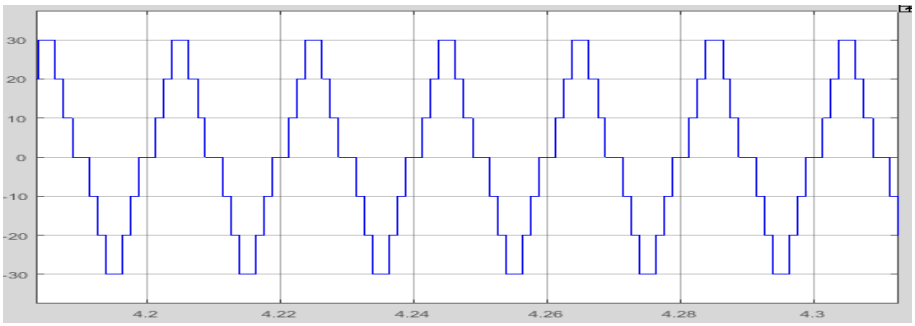

Figure 5. Output Voltage waveform of new MLI

5. RELIABILITY ANALYSIS OF NEW PROPOSED MULTI-LEVEL INVERTER

Similar to cascaded multi-level inverter, for calculating the power loss of the switches, the switch current waveforms are analyzed. The reliability of the new MLI, is calculated by using the relations, equations and coefficients are referred from MIL-HDBK-217. Gate pulse and Current waveforms of switches S_1, S_2, S_3 & S_4 of new MLI inverter is shown in Figure 6.

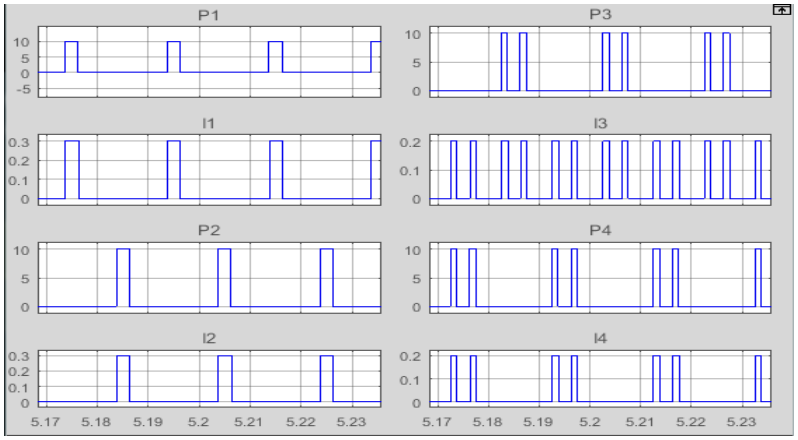

Figure 6. Gate pulse and current waveforms of switches S_1, S_2, S_3 & S_4 of new MLI

The power loss in switches S_1, S_2, S_3 & S_4 of proposed new MLI are given in Table 7.

Table 7. Power Loss in Switches S_1, S_2, S_3&S_4 of Proposed New MLI

Switch number	Current in the Switch	Duty Cycle	Ploss
S_1	0.11618	0.15	$2.024*10^{-5}$
S_2	0.11618	0.15	$2.024*10^{-5}$
S_3	0.10583	0.14	$1.5679*10^{-5}$
S_4	0.07211	0.13	$6.75*10^{-6}$

Similarly, the power loss in switches S_5, S_6, S_7 & S_8 of proposed MLI is given in Table 8

Table 8. Power loss in Switches S5, S6, S7 & S8 of proposed new MLI

Switch number	Current in the Switch	Duty Cycle	Ploss
S_5	0.0529	0.14	$3.91*10^{-6}$
S_6	0.036	0.13	$1.68*10^{-6}$
S_7	0.16124	0.4	$1.03*10^{-4}$
S_8	0.13964	0.5	$9.74*10^{-5}$

Failure rate of all switches, and hence failure rate of the system, is calculated as,

$\lambda_{ps} = \Sigma \lambda_n = 1.352*10^{-5}$

Mean time between failure of the new MLI is 73964 million hours. From the simulation results the efficiency of the proposed new MLI is calculated as 95.45%.

We can infer that proposed new MLI has better reliability indices and better efficiency than CMLI, due to decrease in number of switches. Further analysis of the new inverter with different quality component reveals that the inverter with S grade is having better reliability than components with grades R, P, M or commercial. Table 9 gives the reliability of DC-AC improved multilevel inverter circuit with different quality grade components.

Table 9. Reliability for Different Grade Component

Sl.no	Component Grade	Quality Factor πQ	Switch λp	Failure Rate λps	MTBF (*106 Hours)
1	S	0.03	9.34*10-9	7.472*10-8	13381995
2	R	0.1	3.11*10-8	2.49*10-7	4014598
3	P	0.3	9.34*10-8	7.472*10-7	1338199
4	M	1.0	3.11*10-7	2.49*10-6	401459
5	Commercial	5.5	1.71*10-6	1.352*10-5	73964

6. CONCLUSION

In this paper, a simulation model of existing CMLI is constructed and its reliability and efficiency is calculated. Also a novel MLI has been built using MATLAB/SIMULINK and its reliability and efficiency is evaluated. It is found that for both reliability and efficiency, the proposed new novel MLI is better than its counterpart. Moreover, the MTBF of the new MLI is 1.5 times that of the cascaded multilevel inverter and there is a 5% increase in efficiency. Also, the new inverter is analysed for different quality of components which reveals that inverter with S grade component is most reliable.

REFERENCES

[1] Franquelo, L.G., Rodriguez, J., Leon, J.I., Kouro, S., Portillo, R., and Prats, M.A.M., The age of multilevel converters arrives, *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp.28 -39 2008.

[2] Rashid, M.H, 2004. Power Electronics: circuits, devices and applications. Third Edition, Prentice Hall. (Book)

[3] S. N. Rao, D.V. Ashok-Kumar, C. S. Babu, *Implementation of Cascaded based Reversing Voltage Multilevel Inverter using Multi Carrier Modulation Strategies*, International Journal of Power Electronics and Drive Systems, Vol. 9, No. 1, pp. 220-230, March., 2018

[4] Ibrahim Haruna Shanono, Nor Rul Hasma Abdullah, Aisha Muhammad, *Five-Level Single Source Voltage Converter Controlled Using Selective Harmonic Elimination*, Indonesian Journal of Electrical engineering and computer science, Vol 12, No 3: December 2018

[5] R. Palanisamy, K. Vijayakumar, D. Selvabharathi, *MSPWM Based Implementation of Novel 5-level Inverter with Photovoltaic System*, International Journal of Power Electronics and Drive Systems, vol.8, No.4, pp. 1494-1502, Dec. 2017

[6] Carpita, M & Tenconi, S 1991, *A Novel Multilevel Structure for Voltage Source Inverter*, EPE'91 Conference Proceedings, pp.1.090-1.094.
[7] Bum-Seok, Sinha, G, Manjrekar, MD & Lipo, TA 1998, *Multilevel power conversion-an overview of topologies and modulation strategies*, IEEE Proceedings of the 6th International Conference on Optimization of Electrical and Electronic Equipments, OPTIM'98 vol. 2, pp. AD-11.
[8] Choi, NS, Cho, JG & C'ho, GH 1993, *A General Circuit Topology of Multilevel Inverter*, IEEE -PESC'9l Conference Record, pp. 96-103.
[9] F. Z. Peng and J. S. Lai, *Multilevel cascade voltage-source inverter with separate DC sources*, U.S. Patent 5 642 275, June 24, 1997
[10] Dixon, J & Moran, L 2006, High-level multistep inverter optimization using a minimum number of power transistors, *IEEE Trans. Power Electronics*, vol. 21, no. 2, pp. 330-337.
[11] Najafi, E &Yatim, AHM 2012, Design and implementation of a new multilevel inverter topology, Industrial Electronics, *IEEE Transactions*, vol. 59, no. 11, pp. 4148-4154
[12] MIL-HDBK-217, Reliability Prediction of Electronic Equipment (Book).
[13] M.Sujatha, A.K.Parvathy, *Reliability Analysis of Boost Converter Used for Solar PV System*, Jour of Adv Research in Dynamical & Control Systems, 11-Special Issue, November 2017, ISSN 1943-023X, pp.703-709, Nov 2017
[14] Ebeling, C. E, An introduction to Reliability and Maintainability Engineering, Tata McGraw Hill Publishing Company Limited, New Delhi, pp. 189-275, 2005

BIOGRAPHIES OF AUTHORS

M.Sujatha received her B.E., degree from Alagappa Chettiar College of Engg., and Technology, Karaikudi in 1997 and M.E., degree from College of Engineering, Guindy, Anna University, Chennai in 2009. She is a member of ISTE and IET. She is currently working as Assistant Professor with the department of electrical and electronics engineering in Hindustan Institute of Technology and Science and working towards Ph.D. degree in the area of reliability improvement of converters and inverters. Her areas of interest include Power Electronics and Renewable Energy

Dr.A.K.Parvathy received her B.Tech. and M.Tech. degrees from Calicut University, India, in 1993 and 1998 respectively. She obtained Ph.D. in Advanced Control of PMSM from Anna University, Chennai, India in 2013. She is serving as Professor & Head of Department, Department of EEE, HITS, Chennai. She has published around 30 papers in International and National journals and conference proceedings. Her research interests are linearization, motion control and renewable energy sources.