Rectifier for RF energy harvesting using stub matching

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ABSTRACT

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Dickson Multiplier Energy Harvesting Stub Matching One of challenge in rectenna design is the impedance matching of the antenna to the rectifier load. Rectifier exhibits complex impedance while antennas are normally designed to match either 50 Ω or 75 Ω loads. For the optimum power transfer between antenna and the rectifier circuit, both impedances should be matched. This paper presents the design and development of the 7-stages Dickson multiplier in energy harvesting. The objective of this paper is to analyze the performance of the designed multiplier together with matching circuit. An improvement of 60% output voltage is achieved by feeding -30dBm of low input power at the multiplier circuit.

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1. INTRODUCTION

Energy harvesting has been topic of interest by many researchers' years before as world are looking for renewable energy to replace current energy source [1]-[10]. Radio frequency (RF) became a more popular source in harvesting energy for its availability and easy scavenging system compared to others source such as wind, solar, vibration, piezoelectric and thermal. All this source are far beyond our control, for example thermal needs heat, solar requires light present and vibration needs motion [7].

RF energy can be harvested either from ambient or from dedicated source. A device designed to collect the electromagnetic energy in the free space and transform into direct current (DC) is called rectenna. Figure 1 shows general block of rectenna where it is basically a combination of rectifier and antenna. Matching circuit is applied between the antenna and the rectifier circuit.



Figure 1. General block diagram of Rectenna

In high frequency analysis, impedance matching is one of important aspect. The impedances of antenna and rectifier circuits are need to be matched, in which it can avoid of the transmitted wave reflected back and for a maximum power transfer. A good matching network will allow a maximum power transfer between the antenna and the rectifier circuit.

The number of RF transmitters will continue to growth along with the number of mobile subscriptions. Hence, there are great potential in harvesting the energy from Global System for Mobile Communication (GSM) frequency band. Many approaches have been proposed previously such as adding parasitic elements [8], L or T-matching [9] and [10] and stub matching techniques [11] – [15]. RF-to-DC efficiency of 45% at 868 MHz with an optimum load of 2.5 k Ω is presented in [9] after L matching is applied to the rectifier circuit. Authors in [11] successfully invented an efficient of single stage RF energy harvester module at 900 MHz with exhibits a direct current (DC) rectified voltage of 1.25 V at 0.5 m where they implemented a capacitor with stub matching in the matching circuit. Different matching circuits were analyzed in [12] with a 4-stage Villard rectifier. In their work, the shorted stub matching performed better for low power input in the range from -30 dBm to -5 dBm.

A multistage rectifier, otherwise known as voltage multiplier has been focus in this work together with a stub matching network. The frequency of interest in the designed circuit is GSM band as the received signal strength is higher compared to other ambient RF signal. Due to nonlinear behavior of the diode in rectifier circuit, a proper matching between rectifier and antenna is needed. An increment in the rectified output voltage is demonstrated after the matching circuit is applied before the designed multiplier circuit.

2. DESIGN

In this section, rectifier and matching circuit will be discussed individually.

2.1. Rectifier Design

The rectifier describes is this paper is based on 7-stage Dickson multiplier with Schottky diode as stated in Figure 2. Each stage is consisting of two diodes and two capacitors. The RF input power in RF energy harvesting system is typically small, thus the DC harvested from a single stage rectifier is not enough. Therefore, to obtain a higher DC voltage the circuit is cascaded into multiple stage. The cascaded circuit is called Dickson multiplier. In 2003, Karthaus and Fischer [6] had modified the original Dickson topology by eliminating the need of clock pulses and reducing the number of coupling and stray capacitors.

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Figure 2. Dickson n-stage Rectifier Configuration [6]

The rectify elements in the circuit mainly determines the RF to DC conversion efficiency and Schottky diodes appeared to be a good candidate as they been widely used [3]-[7]. Due to high operating frequency and low input power, diodes have a very fast switching time and the lowest possible turn on voltage [4]. Schottky diodes offer great advantages in terms of speed because it does not rely on holes or electrons recombining when they enter the opposite type of region as in the case of a conventional diode. As a result, HSMS2850 Schottky diodes are selected based on the low turn on voltage. The diode itself has been designed and optimized for use in small signal (for input power less than -20 *dBm*) applications at frequencies below 1.5 GHz [16]. 47 *pF* capacitor is used in each stage capacitor and the load is 100 *nF* parallel with 100 k Ω . The circuit has been simulated based on a low cost FR-4 board (with dielectric constant, $\epsilon_r = 4.6$, and substrate thickness, t = 1.6 mm). The circuit dimension is 73 mm x 60 mm. All the design and result are simulated by using Advanced Design System (ADS) software.

2.2. Matching Circuit

Impedance matching is one of the important aspects of high frequency circuit analysis. The design circuit has to be impedance matched for a maximum power transfer between the receiving antenna and the rectifier circuit. Single stub matching will be discussed further in this paper.

A single stub matching technique is suitable for matching any complex load to characteristic impedance. Unlike a quarter wavelength transformer, the stub matching is designed by using 50Ω transmission line for both main line and stub. Stubs are shorted or open circuit lengths of transmission line intended to produce a pure reactance at the attachment point, for the line frequency of interest. Figure 3 (a) and (b) describe parallel and series single stub matching network. Parallel stub matching is preferable since it easier and feasible for microstrip board application. The stub matching can be either shorted or open stub depends on the constraint of the design. Generally, one will choose based on which topology gives the shortest length, in the range of less than half a lambda (λ). For a wider bandwidth, stubs are supposed to be as short as possible.

In Figure 3, Z_L is the load impedance, Z_o is the characteristic impedance which in this case it is 50 ohm antenna impedance, 1 is the stub length and d is the length from stub to the load. With stub added in the transmission line between Z_o and Z_L at a certain length, the impedance seen beyond the stub is equal to the characteristic impedance. For a parallel stub matching, it is convenient to express the impedance-matching process using admittances rather than impedances. Initially, the load impedance is converted to normalize admittance.



Figure 3. Single Stub Matching Configuration (a) parallel and (b) siries

$$Z'_{L} = \frac{Z_{L}}{Z_{0}}$$

$$\tag{1}$$

$$Y'_{L} = \frac{1}{Z'_{L}}$$
(2)

$$Y_X = Y_{stub} + Y(d_{stub}) \tag{3}$$

$$Y_{stub} = jB_{stub} \tag{4}$$

$$Y(d_{stub}) = Y_0 + jB(d_{stub})$$
⁽⁵⁾

A stub should be placed at a location where the line admittance has a real part that equal to Y_o . As show in equation (4), stub admittance is an imaginary, either capacitance or inductance. To obtain matched condition, susceptsance (*B*) of stub and *dstub* should be equal in value with opposite polarity. As shown in Figure 4, the input impedance at 915 MHz is equal to 12 - j 39.8 Ω , which is complex negative reactance impedance. Smith Chart is used to find the stub length (*d*) and the line length from load impedance (*l*). Applying both formula (1) and (2), the normalized admittance is calculated as $0.347 + j1.15 \Omega$. Then, the value Y'L is plotted on the smith chart. Using smith chart tools provided in ADS software, value of stub length and stub location can be calculated.





Figure 4. Impedance of the multiplier simulated at 915 MHz

As can be seen in Figure 5, the length of open is greater than half a λ compared to shorted stub. Figure 6 shows the proposed stub matching circuit in ADS environment. From the calculation, stub location occurs at 9.13 mm and the stub length of open and shorted are found as 55.97 mm and 11.79 mm respectively



Figure 5. Smith Chart (admittance plot) plotted to find stub length (a) open parallel stub and (b) shorted parallel stub



Figure 6. Proposed matching network (a) open parallel stub, and (b) shorted parallel stub

The width is calculated at transmission line characteristic impedance, which is 50 Ω . Reflection coefficient of both stub matching is showed in Figure 7. Shorted stub matching give a deeper and wider bandwith, which is -22.78 dB with a bandwitdh of 246 MHz. While, less bandwitdh is obtained in open stub simulation, 83 MHz with -20.45 dB deep.



Figure 7. Reflection Coefficient of the proposed stub matching

3. SIMULATED RESULTS AND ANALYSIS

Results are simulated by using Advanced Design System 2013 (ADS). The circuit dimension with stub matching are 106 x 103 mm and 106 x 60 mm for the open and shorted stub. The rectified output voltage is simulated across 100 nF parallel with 100 k Ω loads. Results are attained for both open and shorted stub attached to the multiplier circuit, where both circuit resonate at 915 MHz with -26 dB return loss. A bandwidth of 7 MHz and 8 MHz were obtained for open and shorted stub respectively, as shown in Figure 8.



Figure 8. Reflection Coefficient of the multiplier with the matching network

The rectified output voltage of the circuit is then measured to verify the circuit performance without and with matching circuit. At the resonant frequency, the result showed that there are improvements in the rectified output for low input power ranging from -30 dBm to 0 dBm after the matching network is applied in front of the circuit.A maximum increase of 60% was achieved in rectified output voltage during -30 dBm input power for multiplier with matching circuit. 1.49 V and 1.50 V are achieved at -10 dBm input power for circuit with open and shorted stub matching, while 1.05 V for circuit without matching. The details result is illustrated in Table 1.

Table 1. Simulated results with open and shorted stub matching network for the proposed multiplier

Pin (dBm)	Without Stub		Open Stub		Shorted Stub	
	Io (mA)	Vo(V)	Io (mA)	Vo(V)	Io (mA)	Vo(V)
-30	0.04	0.02	0.06	0.05	0.06	0.05
-25	0.07	0.06	0.13	0.13	0.14	0.31
-20	0.15	0.15	0.26	0.33	0.27	0.33
-15	0.31	0.41	0.49	0.73	0.50	0.74
-10	0.66	1.05	0.88	1.49	0.86	1.50
-5	1.40	2.53	1.54	2.80	1.55	2.81
0	3.17	5.97	2.66	4.97	2.67	4.97
5	5.32	10.46	4.42	8.23	4.43	8.24
10	6.72	15.63	6.09	14.28	6.12	14.30

Figure 9 shows the output power versus input power of the rectifier cricuit. The multiplier with mathcing circuit are able to increase the output voltage at low input power. Multiplier with shorted stub matching circuit exhibits greater output power for -30 dBm to -20 dBm input power. Whereas, for the rest of the tested input power, a good agreement has been achieved in the output power for both open stub and shorted stub circuit. Data in Table 1 showed the maximum output current and rectified output voltage at 915 MHz for multiplier without stub, with open and shorted stub matching circuit. From the results, both matching network are successfully increased the output voltage of the rectifier at low input power.

As a summary, both of the matching circuits have successfully increase the output voltage of the multiplier when low input power is applied to the circuit. Shorted stub matching is less prone to electromagnetic radiation leakage as in this work it provides 3% higher output with less board size compared to open stub. However, open stub may become more practical on microstrip where it does not use short via as a ground terminal.



Figure 9. Rectified Output Power of the multiplier circuit simulated at 915 MHz

4. CONCLUSION

A matching using stub element has been discussed in order to enhance the efficiency of the multiplier circuit at low power level. Simulation results from both circuits have been presented to verify the matching circuits are able to increase multiplier efficiency. A multiplier with shorted circuit stub gives better results compared to open circuit stub with smaller physical dimension.

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