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A memristor-based chaotic-masking for analog spread-spectrum communication

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Article Info

ABSTRACT

This paper presents a simple chaotic-masking system. The system uses a chaos generator built around a grounded memristor. The memristor is emulated using the current-feedback operational amplifier (CFOA). At the sending end the signal is masked by adding chaos. At the receiving end the signal is recovered by subtracting the chaos. The performance of proposed system is investigated using sinusoidal and square wave signals.

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1. INTRODUCTION

Constantly reliable and secure systems are of primary interest in modern communication systems; especially in military applications. Moreover, due to power and weight limitations, especially for hand-held systems, small power, reliable, secure and simple communication systems are of great interest. Spread spectrum techniques afford the ability of the transmitter to avoid any interruption by unauthorized systems. Over the years a number of spread spectrum systems have been developed and are widely used; see for example the frequency hopping technique.

On the other hand, secure communication systems can be implemented using chaotic signals. These chaotic signals are noise like, aperiodic, very sensitive to initial conditions and have a broadband. Nevertheless, chaotic signals have a deterministic behavior. Thus, while a sinusoidal carrier would produce a spectral power density that concentrates in a narrow band of frequencies, chaotic signals would produce a wide bandwidth. This explains why chaotic signals can be used for spreading the information of interest. In this regard it is similar to the spread spectrum technique. Therefore chaotic signals are strong candidates for analog scrambling of signals of interest. This would produce a simple analog implementation for signal scrambling if compared to the much more sophisticated digital encryption techniques.

Over the years many chaotic scrambling techniques have been developed; see for example [1]-[6]. Most of these techniques use a chaos generator built around Chua's chaotic oscillator. No attempt has been made, so far, to develop a scrambling circuit built around a memristor-based chaotic oscillator circuit. The memristor is the fourth electrical engineering element. While the resistance links the voltage and the current, the capacitance links the voltage and the charge, the inductor links the current and the flux, the memristor links the flux and the charge. In this work we investigate the feasibility of designing a new analog scrambling technique using a memristor-based chaotic generator. Such an approach would provide

simpler ide a simpler realization for the analog scrambling technique that can be easily implemented using a fewer number of active and passive elements.

2. PROPOSED APPROACH

The block diagram of the proposed chaos-based scrambling technique using a memristor-based chaos generator is shown in Figure 1.
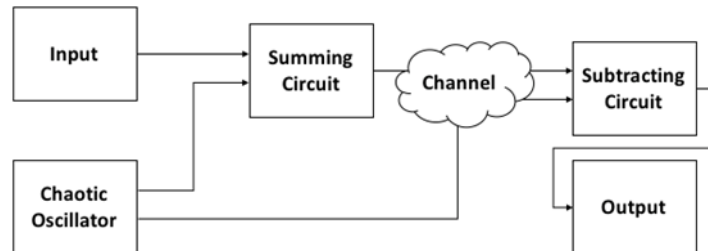

Figure 1. Block diagram of the proposed chaos-based scrambling technique

The block diagram of Figure 1 comprises a chaotic oscillator circuit. In this work this circuit is implemented using the Wien bridge oscillator circuit shown in Figure 2. As shown in Figure 2 one of the resistors of the classical Wien bridge oscillator is replaced by a memristor.
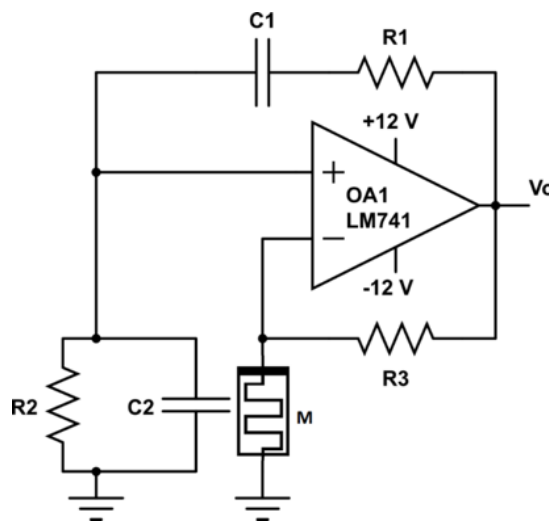

Figure 2. Memristor-based Wien bridge oscillator

Classical analysis of the circuit of Figure 2, with the operational amplifier assumed ideal, yields the characteristic shown in (1).

$$as^2 + bs + c = 0 \tag{1}$$

The parameters in (1) are given by

$$a = C_1 C_2 R_1 R_2 R_M(t) \tag{2}$$

$$b = (C_1 R_1 + C_2 R_2) R_M(t) - C_1 R_2 R_3 \tag{3}$$

$$c = R_M(t) \tag{4}$$

As shown in (2)-(4), $R_M(t)$ represents the memristor resistance. In order to calculate the frequency and the condition of oscillation of the circuit of Figure 2, the poles of the oscillator circuit of Figure 2 must be calculated using (1). This yields

$$s_{1,2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{5}$$

As shown in (5) the frequency and the condition of oscillation of the oscillator circuit of Figure 2 can be expressed as

$$\omega_0^2 = \frac{1}{R_1 R_2 C_1 C_2} - \varepsilon^2 \tag{6}$$

$$\varepsilon = \frac{(C_1 R_1 + C_2 R_2) R_M(t) - C_1 R_2 R_3}{2 R_1 R_2 C_1 C_2 R_M(t)} \tag{7}$$

and

$$R_2 R_3 C_1 > (R_2 C_2 + C_1 R_1) R_M(t) \tag{8}$$

At present memristors are not commercially available at a low cost. Therefore, recourse to memristor emulation is a must in order to test the operation of the oscillator circuit of Figure 2. While there are a large number of memristor emulators available in the open literature, the memristor emulator circuit used in this work is shown in Figure 3 [7]. As explained in [7], the circuit of Figure 3 is operating to satisfy the characteristic equations and relations between the charge through the mutator and the flux linkage as shown in (9) and (10).
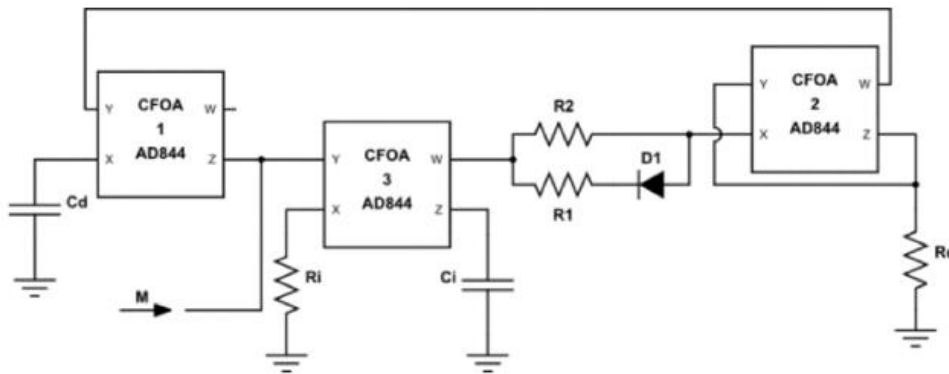

Figure 3. Memristor emulator [7]

$$v_R = \frac{-1}{C_i} \int i_M \, dt + i_R R_d \tag{9}$$

$$v_M = -R_i R_d C_d \frac{d}{dt} i_R \tag{10}$$

According to (9), the input current i_M will be integrated by the capacitor C_i and then scaled through the non-linear resistor; formed of the resistors R_1, R_2 and the diode D, with the inverting amplifier formed of CFOA3 and the resistor R_d. Then, according to (10) the output signal of this non-linear scalar is differentiated by the capacitor C_d to obtain the voltage v_M. Thus, the relationships between the input voltage v_M and the input current i_M, and the voltage across the nonlinear resistor v_R and the current through the nonlinear resistor i_R can be expressed as in (9) and (10).

Figure 4 shows a possible circuit representation of (9) and (10). Figure 4 represents the transformation of a current-controlled resistor into a flux-controlled memristor. It is worth mentioning here that connecting a resistance in parallel with the capacitor C_i, then rather than integrating the input current i_M with an ideal integrator, the integration will be performed by a nonideal integrator formed of C_i in parallel with this resistance. This will not change the equivalent circuit of Figure 4. It will remain valid except that the integrator is nonideal. If the input current i_M is a sinusoidal current of the form $i_M = I_{max} \sin \omega t$ and the voltage v_R can be expressed as $v_R = i_R R_{eq}$ where R_{eq} is the effective equivalent resistance of R_1 and R_2; this equivalent resistance depends on the values of R_1 and R_2 and the status of the diode D. Thus, using (9) and (10) and assuming that R_{eq} is always larger than R_d, it is easy to show that equivalent resistance of the memristor can be expressed as

$$M = \frac{R_i R_d C_d}{(R_{eq} - R_d)C_i} \qquad (11)$$

As shown in (11) clearly shows that the memristor is equivalent to a nonlinear resistor with a resistance which is dependent on R_{eq}. This is attributed to the fact that R_{eq} can acquire two different values depending on the status of the diode D. Thus, (11) shows that the memristor can acquire two values of resistance that is RON and ROFF.
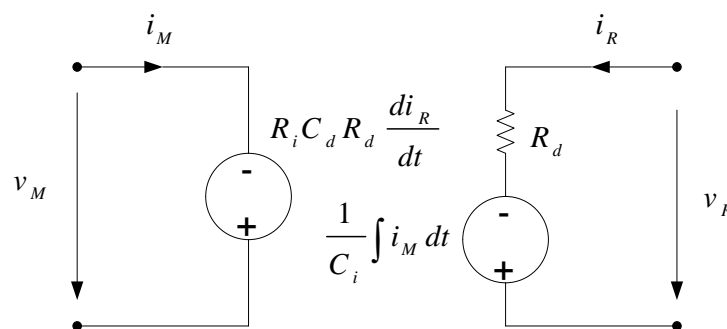

Figure 4. Memristor equivalent circuit

3.   EXPERIMENTAL RESULTS
The proposed analog scrambling technique of Figure 1 was tested using the circuits of Figure 2 and Figure 3. The used components are shown in Table 1 and the results obtained are shown in Figures 5-Figure 9.

Table 1. List of Components used in the Experimental Testing of the Proposed Scrambling Technique

Memristor emulator	
R1	9 kΩ
R2	18 kΩ
Ri	Variable 50 kΩ
Rd	Variable 5 kΩ
Ci & Cd	200 nF
Wien-Bridge oscillator	
R1 & R2	5 kΩ
C1 & C2	5 nF
R3	Variable 5 kΩ
Summing & Subtracting circuits (Op-Amps)	
All resistors	1kΩ

Figure 5 shows the chaos produced by the circuit of Figure 2 using the memristor emulator of Figure 3. Inspection of the results shown in Figs. 6-9 clearly shows that the concept of chaos-based scrambling using memristor-based chaos generator is feasible with the received sinusoidal/square waves are almost identical to the sent signals.
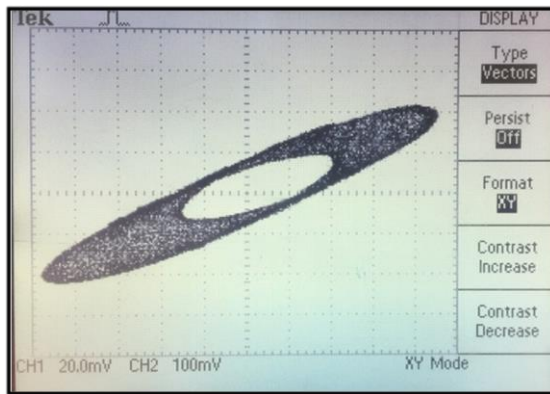

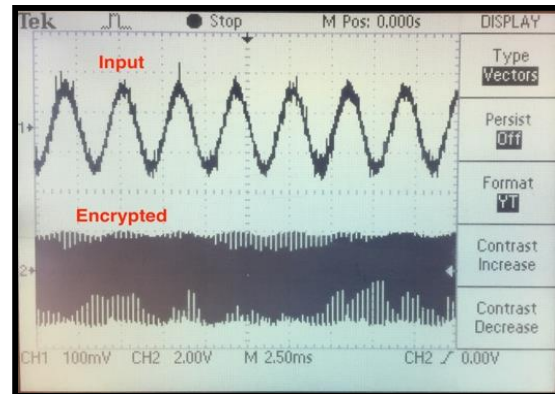Figure 5. Chaotic oscillator phase diagram

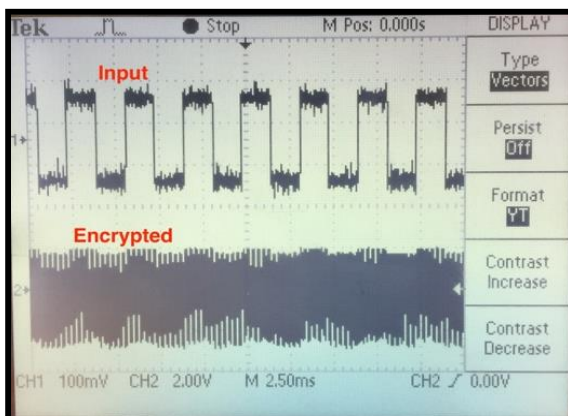Figure 6. Sinusoidal input with its corresponding encrypted signal

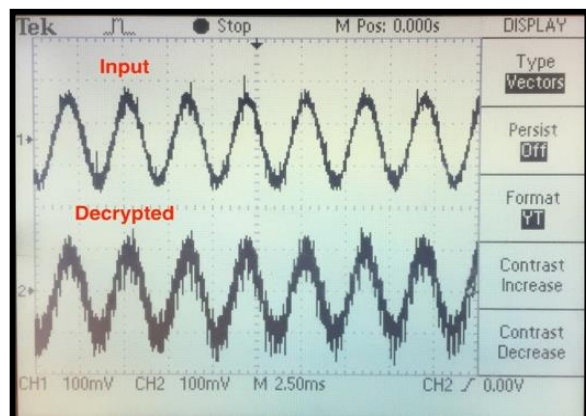Figure 7. Square input with its corresponding encrypted signal

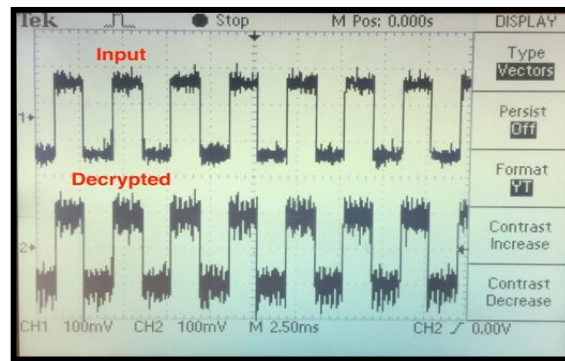
Figure 8 Decrypted sinusoidal signal

Figure 9. Decrypted square signal

4.   CONCLUSION

This work presented a simple realization for chaos-based scrambling technique using a memristor-based chaotic circuit. The proposed realization is simple and uses off-the-shelf components. The experimental results obtained confirm the functionality of the proposed circuit. In the presented work, the chaos needed at the receiving end was obtained directly from the chaos generator at the sending end. Further work is still needed to synchronize the chaos generator at the receiving end with the chaos generator at the sending end.

REFERENCES

[1]   K. Murali and H. Leung and H. Yu, Design of noncoherent receiver for analog spread spectrum communication based on chaotic masking, IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 50, 2003, pp. 432-441.
[2]   M. ZapateiroDe la Hoz et. al., A modifiued Chua chaotic oscillator and its application to secure communication, Applied Mathematics and Computation, Vol. 247, 2014, pp. 712-722.
[3]   G. Kenfack, et. al., Chaos-based encryption of ECG signals: Experimental results, Journal of Biomedical Science and Engineering, Vol. 7, 2014, pp. 368-379.
[4]   R. Trejo-Guerra et. al., Chaotic communication system using Chua's oscillators realized with CCII+s, International Journal of Bifurcation and Chaos, Vol. 19, 2009, pp. 4217-4226.
[5]   N.J. et. al., Chaotic scrambling for wireless analog video, Communications on Nonlinear Science and Numerical Simulation, Vol. 15, 2010, pp. 2504-2513.
[6]   C. Sanchez-Lopez et. al., Design and Applications of Continuous-Time Chaos Generators, in the book "Chaotic Systems" edited by Esteban Tlelo-Cuautle, 2011.
[7]   M.T. Abuelma'atti and Z.J. Khalifa, A new memristor emulator and its application in digital modulation, Analog Integrated Circuits and Signal Processing, Vol. 80, 2014, pp. 577-584.
[8]   H.Kim, M.P. Sah, C. Yang, S. Cho and L.O. Chua, Memristor emulator for memristor circuit applications, IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 59, 2012, pp. 2422-2431
[9]   A.L. Fitch, H.H.C. Lu, X.Y. Wang, V. Sreeram and W.G. Qi, Realization of an analog model of memristor based on light dependent resistor, Proceedings of the IEEE International Symposium on Circuits and Systems, 2012, pp. 1139-1142
[10] J. Valsa, D. Biolek and Z. Biolek, An analogue model of the memristor, International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, Vol. 24, 2011, pp. 400-408
[11] M.T. Abuelma'atti and Z.J. Khalifa, A new memristor emulator and its application in digital modulation, Analog Integrated Circuits and Signal Processing, Vol. 80, 2014, pp. 577-584
[12] Z. Biolek, D. Biolek and V. Biolkova, SPICE model of memristor with nonlinear dopant drift, Radioengineering, Vol. 18, 2009, pp. 210-214
[13] Z. Kolka, D. Biolek and V. Biolkova, Hybrid modelling and emulation of mem-systems, International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, Vol. 25, 2012, pp. 216-225
[14] D. Biolek, J. Bajer, V. Biolkova and Z. kolka, Mutators for transforming nonlinear resistor into memristor, Proceedings of the 20th European Conference on Circuit Theory and Design, ECCTD2011, 2011, pp. 488-491
[15] V. Biolkova, D. Biolek and Z. Kolka, Unified approach to synthesis of mutators employing operational transimpedance amplifiers for memristor emulation, Proceedings of the 11th International Conference on Instrumentation, Measurement, Circuits and Systems, 2012, pp. 110-115
[16] P.S. Maheshwar, C. Yang, H. Kim and L. Chua, A voltage mode memristor dridge synaptic circuit with memristor emulators, Sensors, Vol. 12, 2012, pp. 3587-3604