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Design and implementation of AMBA bridge protocol in System-on-Chip design

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ABSTRACT

The Advanced Microcontroller Bus Architecture (AMBA) is widely used in modern technology device. The design of bridge in the system is due to increase demand of power consumption and functionality. The bridge help to reduce power by separate the system into high bandwidth and low bandwidth. The goal of this paper is to design and implement the AMBA bridge into a SoC design which consists of a processor, RAM, ROM, watchdog and LED module. These peripherals are connected separately based on different bandwidth with a bridge as the medium. The result shown the bridge transfer a correct data from the ROM into the RAM. The experiment was carry out using Synopsys 2017 and Keil uVision.

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1. INTRODUCTION

The Advanced Microcontroller Bus Architecture (AMBA) is widely used in many SoC microcontroller and devices. This type of AMBA has a standard interface [1] which is efficient for System on Chip interconnect [2]. The designer just need to design the IP that support AMBA protocol and able to use the buses that will reduce the time to market. The AMBA also can support burst and sequential mode which is suitable for fast memory access.

There are many type of buses in AMBA family such as Advanced Extensible Interface (AXI), Advanced High-performance Bus (AHB), Advanced System Bus (ASB) and Advanced Peripheral Bus (APB). Bridge is one of the important component to connect a high bandwidth bus to a low bandwidth bus for minimum power consumption [3]. The bridge not only need to ensure no data loss during the transfer but the bridge also need to make sure the data transfer between the buses are correct. The bridge will act as master for the APB bus and control the transfer sequence after receive command from AHB bus as shown in Figure 1. The bridge is using finite state machine to determine the stage of transfer and only one peripheral will be selected at one time [4]. There are three stages in the AMBA bridge which are idle stage, setup stage and enable stage.

In this paper, an AMBA bridge has been design to ensure the bridge can support different frequency. The APB frequency using half frequency of the AHB. This two clock is synchronize, in other word, the transmit stage can only be occurred when positive edge of clock. The design was tested using one RAM and ROM in the APB side. The value of the ROM is read and write into the RAM to show the result in simulation.

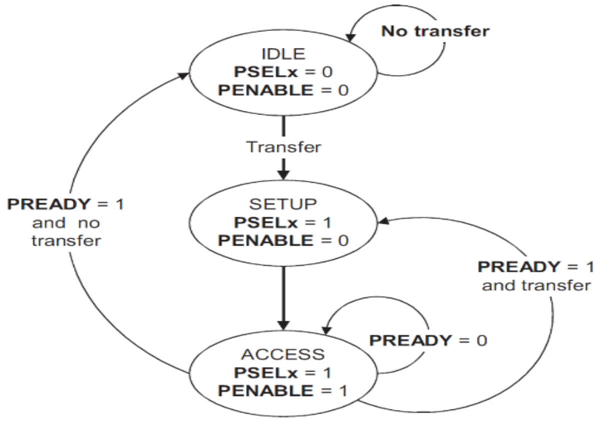

Figure 1. The state machine of AMBA bridge [4]

In paper [5], the author design a different phase and frequency AMBA bridge. The design of the bridge is follow AMBA protocol which the control signal from AHB is delay to APB. The design using handshake signaling method to communicate between AHB and APB. However, this two bus has its own clock frequency, therefore the design include double stage synchronizer inside the bridge to avoid setup and time violation as shown in Figure 2.

The design is verify by using module AHB driver and monitor to act as a master for those buses. These control signals and clock are inserted through an internal memory that act as a bus master. This bus master will write some data to the bridge and receive it after passing through bridge and compare the result. While the APB driver and monitor also insert the signals received from the bridge. The result was successfully synthesized.

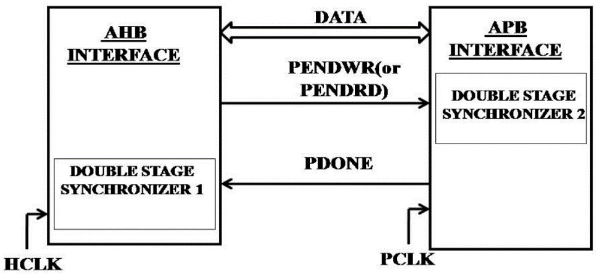

Figure 2. Double synchronizer in the bridge [5]

In paper [6], the author design a low power AMBA bridge. The design consists of a bridge, and a secure UART as the APB slave. The design also have a few states to determine the data transfer stage as shown in Figure 3.

The bridge will keep monitor the signal in the idle state. The signal will go write state or read state depend on the HWRITE signal. If the states is in read states, PSEL will insert. The next state will be READOK allow the data to fetch back to the processor. Then the state will go back to idle state. The same process will go through in the write state. The result also shown that the AMBA 3 specification manage to reduce 6% power and 10% area.

Apart from that, the author in paper [7] had design an IIC IP with Avalon bus. The design combine with other IPs in Quartus II using System on Programmable Chip (SOPC) to become a complete system. The design was verify using Atmel IIC memory.

The SOPC will handle and generate the best Avalon bus for the design. The design include a bus controller, state machine and read and write controller as shown in Figure 4. The design system include processor, memory, PIO, and JTAG. The author then assign the base address and interrupt settings for the peripheral. Next, the SOPC system was generated. A software was included to verify the functionality of the IIC IP core by read and write operation on the IIC memory. The result show that the design can be fast generate using SOPC and shorten the development cycle.

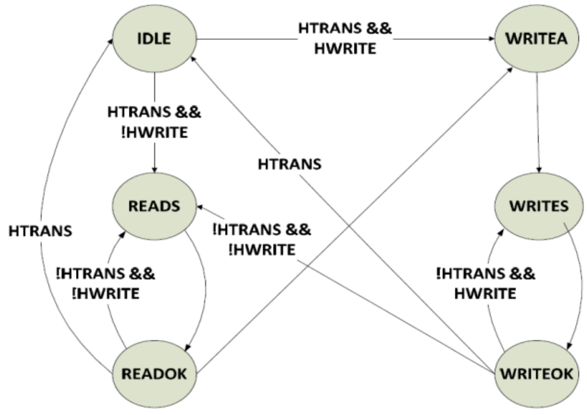

Figure 3. The state machine of the bridge [6]

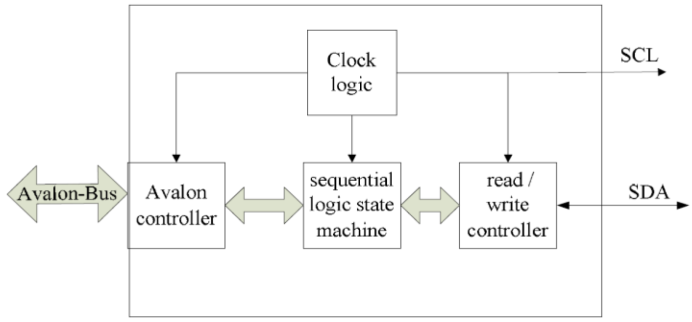

Figure 4. The design of the IIC IP [7]

In paper [8], the author proposed a two layer of buses working based on the Wishbone structure. The double bus interconnect with the peripherals based on the speed of the device. The main purpose for this type of architecture is because the convention wishbone bus does not differentiate high speed bus and low speed bus. This will cause the whole system to run at the speed of the slowest peripheral.

The design then was connect with different devices to form a system based on the double bus. The interconnect structure for the bus is a interconnect matrix which utilize the crossbar switch interconnection structure. It allow different master and different slave communicate simultaneously based on the priority.

The design include a bus bridge between the wb_conmax to encode the address and synchronize the clock. The system was then targeted to Xilinx for verification as shown in Figure 5. The result show that the proposed design increase the logic gate but reduce power consumption.

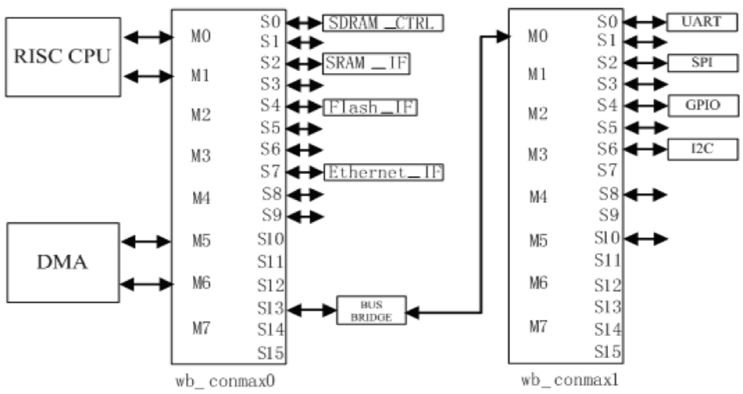

Figure 5. The two layer bridge [8]

The other author [9], had propose an off-the-shelf microcontroller SoC system for system control and support function for complex computer node. The system consists of PowerPC 440 processor, digital Input Output, IIC, JTAG and etc. The system use IBM CoreConnect as internal bus communication. The System have the capability to connect Ethernet based and run the application in order to access the system management units.

The design also include hot plug for the exchange of this microcontroller without affect the system operation. The system can operate simultaneously or as master and slave mode. The slave will replace the master to continue the task if the master fault. The bus use in the design is Processor Local Bus (PLB) which based on CoreConnect architecture as shown in Figure 6.

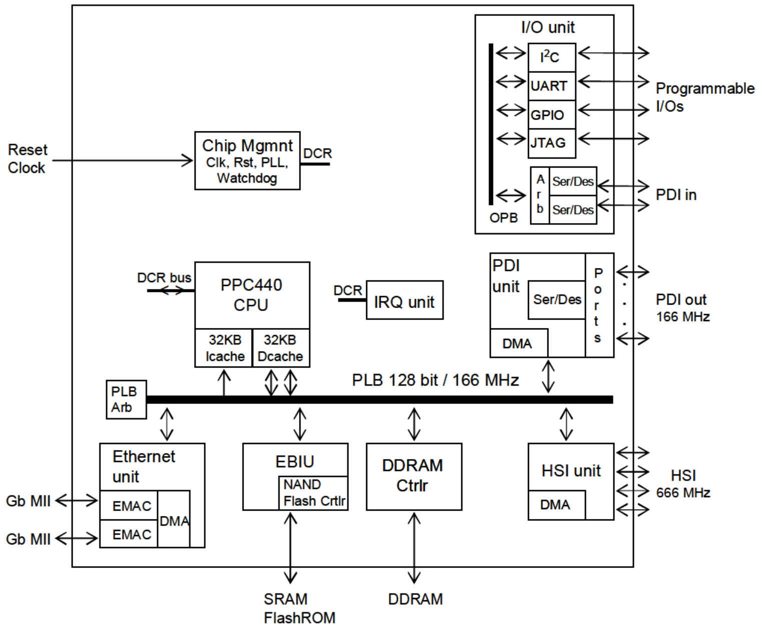

Figure 6. The off-shelf microcontroller system [9]

The bus has a high bandwidth with 166MHz, 128 bits data bus and a round-robin scheme to select the devices. The design ware verified using Cadence Simulator and Cadence Palladium II hardware accelerator.

In conclusion, after a few paper have been reviewed, some aspect of the bus was compared as shown in Table 1. Most of the buses is an open architecture, which mean anyone is allow to build the code. The design of SoC require a standard bus signal in order to achieve time-to-market. Besides, the bus architecture need transfer data without any error for different frequency.

The buses use to compare are AMBA, Avalon, Wishbone and IBM CoreConnect. The AMBA has 32 bits data bus and can support up to 100MHz which is suitable for microcontroller. Meanwhile, Core-connect has 128 bits and can support 166MHz is suitable for high end device. It is found that the AMBA hold more advantage than other type of buses for certain application. Therefore, for this paper, AMBA bus and bridge was chosen as the research purposes for small application. Design such as AES [10] with AMBA interface can be added easily as they have standard interface.

Table 1. Comparison of Different Buses

Features	[5, 6]	[7]	[8]	[9]
Type of bus	AMBA	Avalon	Wishbone	CoreConnect
Topology	Shared bus	Avalon MM	Crossbar switch	PLB
Arbitration	Not used	Not used	Parameterized	Round Robin
Frequency	100MHz	100MHz	100MHz	166MHz
Development cycle	Fast	Fast	Medium	Medium
License	No	Yes	No	No

2. RESEARCH METHOD

In this paper, a system with a processor, an AMBA bus and a bridge are designed. The system using 2 APB module act as RAM and ROM to test the bridge [11][12]. The bridge is design to handle two different frequency, which the APB frequency is half of the AHB.

The bridge has been modify from the ARM bridge with the decoder is build inside on it. The SRAM will later store the application program to verify the design. The LED IP in this design also act as a verification reference to check whether the bridge select the intended IP.The system design is illustrated in Figure 7.

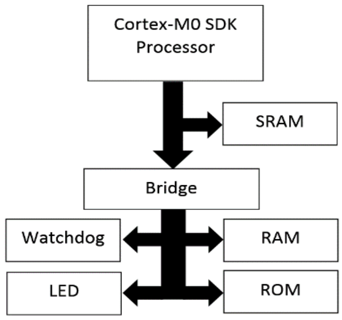

Figure 7. The propose system architecture

Next, this IP is integrated into the system. The memory map is designed as shown in Table 2. The RAM is design with only one address register with 32 bits. The RAM will be store result temporarily data which can be increase the width if needed. Besides, the ROM is design with only four address register which store some data which is 0x40, 0x30, 0x20, and 0x10 as shown in Table 3. The bus will choose the address based on the application program.

Table 2. IP base Address

Module	Base Address	End Address
SRAM	0x0000_0000	0x4FFF_FFFF
LED	0x5000_0000	0x50FF_FFFF
RAM	0x5100_0000	0x51FF_FFFF
ROM	0x5200_0000	0x52FF_FFFF
Watchdog	0x5300_0000	0x53FF_FFFF

Table 3. ROM Address

Module	Base Address	Data
ROM	0x5200_0000	0x40
	0x5200_0004	0x30
	0x5200_0008	0x20
	0x5200_000C	0x10

The next step is using a Hex file to verify the design using simulation waveform [13]. The Hex file for the processor to run the program is created using Keil software. The Hex file is only binary code which only can be understand by processor. There are two steps to run the program. First, the program write a value and a delay for the LED IP to act as a blinking LED. Then, the RAM store the data from SRAM in AHB side which is written in the program. While in next step the ROM data that pre-stored in the Verilog is stored into the RAM.The design of this system use AMBA bus as the internal communication. The design of RAM and ROM contain APB interface to communicate with AMBA.

3. RESULTS AND ANALYSIS

The simulation result using Synopsys is shown in Figure 8. The result shown the RAM store the result 0xF and 0x8 in the first two data set. This store is to prove that the bridge is capable to write the data to the intended peripherals. The RAM then store the value from ROM which are 0x40, 0x30, 0x20 and 0x10. It shows that the bridge able to read data from its peripheral and transfer to other device.

It can be noticed that the PCLK is half of the frequency of clk or HCLK. It can also be notice that the address is point to the intended IP while transfer the data. For example, the 0x30 was read based on the address which is 0x5200_0004 (red circle). The bridge basically control the PENABLE, PSEL, and PWRITE. These signals are purposely extended until the next cycle for synchronous purposes.

The result show that the data transfer as intended even with different clock frequency. The processor Cortex-M0 is obtained from ARM official website [14][15] through ARM University Program.

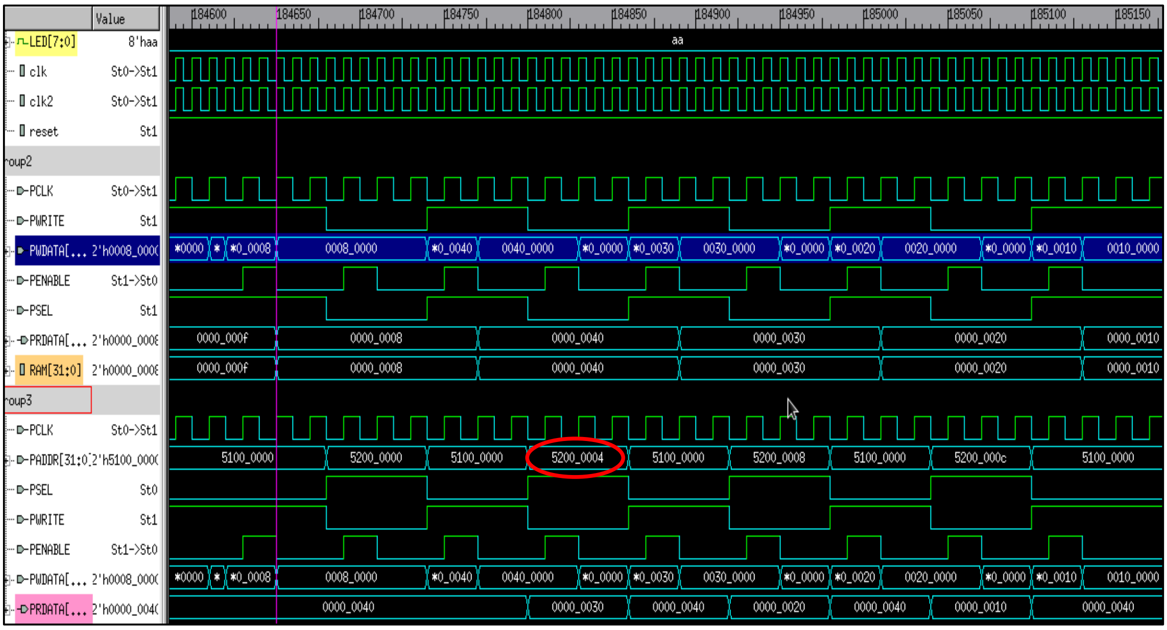

Figure 8. The simulation result for the bridge and the intended IP signal

4. CONCLUSION

This paper has presented the design of a system with a bridge. The main goal of this effort is to design a bridge that can transfer data between two buses with different frequency. The work is implement into a system from the work proposed by [16]. This will reduce some power consumption. The result also shown that the system had transfer the data accurately. In future study, the RAM and ROM IP can be substitute with a more specific purpose IP for a small application.

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REFERENCES

[1] C. Fan, C. Lan, Y. Bo, and O. Ram, “Designing WISHBONE to AMBA Wrapper,” pp. 403–406, 2009.
[2] S. Sombatsiri, K. Kobashi, K. Sakanushi, Y. Takeuchi, and M. Imai, “An AMBA Hierarchical Shared Bus Architecture Design Space Exploration Method Considering Pipeline , Burst and Split Transaction,” 2013.
[3] K. Rawat and K. Sahni, “Design of AMBA APB Bridg ge with Reset Controller for Efficient Power Consumption.”
[4] ARM Ltd, “AMBA APB Protocol Specification,” 2010.
[5] R. M. Vani and M. Roopa, “Design of AHB2APB Bridge for different phase and Frequency,” vol. 3, no. 2, pp. 190–195, 2011.
[6] A. Paunikar and R. Gavankar, “Design and Implementation of Area Efficient, Low Power AMBA-APB Bridge for SoC.”
[7] H. Ji and Y. Wang, “The Design and Simulation of IIC Communication SOPC Core Based on Avalon Bus,” 2015.
[8] C. Dongye, “Design of the On-chip Bus Based on Wishbone,” pp. 3653–3656, 2011.
[9] J. Saalmueller and J. Wuertz, “Embedded controllers for solving complex industry applications,” in *2006 IEEE International Systems-on-Chip Conference, SOC*, pp. 149–152, 2007.
[10] P. Ceminari, A. Arelovich, and D. Federico, “AES block cipher implementations with AMBA-AHB interface,” pp. 1–4, 2017

[11] H. Shah, R. P. Chinmay Modi, and B. Tarpara, "Design & Implementation of Advance Peripheral Bus Protocol," *Int. J. Sci. Eng. Appl. Sci.*, no. 13, pp. 2395–3470, 2015.

[12] M. K. S. Patil, P. G. D. Salunke, B. L. Mahajan, and A. S. Hiwale, "Implementation of AHB Protocol Using FPGA," no. 4, pp. 1122–1131, 2012.

[13] S. Sharma and S. M. Sakthivel, "Design and verification of AMBA APB protocol," *Lect. Notes Electr. Eng.*, vol. 469, no. 1, pp. 247–259, 2018.

[14] ARM Ltd, *Cortex-M0 technical reference manual*. 2009.

[15] ARM Ltd, "Supporting academia towards tomorrow's technology," *ARM Ltd.*

[16] Shankar, D. Girdhar, and N. K. Shukla, "Design and Verification of AMBA APB Protocol," *Int. J. Comput. Appl.*, vol. 95, no. 21, pp. 29–35, 2014.

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